A Product Line of
Diodes Incorporated

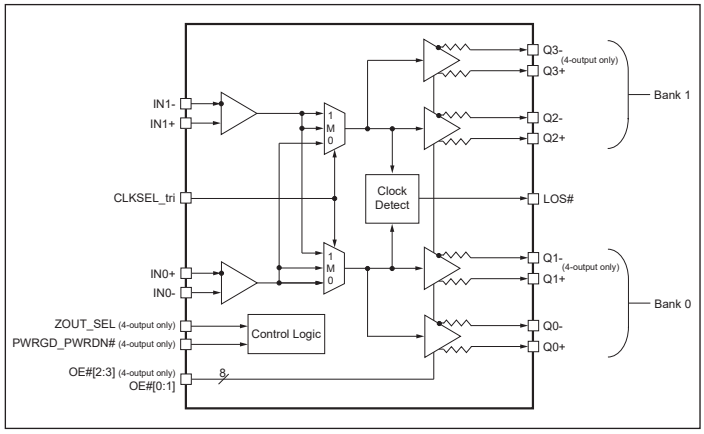
PI6CB332202/PI6CB332204

Low-Power 2-Input Clock Mux for PCIe 6.0 Application

Description

The PI6CB332202/PI6CB332204 is a low-power 2-input PCIe 5.0/6.0 clock mux. It takes two reference inputs to fanout 2/4 low-power differential HCSL outputs up to 400MHz, with on-chip terminations for 85Ω or 100Ω output impedance. An individual OE pin for each output provides easier power management. The device also supports Power Down Tolerant (PDT), automatic output clock locking upon loss of input clock, and Flexible Startup Sequencing features.

Block Diagram



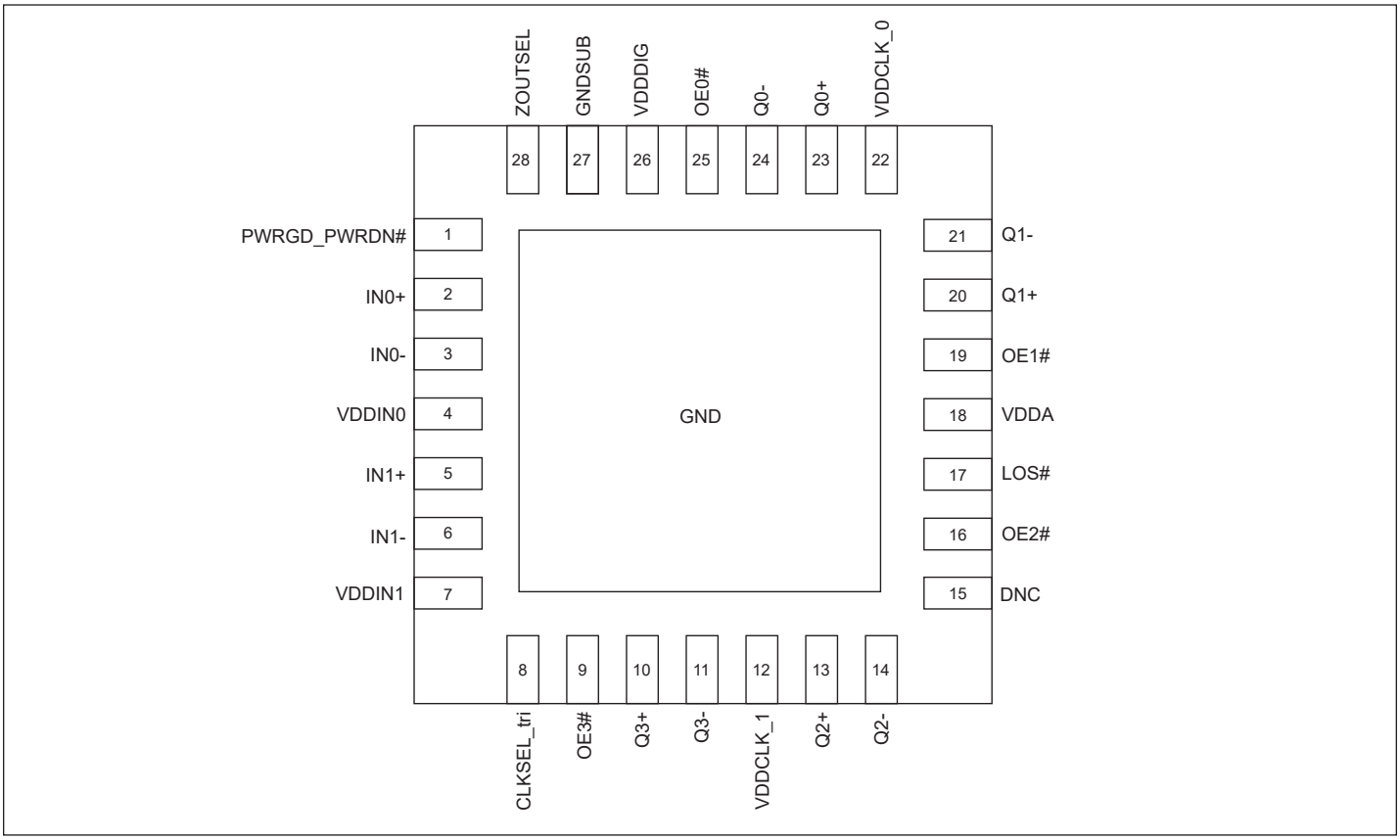
Features

- 2-Input Mux with 2/4 Low-Power HCSL Outputs Supporting On-Chip Termination
- 85Ω or 100Ω Pin Selectable Output Impedance
- Spread Spectrum Tolerant
- Individual Output Enable
- Power Down Tolerant Inputs
- Flexible Power Supply Startup Sequencing
- Automatic Output Clock Locking Upon Loss of Input Clock
- Additive Phase Jitter
  - PCIe 5.0: Typical 6fs RMS
  - PCIe 6.0: Typical 4fs RMS
  - DB2000QL: Typical 10fs RMS
- 3.3V Supply Voltage
- Packaging (Pb-free & Green):
  - 28-pin, 4mm x 4mm, VQFN (ZLF) (4 Outputs)
  - 20-pin, 3mm x 3mm, WQFN (ZNA) (2 Outputs)
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.
  https://www.diodes.com/quality/product-definitions/

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

PI6CB332204 Pin Configuration

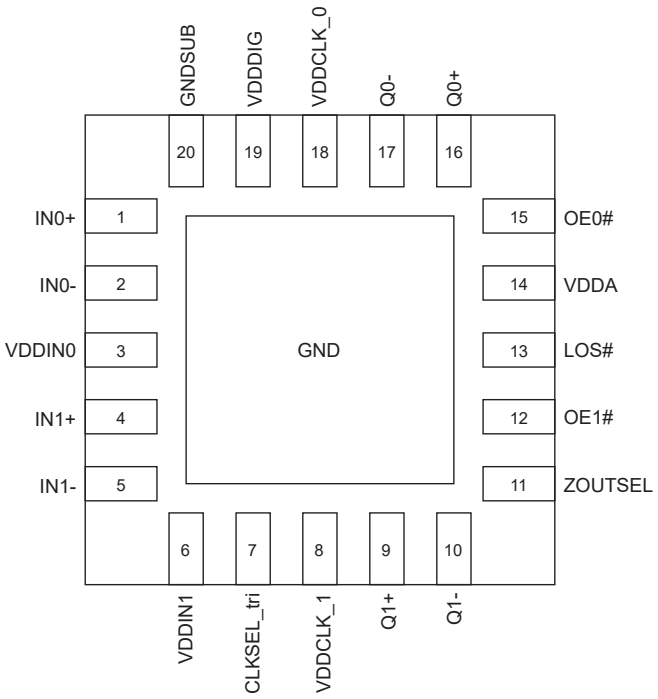


PI6CB332204 Pin Description

Pin Number	Pin Name	Type		Description
1	PWRGD_PWRDN#	Input	CMOS	Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode. Internal pull up, PDT.
2	IN0+	Input	Diff.	True clock input. Internal pull down 50KΩ.
3	IN0-	Input	Diff.	Complementary clock input. Internal pull up 50KΩ.
4	VDDIN0	Power		Power supply for clock input 0.
5	IN1+	Input	Diff.	True clock input. Internal pull down 50KΩ.
6	IN1-	Input	Diff.	Complementary clock input. Internal pull up 50KΩ.
7	VDDIN1	Power		Power supply for clock input 1.
8	CLKSEL_tri	Input	CMOS	Input to select differential input clock 0 or differential input clock 1. This input has an internal pull-up and pull-down resistor to bias a floating pin to the mid-point. 0 = IN0 selected for all outputs. 1 = IN1 selected for all outputs. M = IN0 goes to bank 0 and IN1 goes to bank 1.

Pin Number	Pin Name	Type		Description
9	OE3#	Input	CMOS	Active low input for enabling output 3. 0 = enable output, 1 = disable output. Internal pull up, PDT.
10	Q3+	Output	Diff.	True clock output.
11	Q3-	Output	Diff.	Complementary clock output.
12	VDDCLK_1	Power		Power supply for clock output bank 1.
13	Q2+	Output	Diff.	True clock output.
14	Q2-	Output	Diff.	Complementary clock output.
15	DNC			Do not connect.
16	OE2#	Input	CMOS	Active low input for enabling output 2. 0 = enable output, 1 = disable output. Internal pull up, PDT.
17	LOS#	Output	Open Drain	Output indicating Loss of Input Signal. This pin is an open drain output and requires an external pull up resistor for proper functionality. A low output on this pin indicates a loss of signal on the input clock. PDT
18	VDDA	Power		Power supply for analog circuitry.
19	OE1#	Input	CMOS	Active low input for enabling output 1. 0 = enable output, 1 = disable output. Internal pull up, PDT.
20	Q1+	Output	Diff.	True clock output.
21	Q1-	Output	Diff.	Complementary clock output.
22	VDDCLK_0	Power		Power supply for clock output bank 0.
23	Q0+	Output	Diff.	True clock output.
24	Q0-	Output	Diff.	Complementary clock output.
25	OE0#	Input	CMOS	Active low input for enabling output 0. 0 = enable output, 1 = disable output. Internal pull up, PDT.
26	VDDDIG	Power		Digital power.
27	GNDSUB	GND		Ground pin for substrate.
28	ZOUTSEL	Input	CMOS	Input to select differential output impedance. 0 = 85Ω, 1 = 100Ω. PDT. Internal pull down.
EPAD	GND	Power		Connect epad to ground.

PI6CB332202 Pin Configuration



PI6CB332202 Pin Description

Pin Number	Pin Name	Type		Description
1	IN0+	Input	Diff.	True clock input. Internal pull down 50kΩ.
2	IN0-	Input	Diff.	Complementary clock input. Internal pull up 50kΩ.
3	VDDIN0	Power		Power supply for clock input 0.
4	IN1+	Input	Diff.	True clock input. Internal pull down 50kΩ.
5	IN1-	Input	Diff.	Complementary clock input. Internal pull up 50kΩ.
6	VDDIN1	Power		Power supply for clock input 1.
7	CLKSEL_tri	Input	CMOS	Input to select differential input clock 0 or differential input clock 1. This input has an internal pull-up and pull-down resistor to bias a floating pin to the mid-point. 0 = IN0 selected for all outputs. 1 = IN1 selected for all outputs. M = IN0 goes to bank 0 and IN1 goes to bank 1.
8	VDDCLK_1	Power		Power supply for clock output bank 1.
9	Q1+	Output	Diff.	True clock output.
10	Q1-	Output	Diff.	Complementary clock output.
11	ZOUTSEL	Input	CMOS	Input to select differential output impedance. 0 = 85Ω, 1 = 100Ω. PDT. Internal pull down.

Pin Number	Pin Name	Type		Description
12	OE1#	Input	CMOS	Active low input for enabling output 1. 0 = enable output, 1 = disable output. Internal pull up, PDT.
13	LOS#	Output	Open Drain	Output indicating Loss of Input Signal. This pin is an open drain output and requires an external pull up resistor for proper functionality. A low output on this pin indicates a loss of signal on the input clock. PDT
14	VDDA	Power		Power supply for analog circuitry.
15	OE0#	Input	CMOS	Active low input for enabling output 0 0 = enable output, 1 = disable output. Internal pull up, PDT.
16	Q0+	Output	Diff.	True clock output.
17	Q0-	Output	Diff.	Complementary clock output.
18	VDDCLK_0	Power		Power supply for clock output 0.
19	VDDDIG	Power		Digital power.
20	GNDSUB	GND		Ground pin for substrate.
EPAD	GND	Power		Connect epad to ground.

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature..... –65°C to +150°C
Supply Voltage to Ground Potential, V_{DDxx}..... –0.5V to +3.9V
Input Voltage .....-0.5V to V_{DD} +0.3V, not exceed 3.9V
Input Voltage (PDT pin).....-0.5V to +3.9V
ESD Protection (HBM) 2000V
Junction Temperature ..... 150 °C Max.

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Conditions

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
V_{DDINx}, V_{DDA}	Power Supply Voltage		2.97	3.3	3.63	V
V_{DDCLK_x}	Output power supply voltage		2.97	3.3	3.63	V
I_{DD}	Power Supply Current	V_{DDINx} + V_{DDCLKx}, All outputs active @ 100MHz (PI6CB332202)		46	55	mA
		V_{DDINx} + V_{DDCLKx}, All outputs active @ 100MHz (PI6CB332204)		58	67	
I_{DD_PD}	Power Supply Power Down(1) Current	V_{DDINx} + V_{DDCLKx}, All outputs LOW/LOW		6	7.5	mA
I_{DDO_PD}	Power Supply Current Power Down(1) for Outputs	V_{DDCLKx}, All outputs LOW/LOW		3.5	4.6	mA
T_A	Ambient Temperature	Extended Industrial grade	–40		105	°C

Note:
1. Input clock is not running.
2. Outputs drive 10 inch trace.

Input Electrical Characteristics

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
R_{pu}	Internal Pull up Resistance			120		KΩ
R_{dn}	Internal Pull down Resistance			120		KΩ
L_{PIN}	Pin Inductance				7	nH

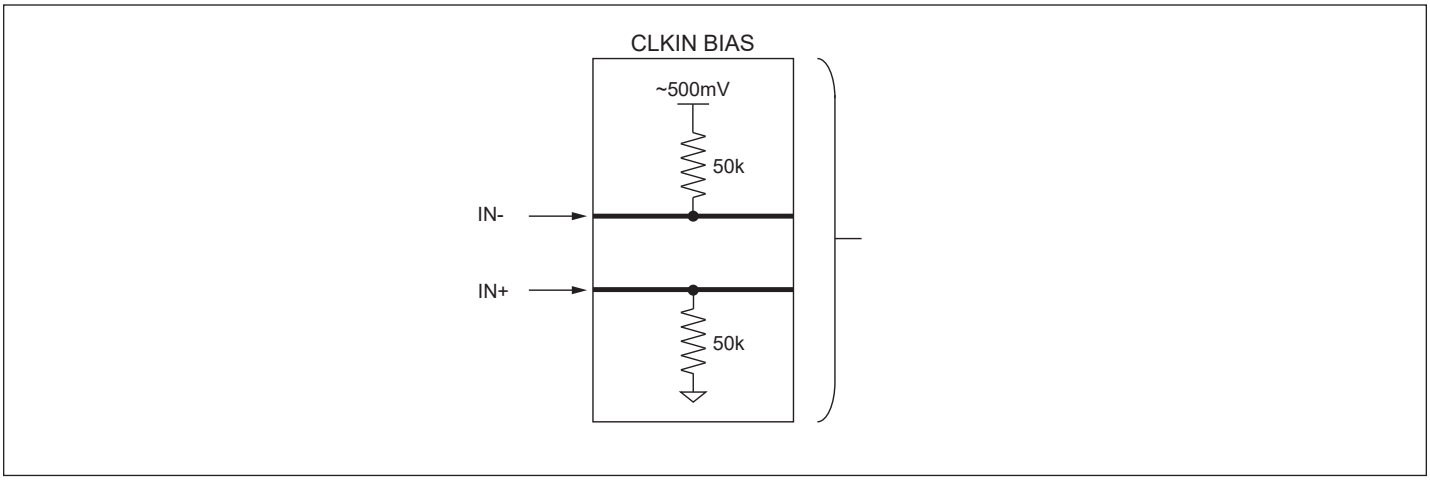


Figure 1. Input Clock Bias Network

LVCMOS DC Electrical Characteristics

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage	Single-ended inputs, except SMBus	0.75* VDD		0.3+ VDD	V
V_{IM}	Input Mid Voltage	CLKSEL_tri	0.4* VDD	0.5* VDD	0.6* VDD	V
V_{IL}	Input Low Voltage	Single-ended inputs, except SMBus	-0.3		0.25* VDD	V
I_{IH}	Input High Current	Single-ended inputs with pullup/ pulldown resistor, $V_{IN} = V_{DD}$			50	uA
		Differential clock inputs IN+/IN-, V_{IN} = VDD			100	
I_{IL}	Input Low Current	Single-ended inputs with pullup/ pulldown resistor, V_{IN} = 0V	-50			µA
		Differential clock inputs IN+/IN-, V_{IN} = 0V	-100			
C_{IN}	Input Capacitance		1.5		5	pF

HCSL Input Characteristics(1)

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
f_{IN}	Input Frequency	V_{DDINx} = 3.3V	20	100	400	MHz
V_{IHDIF}	Diff. Input High Voltage (3)	IN+, IN-, single-end measurement	330		1150	mV
V_{ILDIF}	Diff. Input Low Voltage (3)	IN+, IN-, single-end measurement	–300	0	300	mV

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
V_{COM}	Diff. Input Common Mode Voltage		100		1200	mV
V_{SWING}	Diff. Input Swing Voltage	Peak to peak value (V_{IHDIF} - V_{ILDIF})	200			mV
t_{RF}	Diff. Input Slew Rate (2)	Measured differentially	0.6			V/ns
I_{IN}	Diff. Input Leakage Current	$V_{IN+} = V_{DD}$, $V_{IN-} = 0.8V$	–40		100	uA
t_{DC}	Diff. Input Duty Cycle	Measured differentially	45		55	%
tj_{c-c}	Diff. Input Cycle to cycle jitter	Measured differentially			125	ps

Note:

1. Guaranteed by design and characterization, not 100% tested in production
2. Slew rate measured through +/-75mV window centered around differential zero
3. The device can be driven by a single-ended clock by driving the true clock and biasing the complement clock input to the Vbias, where Vbias is (V_{IH}-V_{IL})/2

HCSL Output DC Characteristics

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Condition	Min.	Typ.	Max.	Units
V_{OH}	Output Voltage High		660	780	900	mV
V_{OL}	Output Voltage Low		–150	20	150	mV
Vcross absolute	Absolute Crossing Point Voltage	Measurement on single ended signal using absolute value	250		550	mV
V_{cross_var}	Crossing Point Voltage Variation				140	mV

HCSL Output AC Characteristics

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Condition	Min.	Typ.	Max.	Units
f_{OUT}	Output Frequency			100	400	MHz
t_{RF}	Rise Time and Fall Time		1.5		4.0	V/ns
Dt_{RF}	Slew Rate Matching	Scope averaging on			20	%
t_{SKEW}	Output Skew	Averaging on, V_T = 50%			50	ps
T_{PDELAY}	Propagation Delay			2000	3000	ps
t_{DC}	Duty Cycle		45	50	55	%
T_{OELAT}	Output Enable Latency		4	5	10	clocks
T_{PDLAT}	PD# De-assertion			200	300	µs
$T_{LOSAssert}$	LOS Assert Time			200	300	ns
$T_{LOSDeassert}$	LOS De-assert Time			6	9	clocks

HCSL Output AC Characteristics - Phase Jitter

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Condition	Typ.	Max.	Specification Limit	Units
$t_{jphPCIeG1-CC}$	Additive PCIe Phase Jitter (Common Clocked Architecture) SSC ≤ -0.5%	PCIe Gen 1 (2.5 GT/s)	1300		86,000	fs p-p
$t_{jphPCIeG2-CC}$		PCIe Gen 2 Hi Band (5.0 GT/s)	58		3,100	fs RMS
		PCIe Gen 2 Lo Band (5.0 GT/s)	4		3,000	
$t_{jphPCIeG3-CC}$		PCIe Gen 3 (8.0 GT/s)	19		1,000	
$t_{jphPCIeG4-CC}$		PCIe Gen 4 (16.0 GT/s)	19		500	
$t_{jphPCIeG5-CC}$		PCIe Gen 5 (32.0 GT/s)	5	12.8	150	
$t_{jphPCIeG6-CC}$		PCIe Gen 6 (64.0 GT/s)	3	7.7	100	
$t_{jphPCIeG1-IR}$	Additive PCIe Phase Jitter (IR Architectures - SRIS, SRNS) SSC ≤ -0.3%	PCIe Gen 1 (2.5 GT/s)	111			fs RMS
$t_{jphPCIeG2-IR}$		PCIe Gen 2 (5.0 GT/s)	51			
$t_{jphPCIeG3-IR}$		PCIe Gen 3 (8.0 GT/s)	23			
$t_{jphPCIeG4-IR}$		PCIe Gen 4 (16.0 GT/s)	22			
$t_{jphPCIeG5-IR}$		PCIe Gen 5 (32.0 GT/s)	6	9.5		
$t_{jphPCIeG6-IR}$		PCIe Gen 6 (64.0 GT/s)	4	7.1		

Note: The Refclk jitter is measured after applying the filter functions found in the PCI Express Base Specification 6.0, Revision 1.0. For the exact measurements

Applications Information

Power Down Tolerant Pins

Pins that are Power Down Tolerant (PDT) can be driven by voltages as high as the normal VDD of the chip, even though VDD is not present (the device is not powered). There will be no ill effects to the device and it will power up normally. This feature supports disaggregation, where the PI6CB33220x may be on one circuit board and devices that interface with it are on other boards. These boards may power up at different times, driving pins on the PI6CB33220x before it has received power.

Flexible Startup Sequencing

PI6CB33220x devices support Flexible Startup Sequencing (FSS), IN+/- pins are PDT. FSS allows application of CLKIN at different times in the device/system startup sequence. FSS is an additional feature that helps the system designer manage the impact of disaggregation. Table shows the supported sequences; that is, the PI6CB33220x devices can have CLKIN running before VDD is applied, and can have VDD applied and sit for extended periods with no input clock.

VDD	PWRGD_PWRDNb	INx+/INx-
Not present	X	Running
		Floating
		Low/Low
Present	0 or 1	Running
		Floating
		Low/Low

Loss of Signal and Automatic Clock Parking

The PI6CB33220x Mux/buffers have a Loss of Signal (LOS) circuit to detect the presence or absence of an input clock. The LOS circuit drives the open-drain LOS# pin (the "#" suffix indicates "bar", or active-low) and sets the LOS_EVT bit in the SMBus register space. There are two slightly different LOS# pin behaviors at power up. Figure 2 below and shows the LOS# de-assertion timing

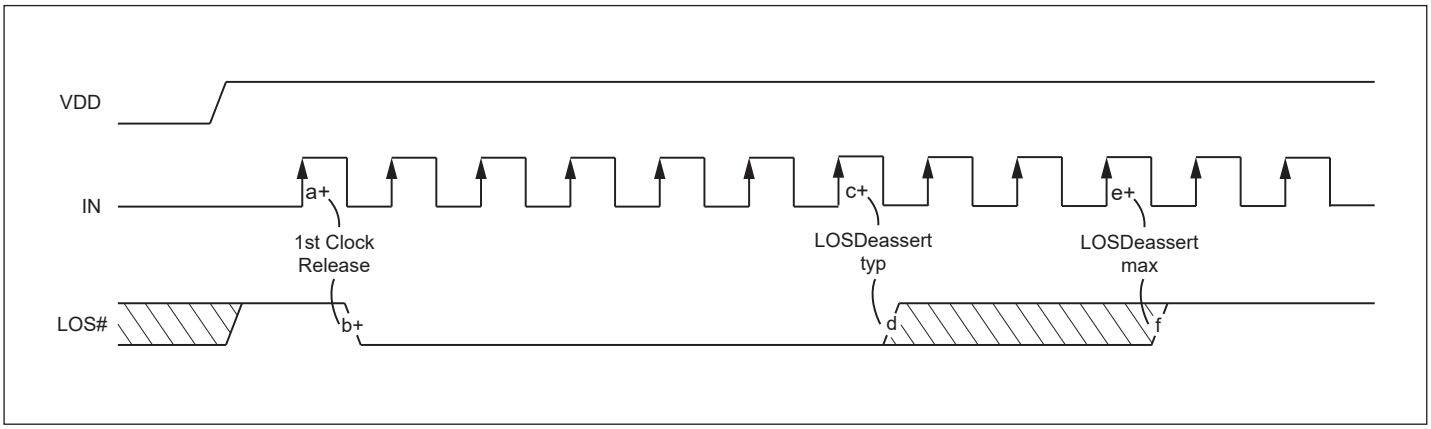


Figure 2. LOS# De-assert Timing

The following Figure 3 shows the LOS# assertion sequence when the CLKIN is lost. It also shows the Automatic Clock Parking (ACP) circuit bring the inputs to a Low/Low state after an LOS event.

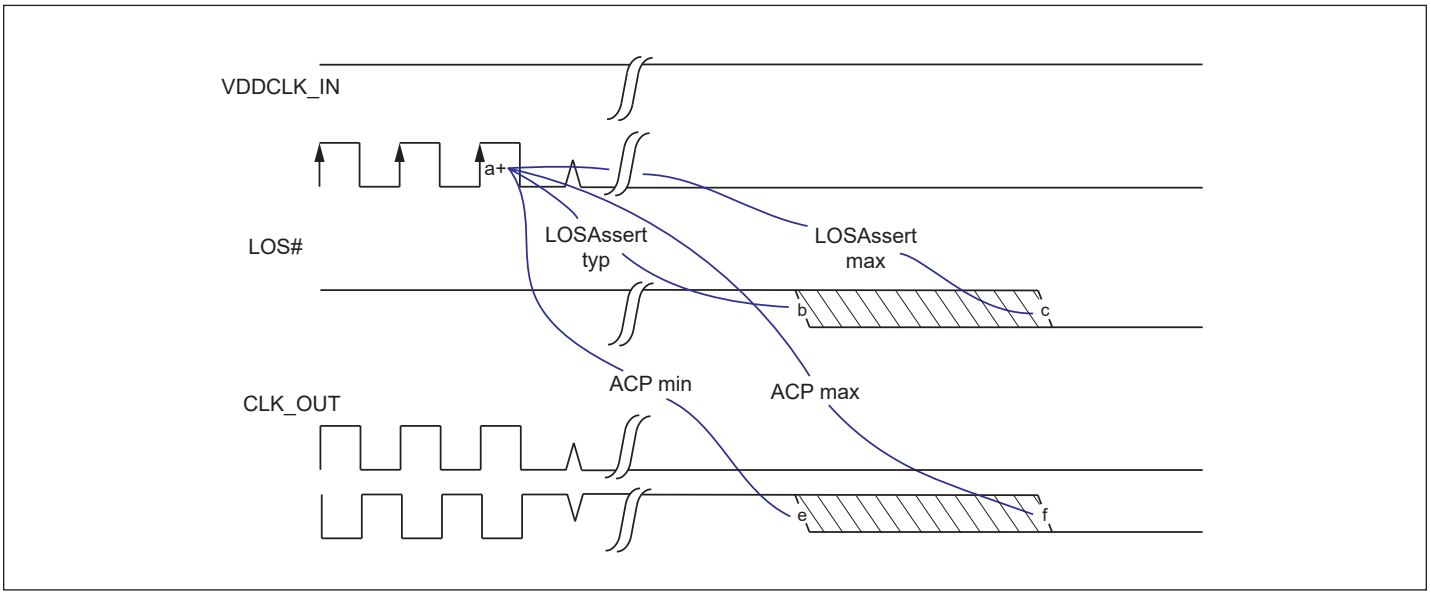


Figure 3. LOS# Assert Timing

Test Load

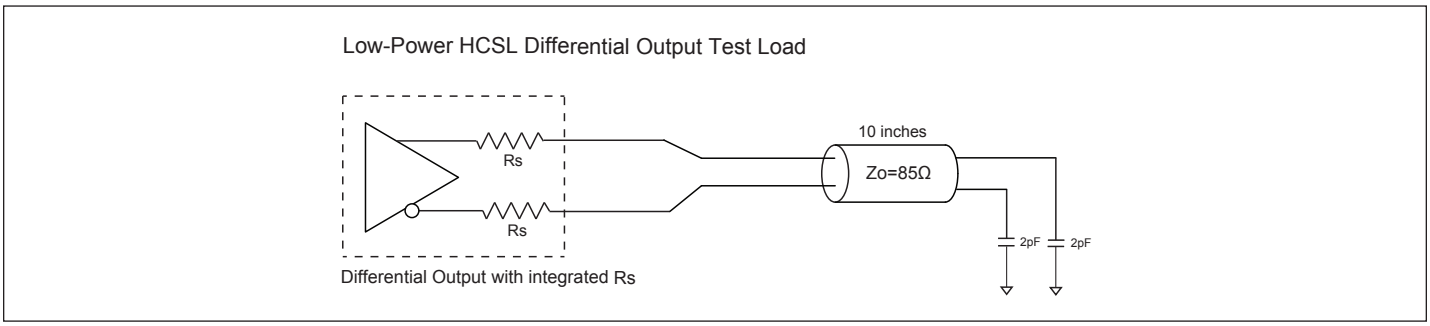


Figure 4. Low Power HCSL Test Circuit

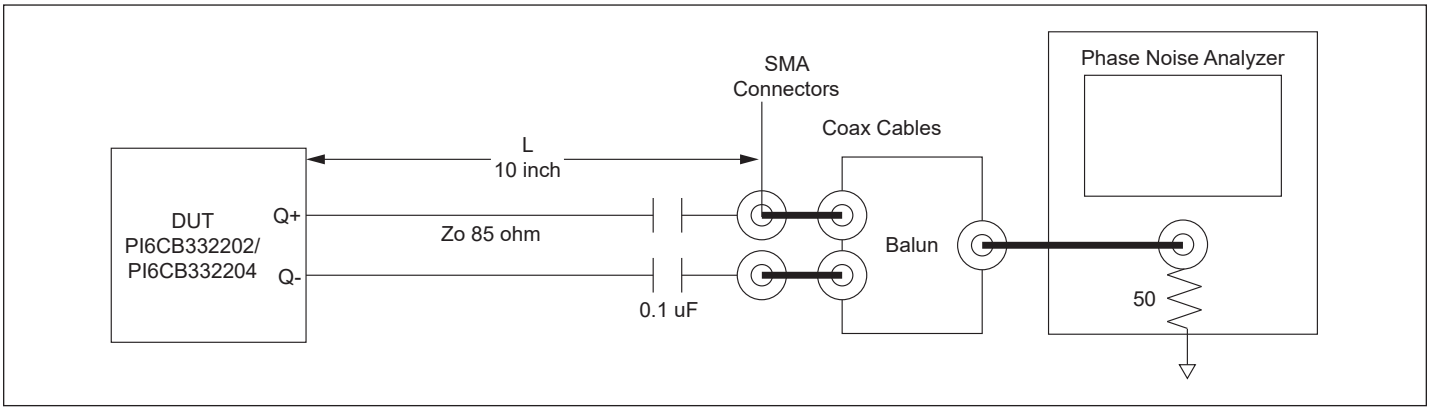


Figure 5. Test Set Up for Phase Jitter Measurement

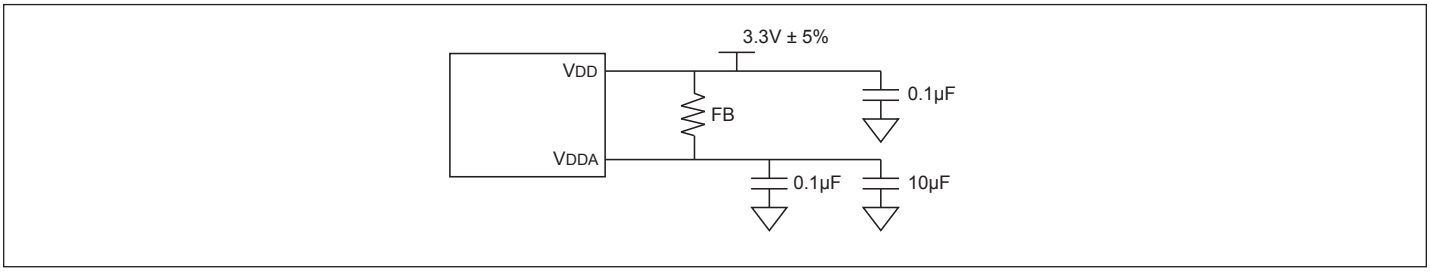


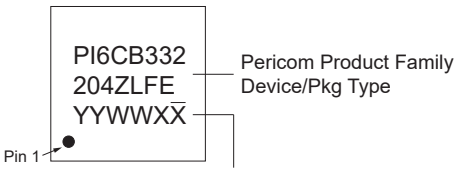
Figure 6. Power Supply Filter

Part Marking

PI6CB332202

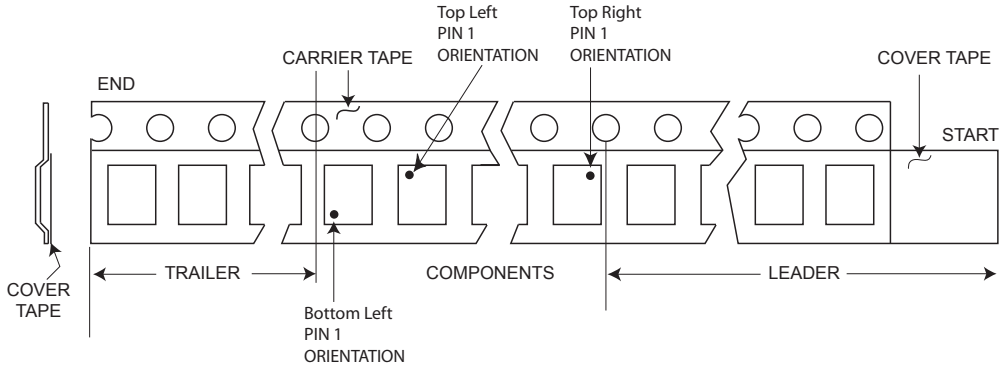
Y: Date Code (Year)
W: Date Code (Workweek)
1st X: Assembly Site Code
2nd X: Fab Site Code
Note: Date Code per MA-1251

PI6CB332204



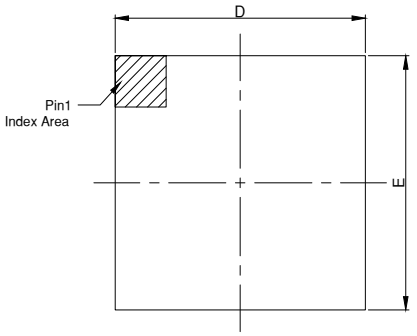
Y: Date Code (Year)
W: Date Code (Workweek)
1st X: Assembly Site Code
2nd X: Fab Site Code
Note: Date Code per MA-1251

Package Information

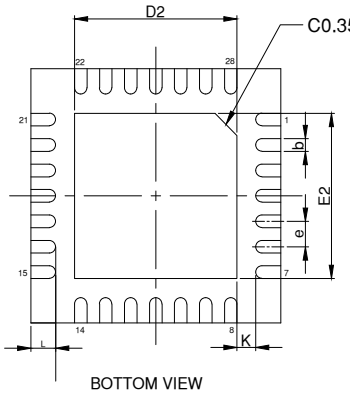


Packaging Mechanical

28-VQFN (ZLF)

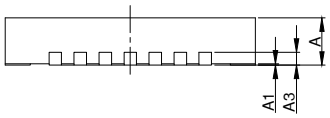


TOP VIEW

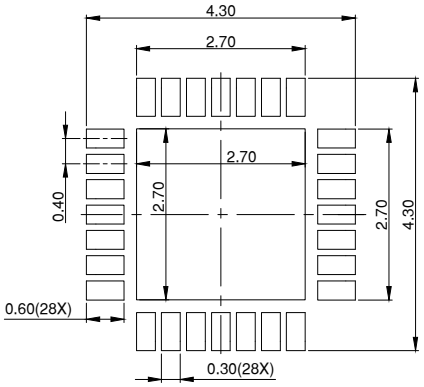


BOTTOM VIEW

PKG. DIMENSIONS(MM)			
SYMBOL	Min	NOM	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.203REF	
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.55	2.60	2.65
E2	2.55	2.60	2.65
e		0.40BSC	
L	0.30	0.40	0.50
K	0.20	--	--
b	0.15	0.20	0.25



SIDE VIEW



RECOMMENDED LAND PATTERN

Notes:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.

DATE: 05/06/24

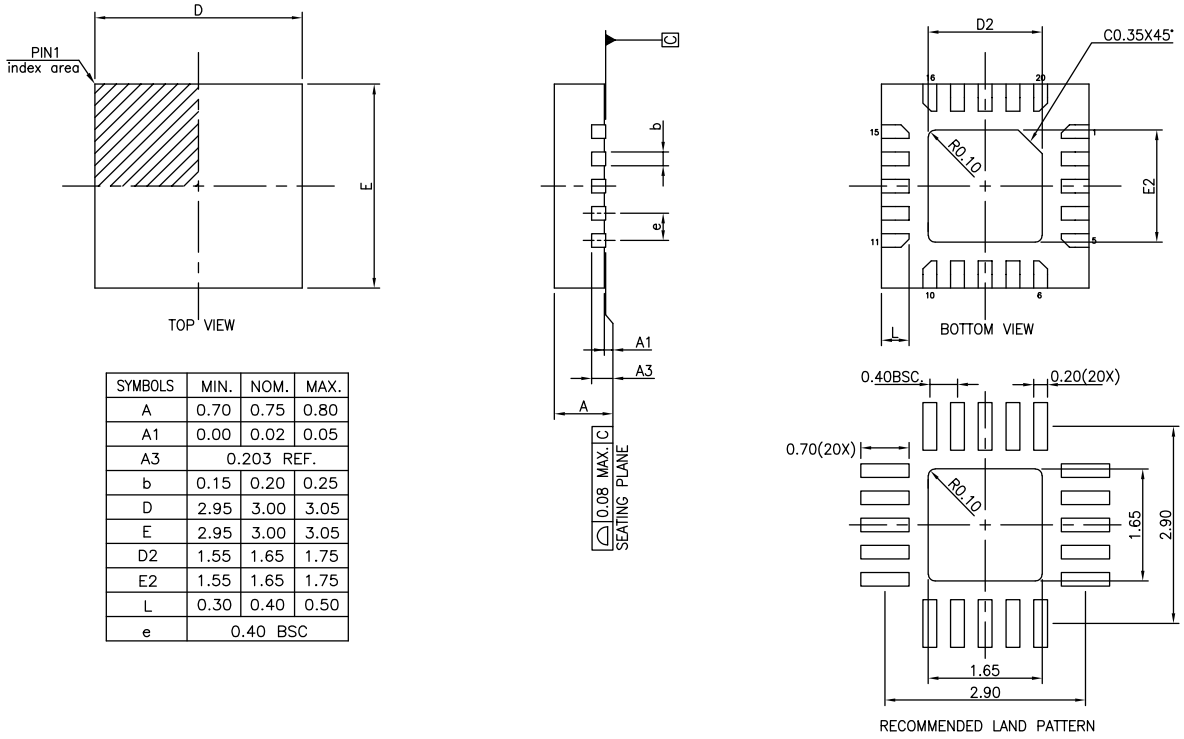
DESCRIPTION: V-QFN4040-28

PACKAGE CODE: ZLF(ZLF28)

DOCUMENT CONTROL#: PD-2292 **REVISION:--**

Packaging Mechanical

20-WQFN (ZNA)



SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF.	
b	0.15	0.20	0.25
D	2.95	3.00	3.05
E	2.95	3.00	3.05
D2	1.55	1.65	1.75
E2	1.55	1.65	1.75
L	0.30	0.40	0.50
e		0.40 BSC	

NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. REFER JEDEC MO-220
3. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.

DATE: 09/25/23

DESCRIPTION: 20 - Contact, TQFN (W-QFN3030-20)

PACKAGE CODE: ZNA (ZNA20)

DOCUMENT CONTROL #: PD-2169 REVISION: B

For latest package info.
please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

Mechanical Data

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish - Matte Sn Plated Leads. Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.02 grams (Approximate) - PI6CB332202
  0.043 grams (Approximate) - PI6CB332204

Ordering Information

Orderable Part Number	Package Code	Package Description	Pin 1 Orientation	Temperature
PI6CB332204ZLFEX	ZLF	28-Contact, V-QFN4040-28	Top Right Corner	–40~105°C
PI6CB332204ZLFEX-13R	ZLF	28-Contact, V-QFN4040-28	Top Left Corner	–40~105°C
PI6CB332202ZNAEX	ZNA	20-Contact, W-QFN3030-20	Top Right Corner	–40~105°C
PI6CB332202ZNAEX-13R	ZNA	20-Contact, W-QFN3030-20	Top Left Corner	–40~105°C

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. E = Pb-free and Green
5. X suffix = Tape/Reel
6. For packaging detail, go to our website at: https://www.diodes.com/assets/MediaList-Attachments/Diodes-Package-Information.pdf

IMPORTANT NOTICE

1. DIODES INCORPORATED (Diodes) AND ITS SUBSIDIARIES MAKE NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARDS TO ANY INFORMATION CONTAINED IN THIS DOCUMENT, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION).

2. The Information contained herein is for informational purpose only and is provided only to illustrate the operation of Diodes' products described herein and application examples. Diodes does not assume any liability arising out of the application or use of this document or any product described herein. This document is intended for skilled and technically trained engineering customers and users who design with Diodes' products. Diodes' products may be used to facilitate safety-related applications; however, in all instances customers and users are responsible for (a) selecting the appropriate Diodes products for their applications, (b) evaluating the suitability of Diodes' products for their intended applications, (c) ensuring their applications, which incorporate Diodes' products, comply the applicable legal and regulatory requirements as well as safety and functional-safety related standards, and (d) ensuring they design with appropriate safeguards (including testing, validation, quality control techniques, redundancy, malfunction prevention, and appropriate treatment for aging degradation) to minimize the risks associated with their applications.

3. Diodes assumes no liability for any application-related information, support, assistance or feedback that may be provided by Diodes from time to time. Any customer or user of this document or products described herein will assume all risks and liabilities associated with such use, and will hold Diodes and all companies whose products are represented herein or on Diodes' websites, harmless against all damages and liabilities.

4. Products described herein may be covered by one or more United States, international or foreign patents and pending patent applications. Product names and markings noted herein may also be covered by one or more United States, international or foreign trademarks and trademark applications. Diodes does not convey any license under any of its intellectual property rights or the rights of any third parties (including third parties whose products and services may be described in this document or on Diodes' website) under this document.

5. Diodes' products are provided subject to Diodes' Standard Terms and Conditions of Sale (https://www.diodes.com/about/company/terms-and-conditions/terms-and-conditions-of-sales/) or other applicable terms. This document does not alter or expand the applicable warranties provided by Diodes. Diodes does not warrant or accept any liability whatsoever in respect of any products purchased through unauthorized sales channel.

6. Diodes' products and technology may not be used for or incorporated into any products or systems whose manufacture, use or sale is prohibited under any applicable laws and regulations. Should customers or users use Diodes' products in contravention of any applicable laws or regulations, or for any unintended or unauthorized application, customers and users will (a) be solely responsible for any damages, losses or penalties arising in connection therewith or as a result thereof, and (b) indemnify and hold Diodes and its representatives and agents harmless against any and all claims, damages, expenses, and attorney fees arising out of, directly or indirectly, any claim relating to any noncompliance with the applicable laws and regulations, as well as any unintended or unauthorized application.

7. While efforts have been made to ensure the information contained in this document is accurate, complete and current, it may contain technical inaccuracies, omissions and typographical errors. Diodes does not warrant that information contained in this document is error-free and Diodes is under no obligation to update or otherwise correct this information. Notwithstanding the foregoing, Diodes reserves the right to make modifications, enhancements, improvements, corrections or other changes without further notice to this document and any product described herein. This document is written in English but may be translated into multiple languages for reference. Only the English version of this document is the final and determinative format released by Diodes.

8. Any unauthorized copying, modification, distribution, transmission, display or other use of this document (or any portion hereof) is prohibited. Diodes assumes no responsibility for any losses incurred by the customers or users or any third parties arising from any such unauthorized use.

9. This Notice may be periodically updated with the most recent version available at https://www.diodes.com/about/company/terms-and-conditions/important-notice

www.diodes.com