

PI3PCIE3242A

3.3V PCI Express® 3.0 4 Channel 2x2 Exchange Switch

Features

- 4 Differential Channel 2x2 Exchange Switch
- PCI Express® 3.0 performance, 8.0 Gbps
- Bi-directional operation
- Low Bit-to-Bit Skew: 10ps (between ± signals)
- Low Crosstalk: -29dB @ 2.5GHz (5Gbps)
-20dB @ 4.0GHz (8Gbps)
- Low Insertion Loss: -1.1dB @ 2.5GHz (5Gbps)
-1.45dB @ 4.0GHz (8Gbps)
- V_{DD} Operating Range: 3.3V ±10%
- Industrial Temperature Range: -40°C to 85°C
- ESD Tolerance: 2kV HBM
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. “Green” Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please [contact us](mailto:contact@diodes.com) or your local Diodes representative.
<https://www.diodes.com/quality/product-definitions/>
- Packaging (Pb-free & Green):
 - 30-contact, TQFN (ZL30), 2.5 x 4.5mm.

Description

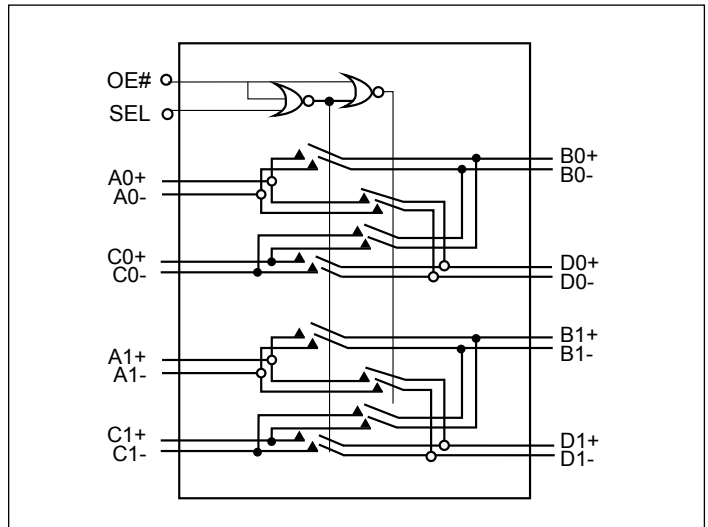
The PI3PCIE3242A is a differential exchange switch featuring pass-through pinout. It supports one full PCI Express® lane 2x2 Exchange Switch operating at 8.0Gbps PCIe® 3.0 performance.

With the select control input low, Port A connects to Port B, and Port C connects to port D for an 8-channel differential pass-through. When the select control input is high Port A connects to Port D, and Port B connects to Port C.

Truth Table

Function	SEL	OE#
Ax = Bx Cx = Dx	0	0
Ax = Dx Cx = Bx	1	0
Ax, Bx, Cx, Dx = Hi-Z (disconnect)	x	1

Block Diagram

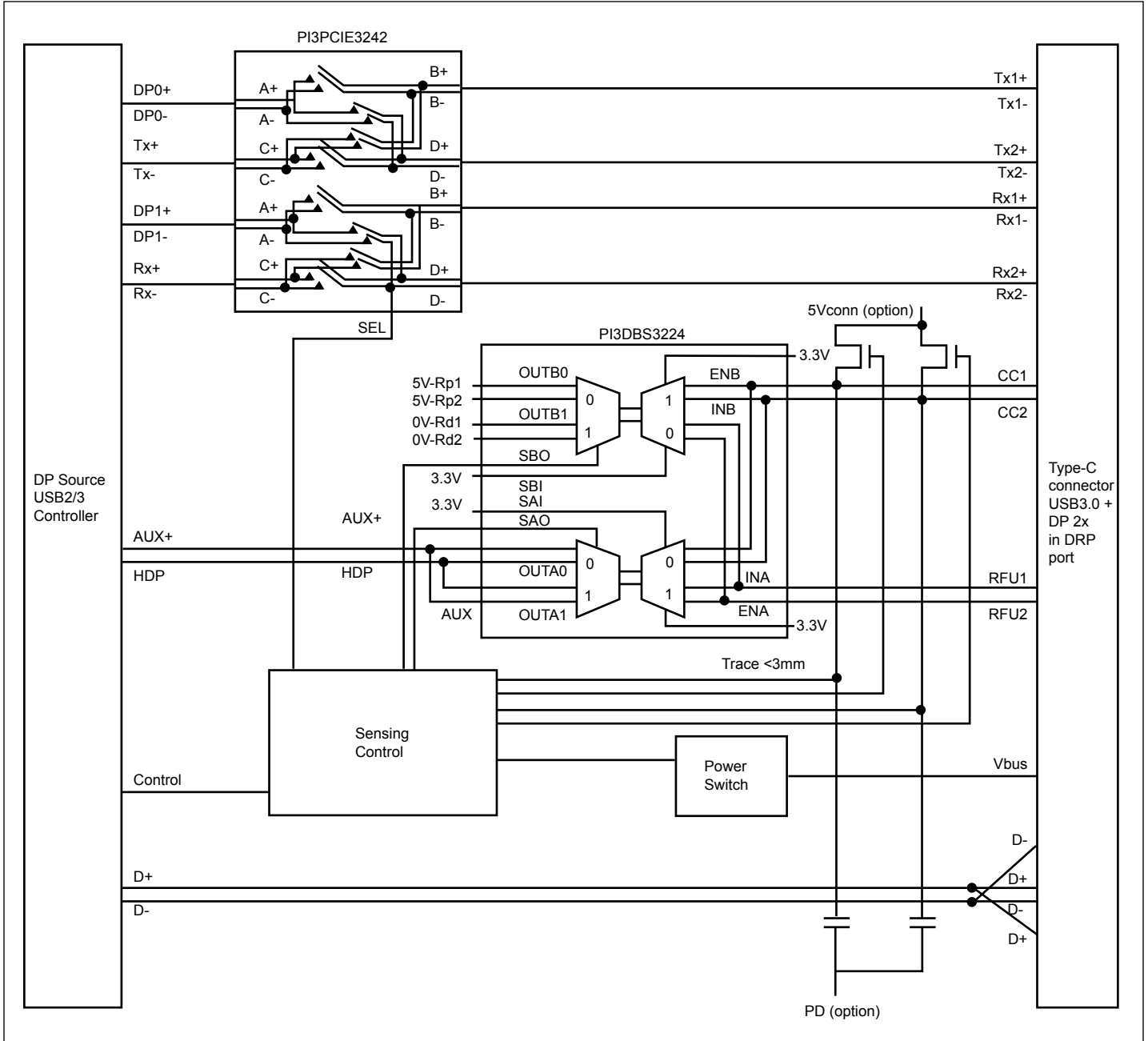


Notes:

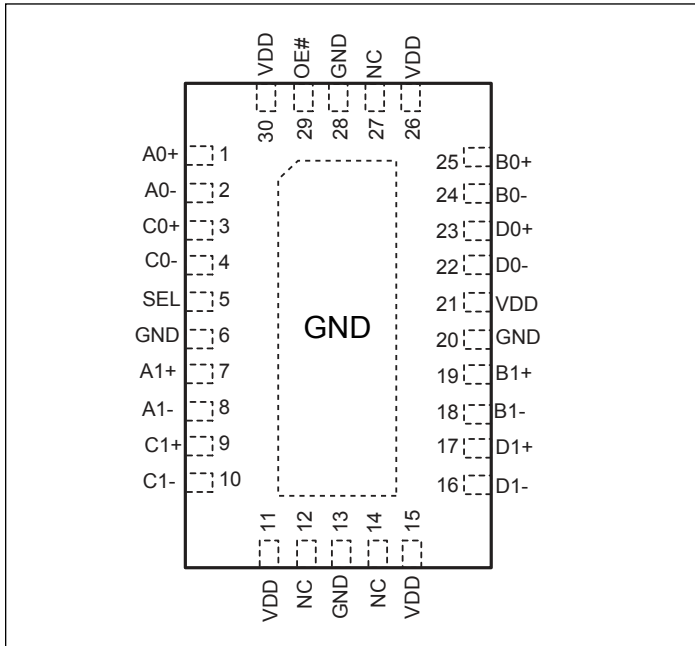
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated’s definitions of Halogen- and Antimony-free, “Green” and Lead-free.
3. Halogen- and Antimony-free “Green” products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

PI3PCIE3242A

**Application Diagram in Switching 2 Lanes of DP1.2 & USB 3.0 Signals Over Type C Connector
Notebook or Tablet**



Pin Diagram



Pin Description

Pin #	Pin Name	I/O	Description
1, 2	A0+, A0-	I/O	Signal I/O, Channel 0, Port A
7, 8	A1+, A1-	I/O	Signal I/O, Channel 1, Port A
25, 24	B0+, B0-	I/O	Signal I/O, Channel 0, Port B
19, 18	B1+, B1-	I/O	Signal I/O, Channel 1, Port B
3, 4	C0+, C0-	I/O	Signal I/O, Channel 0, Port C
9, 10	C1+, C1-	I/O	Signal I/O, Channel 1, Port C
23, 22	D0+, D0-	I/O	Signal I/O, Channel 0, Port D
17, 16	D1+, D1-	I/O	Signal I/O, Channel 1, Port D
29	OE#	I	Output Enable, active low. When OE# = 0 the device I/O is enabled. When OE#=1, all I/O are high impedance
5	SEL	I	Operation mode Select (when SEL=0: A→B, C→D, when SEL=1: A→D, C→B)
11, 15, 21, 26, 30	V _{DD}	Pwr	3.3V ±10% Positive Supply Voltage
6, 13, 20, 28, Center Pad	GND	Pwr	Power ground
12, 14, 27	NC		No Connect

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Supply Voltage to Ground Potential	-0.5V to +3.7V
DC Input Voltage	-0.5V to V _{DD}
DC Output Current	120mA
Power Dissipation	0.5W
Junction Temperature	125°C

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics Recommended Operating Conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V _{DD}	3.3V Power Supply		3.0	3.3	3.6	V
I _{DD}	Total current from V _{DD} 3.3V supply	SEL and OE# at OV or V _{DD}			200	μA
T _A	Operating temperature range		-40		85	°C

DC Electrical Characteristics for Switching over Operating Range

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ. ⁽¹⁾	Max.	Units
V _{IH}	Input HIGH Voltage	Guaranteed HIGH level	0.65 x V _{DD}			V
V _{IL}	Input LOW Voltage	Guaranteed LOW level	-0.5		0.35 x V _{DD}	
V _{IK}	Clamp Diode Voltage	V _{DD} = Max., I _{IN} = -18mA		-0.7	-1.2	
I _{IH}	Input HIGH Current, SEL	V _{DD} = Max., V _{IN} = V _{DD}	-10		+10	μA
I _{IL}	Input LOW Current, SEL	V _{DD} = Max., V _{IN} = GND	-10		+10	
I _{IH}	Input HIGH Current, A _X , B _X , C _X , D _X	V _{DD} = Max., V _{IN} = 1.8V	-10		+10	μA
I _{IL}	Input LOW Current, A _X , B _X , C _X , D _X	V _{DD} = Max., V _{IN} = 0V	-10		+10	

Note:

1. Typical values are at V_{DD} = 3.3V, T_A = 25°C ambient and maximum loading.

Switching Characteristics

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t _{PZH} , t _{PZL}	Line Enable Time - SEL to A _N , B _N , C _N , D _N		0.5		45	ns
t _{PHZ} , t _{PLZ}	Line Disable Time - SEL to A _N , B _N , C _N , D _N		0.5		25	
t _{b-b}	Bit-to-bit skew within the same differential pair				10	ps
t _{ch-ch}	Channel-to-channel skew				20	

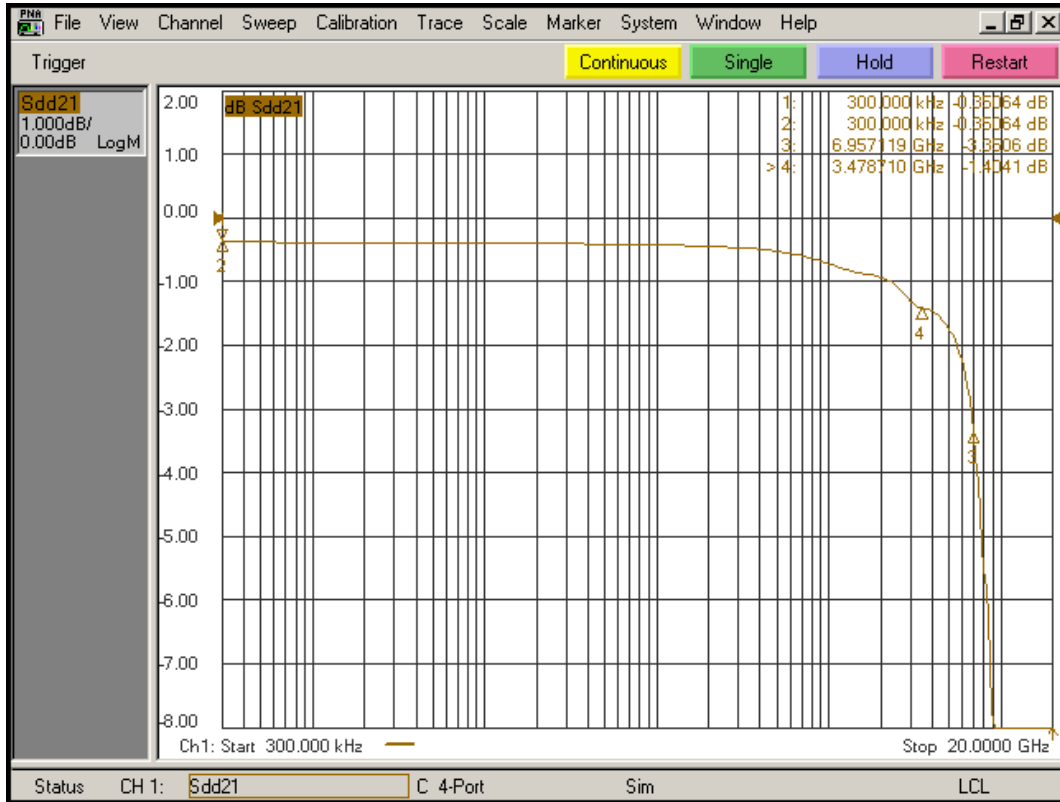
Dynamic Electrical Characteristics

Parameter	Description	Test Conditions	Min.	Typ. ⁽¹⁾	Max.	Units
DDIL	Differential Insertion Loss ($V_{IN} = -10\text{dBm}$, $DC = 0V$)	$f=1.2\text{GHz}$ $f=2.5\text{GHz}$ $f=4.0\text{GHz}$ $f=5.0\text{GHz}$ $f=7.5\text{GHz}$		-0.8 -1.0 -1.3 -1.8 -4.5	-1.0 -1.2 -1.9 -2.6 -5.6	dB
DDIL _{OFF}	Differential Off Isolation	$f= 4.0\text{GHz}$		-19		dB
DDRL	Differential Return Loss	$f= 0$ to 2.8GHz $f= 2.8$ to 5.0GHz $f= 5.0$ to 8.0GHz		-26 -14 -7.5		dB
DDNEXT	Near End Crosstalk	$f= 0$ to 2.8GHz $f= 2.8$ to 5.0GHz $f= 5.0$ to 8.0GHz		-26 -20 -16		dB
V_{IF}	Max Signal Frequency Range	Insertion loss 1.5dB, $V_{IN}=0.623\text{Vpp}$, $DC=0V$		4.0		GHz
		Insertion loss 1.5dB, $V_{IN}=0.623\text{Vpp}$, $DC=0.9V$		4.0		
		Insertion loss 3dB, $V_{IN}=0.623\text{Vpp}$, $DC=0V$		8.0		
		Insertion loss 3dB, $V_{IN}=0.623\text{Vpp}$, $DC=0.9V$		8.0		
BW	-3dB Bandwidth			6.5		GHz

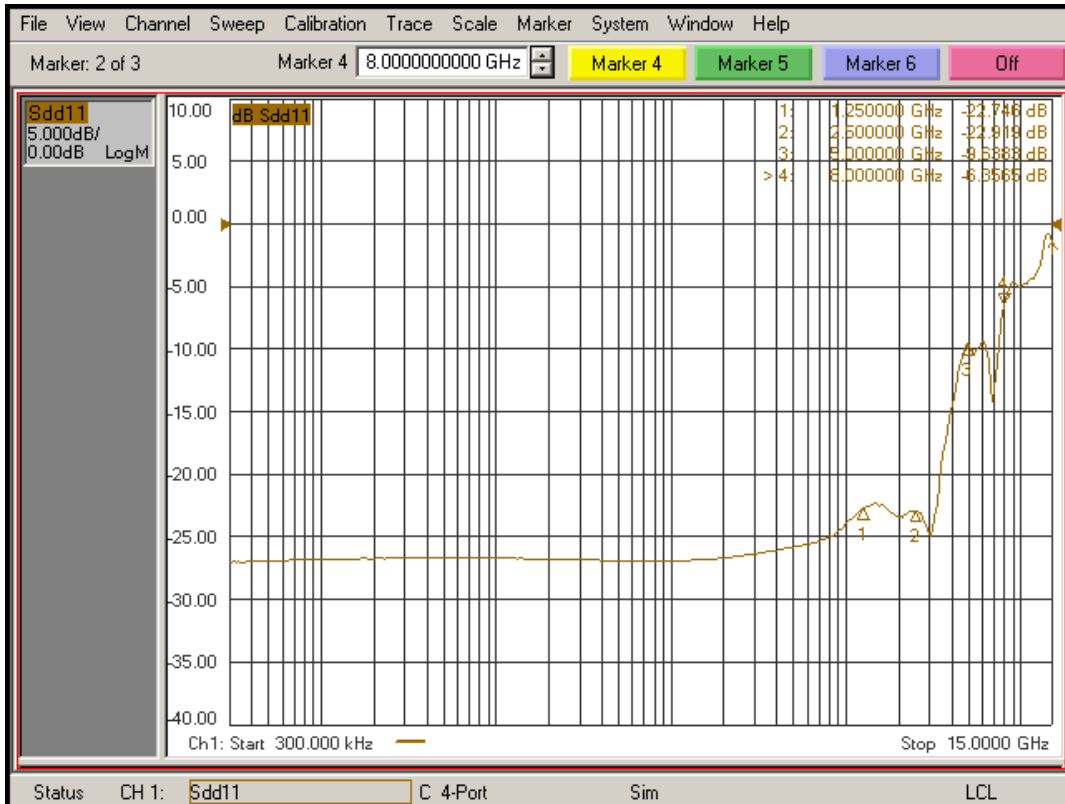
Notes:

1. Guaranteed by design. Typical values are at $V_{DD} = 3.3V$, $T_A = 25^\circ\text{C}$ ambient and maximum loading.

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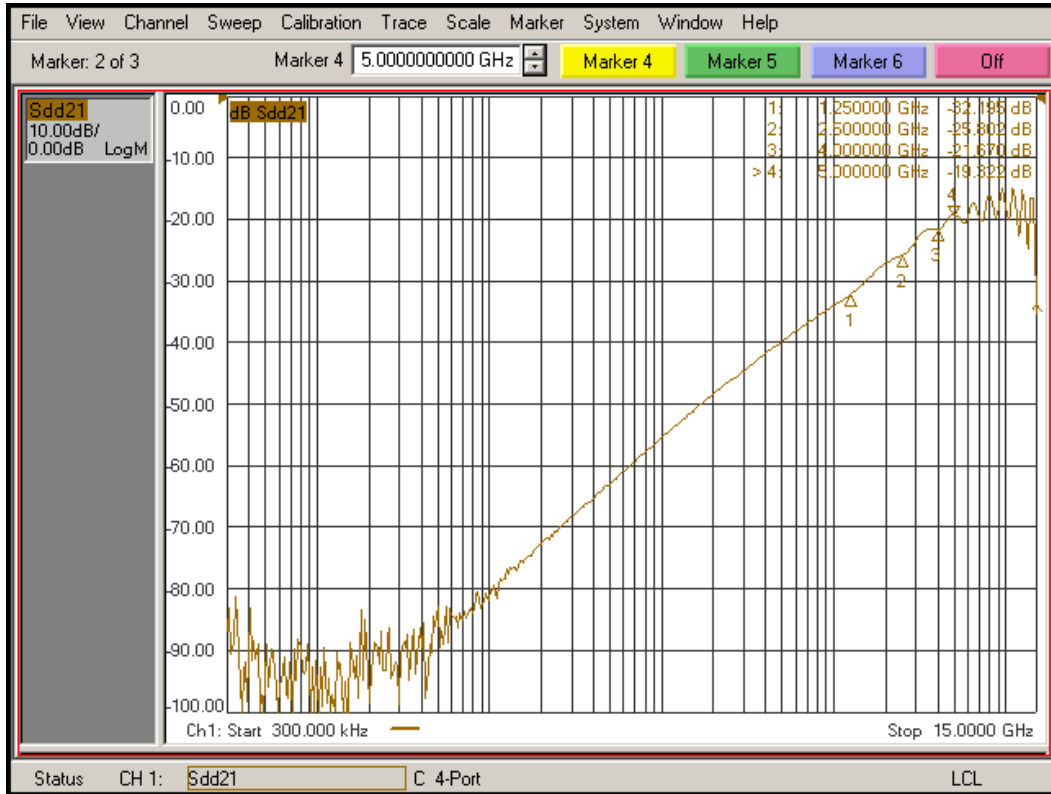


Differential Insertion Loss

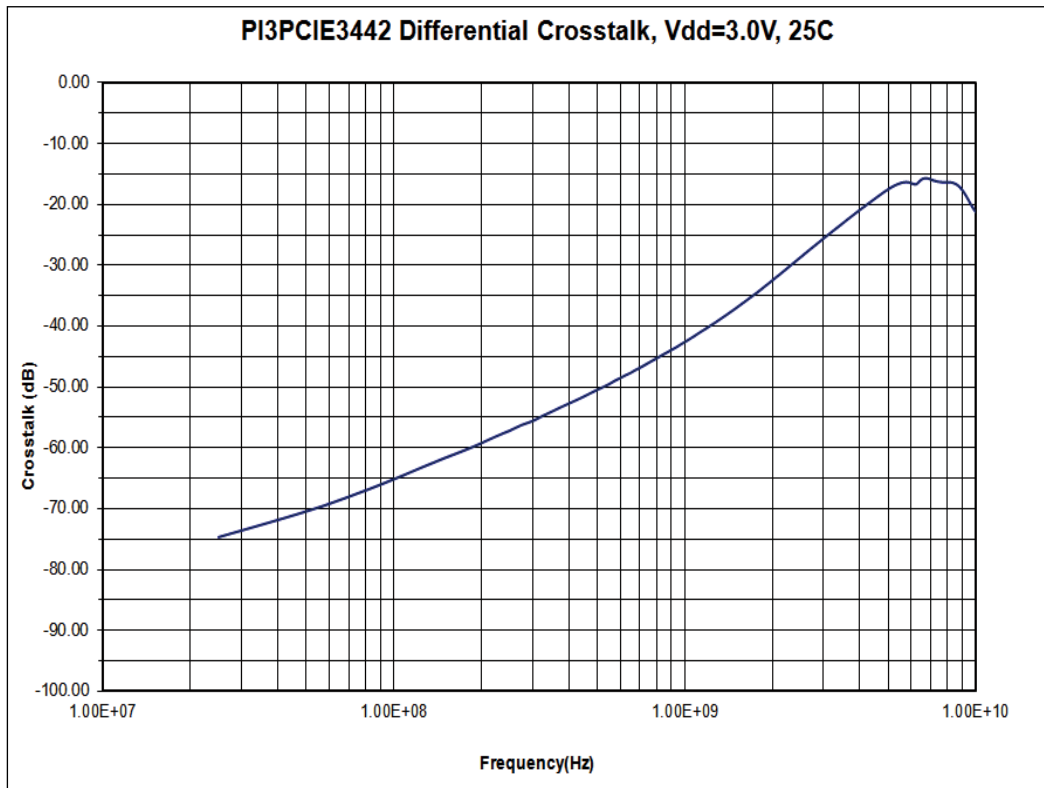


Differential Return Loss

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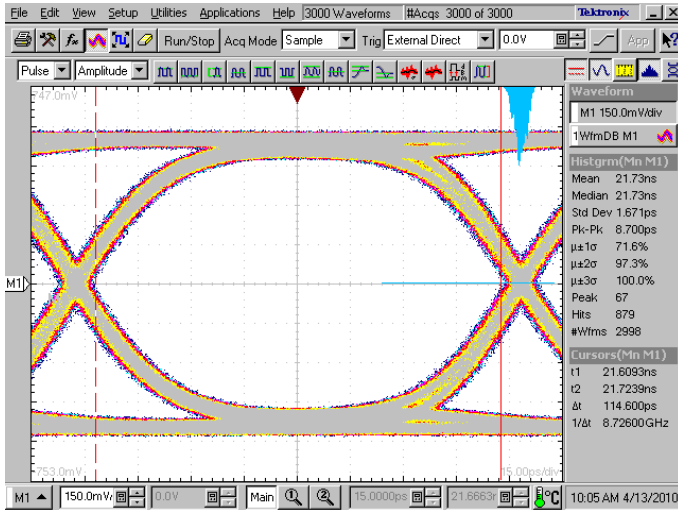


Differential Off Isolation

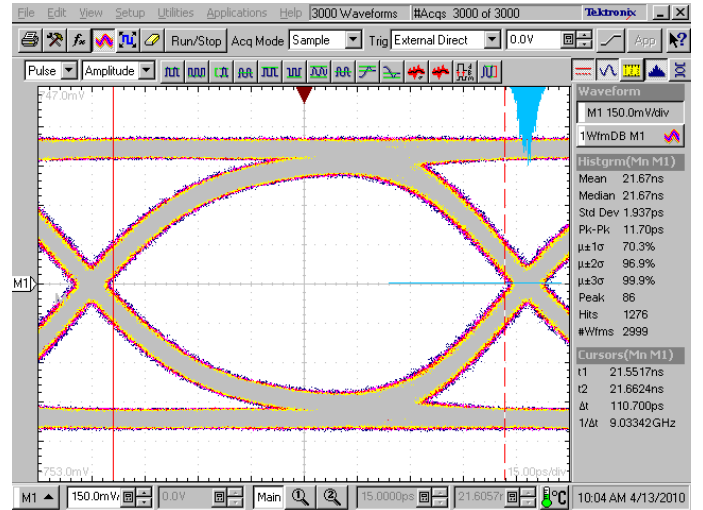


Differential Crosstalk

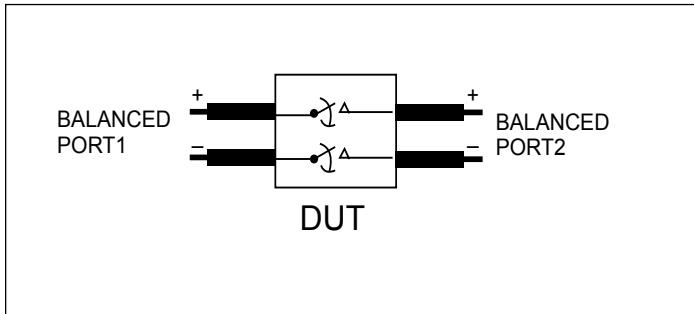
PI3PCIE3242A



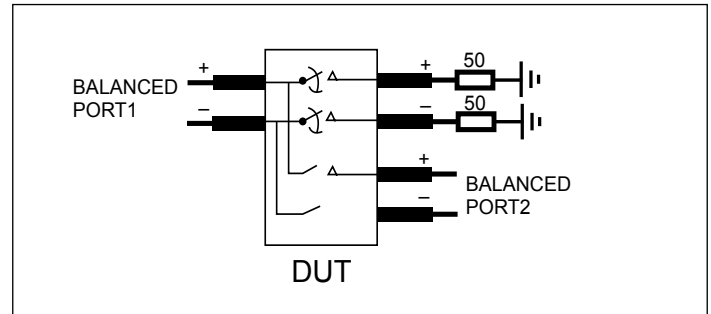
8.0 Gbps RX signal eye without PI3PCIE3242A



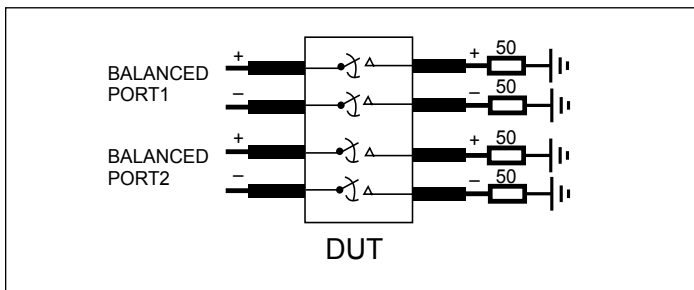
8.0 Gbps RX signal eye with PI3PCIE3242A



Differential Insertion Loss and Return Test Circuit

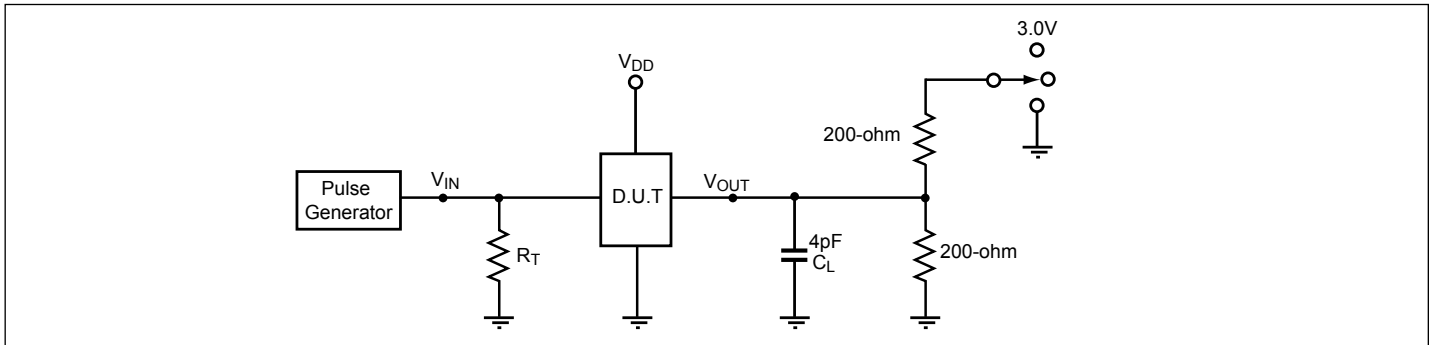


Differential Off Isolation Test Circuit



Differential Near End Xtalk Test Circuit

Test Circuit for Electrical Characteristics



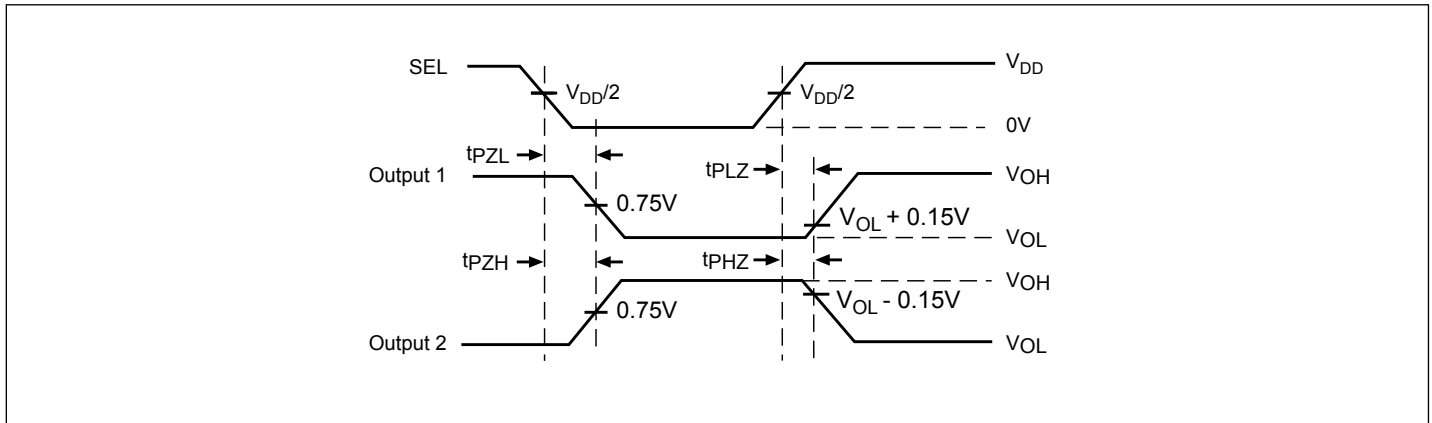
Notes:

1. C_L = Load capacitance: includes jig and probe capacitance.
2. R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator
3. Output 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Output 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
4. All input impulses are supplied by generators having the following characteristics: $PRR \leq \text{MHz}$, $Z_O = 50\Omega$, $t_R \leq 2.5\text{ns}$, $t_F \leq 2.5\text{ns}$.
5. The outputs are measured one at a time with one transition per measurement.

Switch Positions

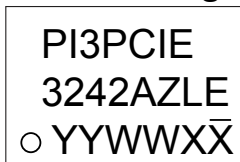
Test	Switch
t_{PLZ}, t_{PZL}	3.0V
t_{PHZ}, t_{PZH}	GND
Prop Delay	Open

Switching Waveforms



Voltage Waveforms Enable and Disable Times

Part Marking



YY : Year
 WW : Workweek
 1st X: Assembly Code
 2nd X: Fab Code

PI3PCIE3242A

Packaging Mechanical: 30-TQFN (2.5x4.5mm)

TOP VIEW

SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203	REF.	
b	0.15	0.20	0.25
D	2.40	2.50	2.60
E	4.40	4.50	4.60
D2	1.15	1.20	1.25
E2	3.15	3.20	3.25
e	0.40	BSC	
L	0.25	0.30	0.35
K	0.20	—	—

SEATING PLANE

BOTTOM VIEW

RECOMMENDED LAND PATTERN

Notes:

- All dimensions are in mm. Angles in degrees.
- Refer JEDEC MO-220.
- Recommended land pattern is for reference only.

PERICOM
Enabling Serial Connectivity

DATE: 10/21/13

DESCRIPTION: 30-contact, Thin Fine Pitch Quad Flat No lead Package (TQFN)

PACKAGE CODE: ZL

DOCUMENT CONTROL #: PD-2172 **REVISION: --**

14-0006

For latest package info.

please check: <http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/>

Ordering Information

Ordering Code	Package Code	Package Description
PI3PCIE3242AZLEX	ZL	30-contact, Thin Fine Pitch Quad Flat No-Lead (TQFN)

Notes:

- No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
- See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- E = Pb-free and Green
- X suffix = Tape/Reel

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