Not Recommended for New Design - Use PI2DPX1067

A Product Line of Diodes Incorporated

PI2DPX1066

1.8V 10Gbps USB-C DP-Alt Linear ReDriver with AUX-SBU Switch

Description

The PI2DPX1066 is a non-blocking USB Type-C® DP-Alt mode linear ReDriver™ in 4-to-4 configuration operated by 1.8v power supply. It supports four operation modes through I2C bus setting for USB3.2 Gen2, USB3.2 Gen2/2-lane DP1.4/DP2.1 (UHBR10), 4-lane DP1.4/DP2.1 (UHBR10) or USB3.2 Gen2x2 with speed up to 10Gbps per channel. It swaps the high speed channels under the flip and non-flip plug in compliance to Type-C connector with the integrated AUX crossbar switch for SBU pins.

The non-blocking linear ReDriver design ensures the differential signals conveying pre-shoot and de-emphasis equalization waveforms from transmitter side to receiver side, this can help to optimize the overall channel link adjustment conducted by the system transmitter and receiver with DFE. The CTLE equalizers are implemented at the inputs of the ReDriver to compensate the channel loss and reduce the ISI jitters. The programmable flat gain and linearity adjustments support the eye diagram opening.

The CTLE EQ gains, flat gains and linearity are individually programmable on each channel for flexible tuning via I2C register settings.

Application(s)

- Laptop PCs
- Desktop PCs
- Gaming Consoles
- VR/AR Goggles
- Active Cables

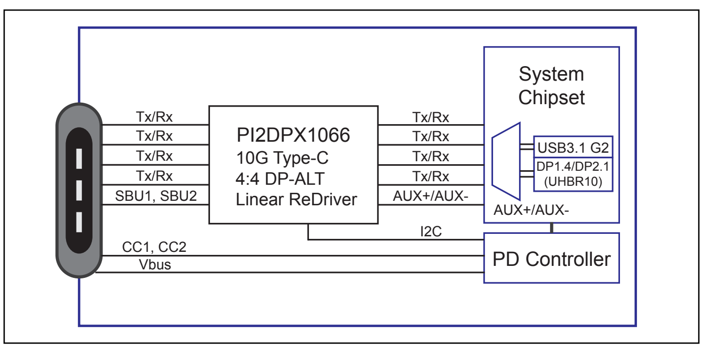

Figure 1-1 System with USB Type-C Connector Application

Features

- 4-to-4 channel configuration with 10Gbps linear ReDriver
- Configurable for USB3.2 Gen2, USB3.2 Gen2/2-lane DP1.4/DP2.1 (UHBR10), 4-lane DP1.4/DP2.1 (UHBR10) or USB3.2 Gen2x2 operations
- Default USB Type-C safe state (Hi-Z) after power-on
- Ultra low latency (<300ps) for better interoperability and data throughput
- Individual controls on CTLE gain, Flat Gain and Output linearity
- Integrated AUX channel crossbar switch for side band signal
- Type-C connector flip and non-flip plug support
- I2C Slave support with speed up to 1MHz
- Very low USB and DisplayPort active mode and power saving mode operation
- Single power supply: 1.8V +/-5%
- Industrial temperature support: -40°C to +85°C
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/
- Package: Tiny 32-pin X2QFN, 2.85 x 4.5 mm (0.4 mm pitch)

Ordering Information

Orderable Part Number	Package Code	Package Description
PI2DPX1066XUAEX	XUA	32-pin, 2.85x4.5mm (X2QFN)

Notes:
- E = Pb-free and Green
- X suffix = Tape/Reel

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

2. General Information

2.1 Revision History

Date	Revision	Description of Changes
February 2020	1	Preliminary Datasheet Release
May 2020	2	Updated Section 4.7 I2C Register Definitions Updated Section 5.3 Thermal Information Updated Section Power Consumption Updated Table 4-5 Chip Enable Control Added Section 4.6.2 Indexed Read/Write Protocol
July 2020	3	Updated all DP1.4 to DP1.4/DP2.0 (UHBR10) Updated Power and Return Loss Numbers
February 2021	4	Updated Section BYTE 3 (Channel assignment of RXDET_EN and configuration mode) Updated Section 5.2 Power Consumption Updated Ordering Information Updated Important Notice Formal Datasheet Release
April 2021	5	Updated Table DP Low Power Mode Description
September 2021	6	Updated Section 6.2 Reference Application Schematics Updated Section 5.2 Recommended Operating Conditions
October 2021	7	Updated Part Marking
November 2021	8	Updated Section 5.1 Absolute Maximum Ratings
February 2022	9	Updated Part Marking
December 2025	10	Updated All DP2.0 to DP2.1 Updated Section 3.2 Pin Description Updated Section 5.1 Absolute Maximum Rating Updated Section 4.7 I2C Register Definitions

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3. Pin Configuration

3.1 Package Pin-out

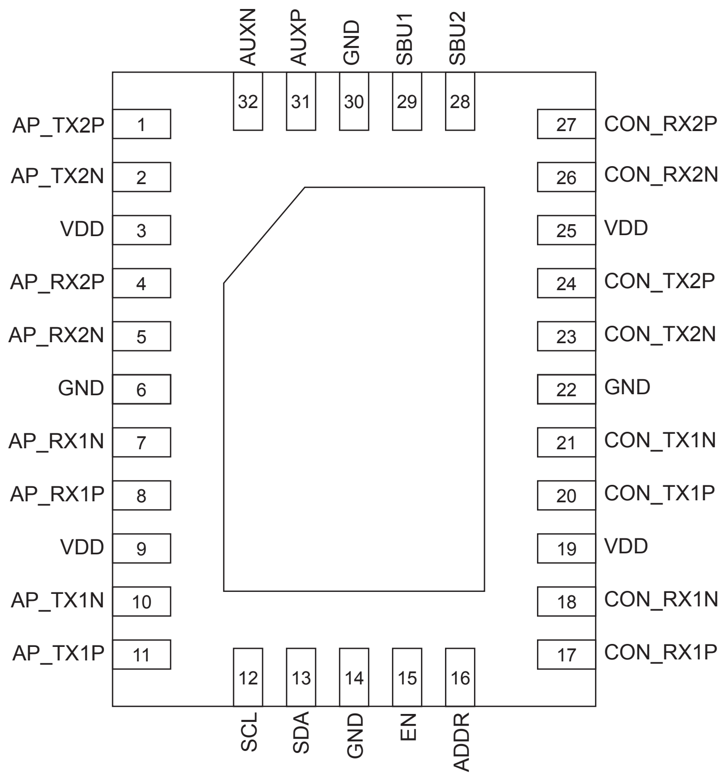


Figure 3-1 32-X2QFN Package Pin-out

3.2 Pin Description

Pin Name	Pin Number	Type	Description
Power and GND			
3, 9, 19, 25	VDD18	Power	1.8V power supply, +/- 5%
6, 14, 22, 30, Center Pad	GND	Ground	Supply Ground
Control Pins			
12	SCL	I	SCL is I2C control bus clock. Open drain structure. (3.3V tolerance)
13	SDA	I/O	SDA is I2C control data clock. Open drain structure. (3.3V tolerance)
15	EN	I	Chip Enable. With internal 300kΩ pull-up resistor. Low: Chip Power Down High: Normal Operation (Default)
16	ADDR	I	The I2C address select. 3-level input pins. With internal 150kΩ pull-up and pull-down resistors.
High Speed I/O Pins			
18, 17 27, 26	CON_RX1N, CON_RX1P CON_RX2P, CON_RX2N	I/O	Type-C receptacle RX/TX Channel CML input/output terminals. With selectable input termination between 50Ω to internal VbiasRx, 78kΩ to internal VbiasRx or 78kΩ to GND. With selectable output termination between 50Ω, 6kΩ to internal VbiasTx or Hi-Z.
21, 20 24, 23	CON_TX1N, CON_TX1P CON_TX2P, CON_TX2N	O	CML output terminals. With selectable output termination between 50Ω, 6kΩ to internal VbiasTx or Hi-Z.
1, 2 10, 11	AP_TX2P, AP_TX2N AP_TX1N, AP_TX1P	I/O	Type-C receptacle RX/TX Channel CML input/output terminals. With selectable input termination between 50Ω to VDD, 78kΩ to internal VbiasRx or 78kΩ to GND. With selectable output termination between 50Ω, 6kΩ to internal VbiasTx or Hi-Z.
4, 5 7, 8	AP_RX2P, AP_RX2N AP_RX1N, AP_RX1P	I	CML input terminals. With selectable input termination between 50Ω to internal Vbias-Rx, 78kΩ to internal VbiasRx or 78kΩ to GND.
Side Band Signal Pins			
28, 29	SBU2, SBU1	I/O	Type-C connector SBU signal connections
31, 32	AUXP, AUXN	I/O	DisplayPort AUX CH differential signal connections

4. Functional Description

4.1 Functional Block Diagram

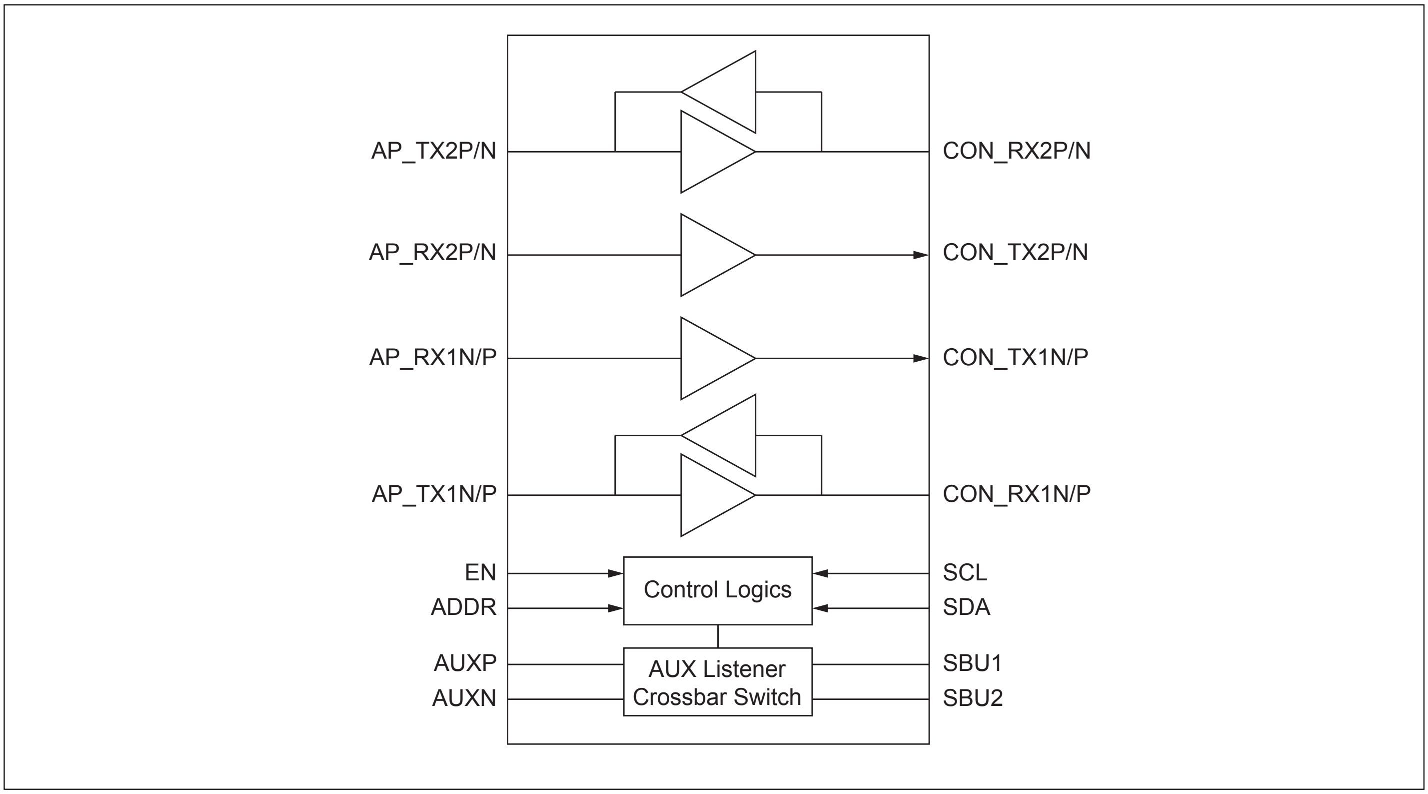


Figure 4-1 PI2DPX1066 Block Diagram

4.2 Operating Modes

4.2.1 Configuration Table

Byte 3 Bit [7:4]	AP_TX2	AP_RX2	AP_RX1	AP_TX1	AUXP	AUXN	Modes
0000	X	X	X	X	X	X	Safe State (Hi-Z)
0001	X	X	X	X	X	X	Safe State (Hi-Z)
0010	CON_RX2 (DP0)	CON_TX2 (DP1)	CON_TX1 (DP2)	CON_RX1 (DP3)	SBU1	SBU2	4 lane DP + AUX
0011	CON_RX2 (DP3)	CON_TX2 (DP2)	CON_TX1 (DP1)	CON_RX1 (DP0)	SBU2	SBU1	4 lane DP + AUX (flipped)
0100	X	X	CON_TX1	CON_RX1	X	X	1 port USB3
0101	CON_RX2	CON_TX2	X	X	X	X	1 port USB3 (flipped)
0110	CON_RX2 (DP0)	CON_TX2 (DP1)	CON_TX1 (USB3)	CON_RX1 (USB3)	SBU1	SBU2	2 lane DP + USB3 + AUX
0111	CON_RX2 (USB3)	CON_TX2 (USB3)	CON_TX1 (DP1)	CON_RX1 (DP0)	SBU2	SBU1	2 lane DP + USB3 + AUX (flipped)
1000	CON_RX2 (USB3)	CON_TX2 (USB3)	CON_TX1 (DP1)	CON_RX1 (DP0)	SBU1	SBU2	USB3 + 2 lane DP + AUX
1001	CON_RX2 (DP0)	CON_TX2 (DP1)	CON_TX1 (USB3)	CON_RX1 (USB3)	SBU2	SBU1	USB3 + 2 lane DP +AUX (flipped)
<1010> ~ <1011>	-	-	-	-	-	-	Reserved
1100	CON_RX2	CON_TX2	CON_TX1	CON_RX1	X	X	2-port USB3 (USB3.2x2)
<1101> ~ <1111>	-	-	-	-	-	-	Reserved

Notes:
1) The high speed channels don't do any flip action. Only the AUX channel is flipped.
2) <0000> default at power on.

4.3 USB Mode

In the low power mode, the signal detector will still be monitoring the input channel. If a channel is in low power mode and the input signal is detected, the corresponding channel will wake-up immediately. If a channel is in low power mode and the signal detector is idle longer than 6ms, the receiver detection loop will be active again. If load is not detected, then the Channel will move to Device Unplug Mode and monitor the load continuously. If load is detected, it will return to Low Power Mode and receiver detection will be active again per 6ms.

Table 4-1. The I/O Termination Resistance Under Different Conditions

Symbol	Parameter	Resistance	Units
RX terminal			
Rin-pd	Input resistance at power down mode	78k to GND	Ω
Rin-U0	Input resistance at U0 condition	50 to VDD	Ω
Rin-U1	Input resistance inU1 (1)	50 to VDD	Ω
Rin-U2/U3	Input resistance in U2/U3 (1)	50 to VDD	Ω
Rin-RXDet	Input resistance in RXDET (1)	78k to VbiasRx	Ω
TX terminal			
Rout-pd	Output resistance at power down mode	78k to GND	Ω
Rout-U0	Output resistance at U0 condition	50 to VbiasTx1	Ω
Rout-U1	Output resistance in U1 mode (1)	6k to VbiadTx1	Ω
Rout-U2/U3	Output resistance in U2/U3 mode (1)	6k to VbiasTx2	Ω
Rout-RXDet	Output resistance in RXDET mode (1)	6k to VbiasTx2	Ω

Notes: (1) The value of Rin-RxDet will be updated only after the receiver evaluation has been done. Thus, the value can be 50Ω or 78kΩ pull-low.

4.4 DisplayPort Mode

The ON/OFF of each DP channel is controlled by the Aux lane count.

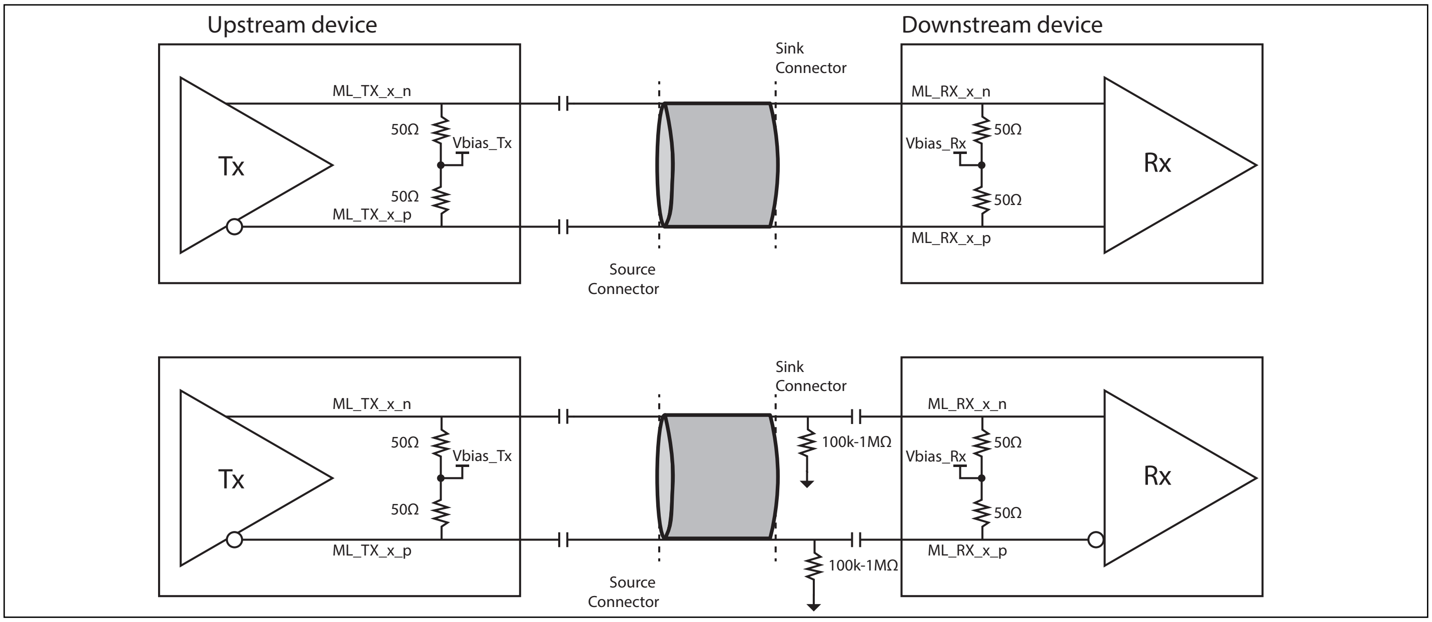


Figure 4-2 DisplayPort Main Link Connection Diagram

4.4.1 DisplayPort Main Link

The electrical sub-block of a DP Main-Link consists of up to four differential pairs. The DP TX drives doubly terminated, AC-coupled differential pairs, as shown in Figure 4-2 in a manner compliant with the Main-Link Transmitter electrical specification.

Table 4-2. DP Low Power Mode Description

PM_State	Mode	Description
1	Active mode	Data transfer (normal operation); The AUX monitor is actively monitoring for Link Training unless it is disabled through I2C interface. When programmed to DisplayPort mode, all Main Link outputs are Enabled by default.
2	Standby mode	Low power consumption (I2C interface is active; AUX monitor is inactive); Main Link outputs are disabled; the Sink device has de-asserted HPD
3	D3 power saving mode	Low power consumption(I2C interface is active; AUX monitor is active). Main link outputs are disabled. It is entered when AUX command receives request to enter D3 low power state. It is exited after HPD LOW for t_{HPD} or EN = 0 or AUX command receives request to exit.
4	Power down mode(OFF)	Lowest power consumption (EN = 0); all outputs are high-impedance; I2C interface is turned off, all inputs are ignored, I2C register is reset

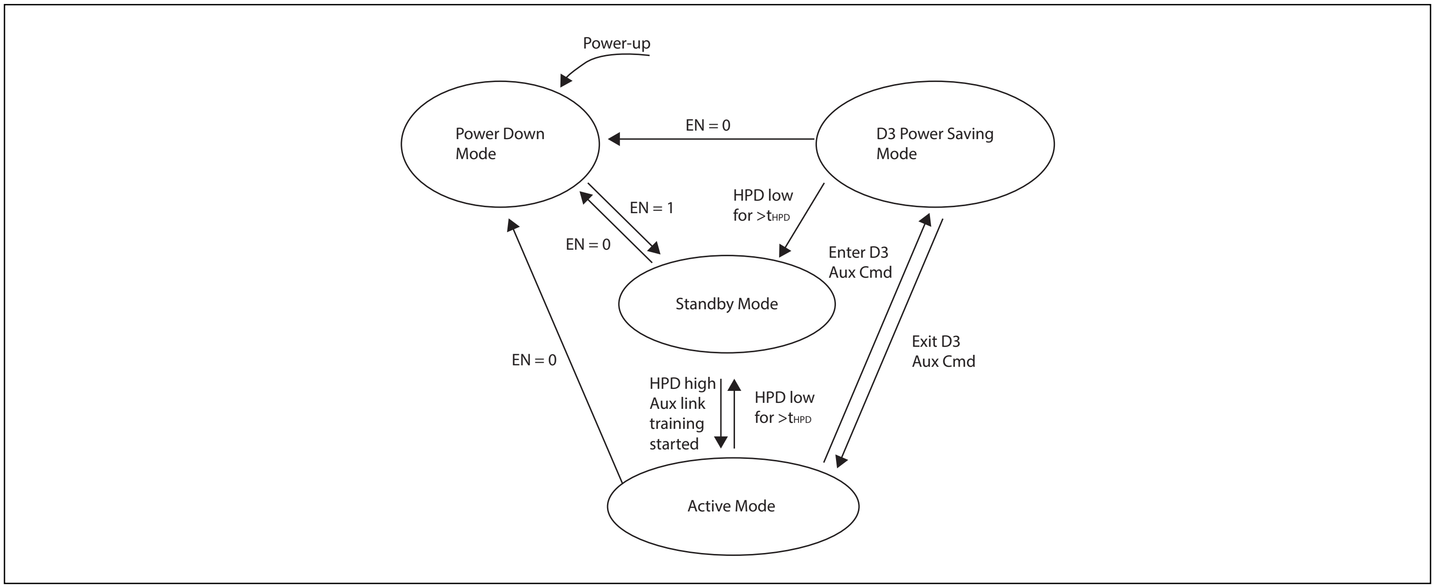


Figure 4-3 DisplayPort Operation mode

4.4.2 DisplayPort Aux Channel

The AUX CH of DP is a half-duplex, bidirectional channel. The DP device with DPTX such as a Source device is the master of the AUX CH (called AUX CH Requester), while the device with DPRX such as a Sink device is the slave (AUX CH Replier). As the master, the Source device must initiate a Request Transaction, to which the Sink device responds with a Reply Transaction.

The system design of a DFP_D on a USB Type-C connector connected to a UFP_D on a USB Type-C connector using a USB Type-C to USB Type-C Cable. The 2MΩ pull-down resistors on SBU1 and SBU2 are representative of the leakage of ESD and EMI/RFI components including termination to ensure no floating nodes, and are intended to show compliance with SBU Termination in USB Type-C r1.1. The plug orientation switch may be replaced by AUX polarity inversion logic in the DisplayPort transmitter or receiver, controlled by the plug orientation detection mechanism associated with the USB Type-C Receptacle. Note: The 3.3V levels in the Adapters are derived from VCONN because not all DisplayPort UFP_D devices provide DP_PWR.

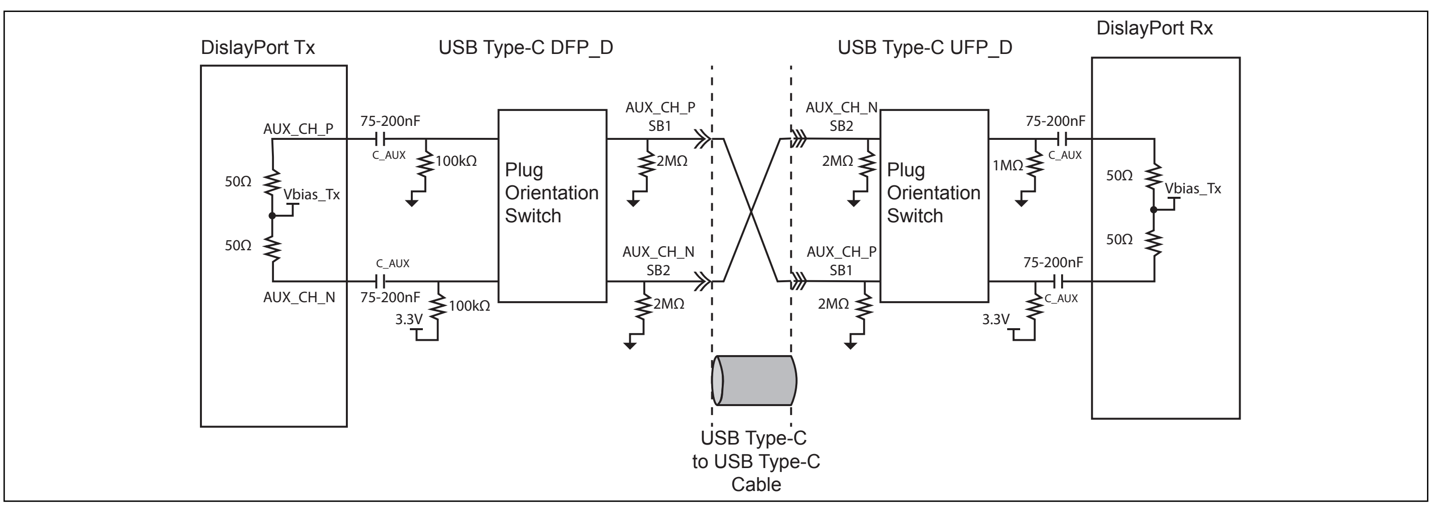


Figure 4-4 AUX Signaling Using USB Type-C to USB Type-C Cables

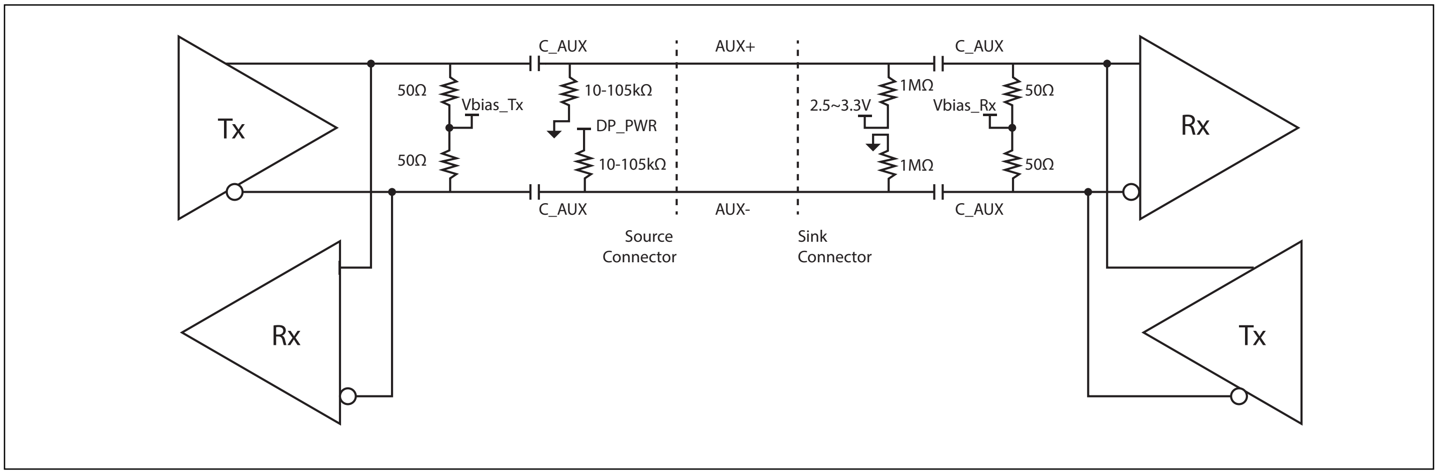


Figure 4-5 DisplayPort Aux Channel Connection

4.5 CTLE Equalization, Flat Gain, Output Linearity and Chip Enable Controls

Table 4-3. CTLE Equalization Gain. (Typical Values at FG = 0dB)

I2C Register Setting EQ<2:0>			Equalizer Setting (dB)			
EQ<2>	EQ<1>	EQ<0>	@1.35GHz	@2.5GHz	@4GHz	@5GHz
0	0	0	0 (Default)	0.1 (Default)	0.6 (Default)	1.1 (Default)
0	0	1	0	0.4	1.4	2.2
0	1	0	0.1	0.9	2.4	3.6
0	1	1	0.4	1.8	4.0	5.4
1	0	0	1.1	3.2	5.9	7.4
1	0	1	1.7	4.4	7.3	8.8
1	1	0	2.7	5.9	8.9	10.3
1	1	1	3.6	7.1	10.0	11.4

Table 4-4. Flat Gain Setting (FG)

I2C register FG[1:0]		Flat Gain setting
0	0	-4 dB
0	1	-2 dB
1	0	+0 dB (Default)
1	1	+2 dB

Table 4-5. Chip Enable Control

EN pin (pin #15)	Channel Operation
0	Disabled
1	Enabled (Default)

4.6 Detail Programming Registers

4.6.1 I2C Slave Address Selections

Table 4-6. I2C Slave Address Selections

I2C Slave Address Assignment							
A6	A5	A4	A3	A2	A1	A0	ADDR (Pin 16)
1	0	1	0	0	0	1	L
1	0	1	0	0	1	0	M/F
1	0	1	0	1	0	0	H

4.6.2 Indexed Read/Write Protocol

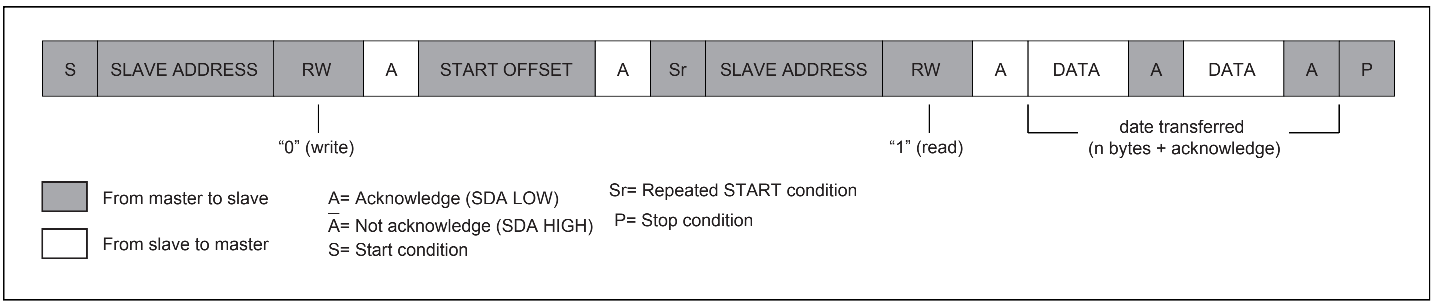


Figure 4-6 Indexed Read

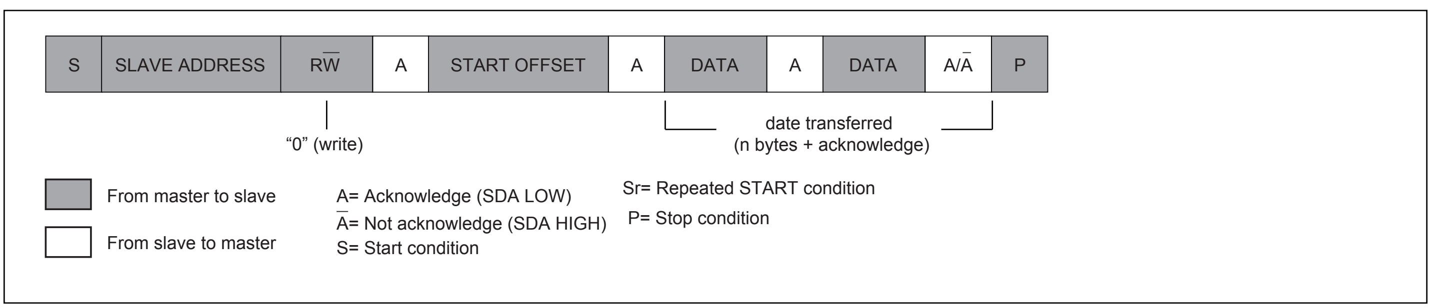


Figure 4-7 Indexed Write

4.7 I2C Register Definitions

4.7.1 BYTE 0 (Revision and Vendor ID Register)

Bit	Type	Power up condition	Comment
7	RO	0	Revision ID = 0000
6	RO	0	
5	RO	0	
4	RO	0	
3	RO	0	Vender ID = 0011
2	RO	0	
1	RO	1	
0	RO	1	

4.7.2 BYTE 1 (Device Type/Device ID Register)

Bit	Type	Power up condition	Comment
7	RO	0	Reserved
6	RO	0	
5	RO	0	
4	RO	1	
3	RO	0	Device ID = 0011
2	RO	0	
1	RO	1	
0	RO	1	

4.7.3 BYTE 2 (Byte count Register 32 bytes)

Bit	Type	Power up condition	Comment
7	RO	0	I2C register byte count = 32 bytes
6	RO	0	
5	RO	1	
4	RO	0	
3	RO	0	
2	RO	0	
1	RO	0	
0	RO	0	

4.7.4 BYTE 3 (Channel assignment of RXDET_EN and configuration mode)

Bit	Type	Power up condition	Comment
7	R/W	0	Operation mode setting. Refer to section 4.2.1
6	R/W	0	
5	R/W	0	
4	R/W	0	
3	R/W	0	Enable/Disable Generic Application mode 0 – Disable 1 – Enable
2	R/W	0	Enable/Disable RXDET_EN 0 – RXDET is Enabled. 1 – RXDET is Disabled.
1	R/W	0	Reserved
0	R/W	0	Reserved

4.7.5 BYTE 4 (Override the power down control and HPD signal bit)

Bit	Type	Power up condition	Comment
7	R/W	0	CON_RX1 power down override 0 – Do not force the CON_RX1 to power down state 1 – Force the CON_RX1 to power down state
6	R/W	0	CON_TX1 power down override 0 – Do not force the CON_TX1 to power down state 1 – Force the CON_TX1 to power down state
5	R/W	0	CON_TX2 power down override 0 – Do not force the CON_TX2 to power down state 1 – Force the CON_TX2 to power down state
4	R/W	0	CON_RX2 power down override 0 – Do not force the CON_RX2 to power down state 1 – Force the CON_RX2 to power down state
3	R/W	0	Reserved
2	R/W	1	
1	R/W	0	HPD signal bit setting.
0	R/W	0	Reserved

4.7.6 BYTE 5 Equalization and Flat gain setting of CON_RX2)

Bit	Type	Power up condition	Comment
7	R/W	0	Reserved
6	R/W	0	CON0_EQ<2> Equalizer setting
5	R/W	0	CON0_EQ<1> Equalizer setting
4	R/W	0	CON0_EQ<0> Equalizer setting
3	R/W	1	CON0_FG<1> Flat gain setting
2	R/W	0	CON0_FG<0> Flat gain setting
1	R/W	0	Reserved
0	R/W	0	Reserved

4.7.7 BYTE 6 (Equalization and Flat gain setting of CON_TX2)

Bit	Type	Power up condition	Comment
7	R/W	0	Reserved
6	R/W	0	CON1_EQ<2> Equalizer setting
5	R/W	0	CON1_EQ<1> Equalizer setting
4	R/W	0	CON1_EQ<0> Equalizer setting
3	R/W	1	CON1_FG<1> Flat gain setting
2	R/W	0	CON1_FG<0> Flat gain setting
1	R/W	0	Reserved
0	R/W	0	Reserved

4.7.8 BYTE 7 (Equalization and Flat gain setting of CON_TX1)

Bit	Type	Power up condition	Comment
7	R/W	0	Reserved
6	R/W	0	CON2_EQ<2> Equalizer setting
5	R/W	0	CON2_EQ<1> Equalizer setting
4	R/W	0	CON2_EQ<0> Equalizer setting
3	R/W	1	CON2_FG<1> Flat gain setting
2	R/W	0	CON2_FG<0> Flat gain setting
1	R/W	0	Reserved
0	R/W	0	Reserved

4.7.9 BYTE 8 (Equalization and Flat gain setting of CON_RX1)

Bit	Type	Power up condition	Comment
7	R/W	0	Reserved
6	R/W	0	CON3_EQ<2> Equalizer setting
5	R/W	0	CON3_EQ<1> Equalizer setting
4	R/W	0	CON3_EQ<0> Equalizer setting
3	R/W	1	CON3_FG<1> Flat gain setting
2	R/W	0	CON3_FG<0> Flat gain setting
1	R/W	0	Reserved
0	R/W	0	Reserved

4.7.10 BYTE 9 (AUX Flip control)

Bit	Type	Power up condition	Comment
7	R/W	0	Reserved
6	R/W	1	Reserved
5	R/W	1	Reserved
4	R/W	0	Reserved
3	R/W	0	Reserved
2	R/W	0	Reserved
1	R/W	0	AUX flip for AUXSBU1/2 and AUXP/N 0 – Flip is disabled 1 – Flip is enabled
0	R/W	0	DP FLIP DP flip for ALL CONx channels 0 – DP Flip is Disabled 1 – DP Flip is Enabled

4.7.11 BYTE 10 (Feature control of the CON0 and CON1)

Bit	Type	Power up condition	Comment
7	R/W	0	Reserved
6	R/W	1	Reserved
5	R/W	0	when Byte3 bit3 = 1, this bit Enable/Disable the deep slumber mode of CON0 and CON1 0 – Enable Deep slumber mode 1 - Disabled Deep slumber mode
4	R/W	0	Reserved
3	R/W	0	Reserved
2	R/W	0	Reserved
1	R/W	1	Reserved
0	R/W	0	Reserved

4.7.12 BYTE 11 (Feature control of the CON2 and CON3)

Bit	Type	Power up condition	Comment
7	R/W	0	Reserved
6	R/W	1	Reserved
5	R/W	0	when Byte3 bit3 = 1, this bit Enable/Disable the deep slumber mode of CON2 and CON3 0 – Enable Deep slumber mode 1 - Disabled Deep slumber mode
4	R/W	0	Reserved
3	R/W	0	Reserved
2	R/W	0	Reserved
1	R/W	1	Reserved
0	R/W	0	Reserved

4.7.13 BYTE 12 (AUX switch and AUX listener)

Bit	Type	Power up condition	Comment
7	R/W	0	Reserved
6	R/W	0	
5	R/W	1	
4	R/W	1	
3	R/W	0	
2	R/W	0	AUX_EN# 0 – Normal operation 1 – Disable AUX Listener and AUX Switch
1	R/W	0	AUX_Listener_EN# 0 – Normal operation 1 – Disable AUX Listener
0	R/W	1	Reserved

4.7.14 BYTE 13

Bit	Type	Power up condition	Comment
7	RO	N/A	Reserved
6	RO	N/A	
5	RO	N/A	
4	RO	N/A	
3	RO	N/A	
2	RO	N/A	
1	RO	N/A	
0	RO	N/A	

4.7.15 BYTE 14

Bit	Type	Power up condition	Comment
7	RO	N/A	Reserved
6	RO	N/A	
5	RO	N/A	
4	RO	N/A	
3	RO	N/A	
2	RO	N/A	
1	RO	N/A	
0	RO	N/A	

4.7.16 BYTE 15

Bit	Type	Power up condition	Comment
7	RO	N/A	Reserved
6	RO	N/A	
5	RO	N/A	
4	RO	N/A	
3	RO	N/A	
2	RO	N/A	
1	RO	N/A	
0	RO	N/A	

4.7.17 BYTE 16 (AUX and HPD status)

Bit	Type	Power up condition	Comment
7	RO	N/A	Reserved
6	RO	N/A	Reserved
5	RO	N/A	AUX_IDLE_DET# Detect the AUX activities "0" – Idle "1" – has activities
4	RO	N/A	DP_HPD The condition of HPD 0 – De-asserted 1 – Asserted
3	RO	N/A	Reserved
2	RO	N/A	Reserved
1	RO	N/A	Reserved
0	RO	N/A	Reserved

4.7.18 BYTE 17

Bit	Type	Power up condition	Comment
7	RO	0	Reserved
6	RO	0	
5	RO	0	
4	RO	1	
3	RO	0	
2	RO	1	
1	RO	0	
0	RO	0	

4.7.19 BYTE 18 (DPCD Address 00101h: Lane Count Set status)

Bit	Type	Power up condition	Comment
7	RO	0	LANE_COUNT_SET Main-Link Lane Count = Value. Bit<4:0>LANE_COUNT_SET Three values are supported. All other values are RESERVED. Note: Because the upstream device is required to set this value within the MAX_LINK_RATE register (DPCD Address 00001h), there is no power-on reset default value for this field. It is suggested to program this field to 1h. (See the Note within the description for the LINK_BW_SET register (DPCD Address 00100h.) 1h = 1 lane (Lane 0 only) 2h = 2 lanes (Lanes 0 and 1 only) 4h = 4 lanes A Source device may choose any lane count as long as it does not exceed the capability of the DPRX. For DPCD Ver.1.0: Bits <7:5> = RESERVED. Read all 0's. For DPCD Ver.1.1: Bits <6:5> = RESERVED. Read all 0's. Bit 7 = ENHANCED_FRAME_EN 0 = Enhanced Framing symbol sequence is not enabled. 1 = Enhanced Framing symbol sequence for BS and SR is enabled. Applicable to SST-only mode. A DPTX must set this bit to 1 when the DPRX has the ENHANCED_FRAME_CAP bit in the MAX_LANE_COUNT register (DPCD Address 00002h, bit 7) set to 1.
6	RO	0	
5	RO	0	
4	RO	0	
3	RO	0	
2	RO	1	
1	RO	0	
0	RO	0	

4.7.20 BYTE 19 - BYTE 30

Bit	Type	Power up condition	Comment
7	RO	0	Reserved
6	RO	0	
5	RO	0	
4	RO	0	
3	RO	0	
2	RO	0	
1	RO	0	
0	RO	0	

4.7.21 BYTE 31 (DPCD Address 00600h: DP Power set status)

Bit	Type	Power up condition	Comment
7	RO	0	SET_POWER_STATE Bit 2:0 001 = Set local Sink device and all downstream Sink devices to D0 (normal operation mode). 010 = Set local Sink device and all downstream Sink devices to D3 (power-down mode). 101 = Set Main-Link for local Sink device and all downstream Sink devices to D3 (power-down mode), keep AUX block fully powered, ready to reply within a Response Timeout period of 300us. All other values are RESERVED.
6	RO	0	
5	RO	0	
4	RO	0	
3	RO	0	
2	RO	0	
1	RO	0	
0	RO	1	

5. Electrical Specification

5.1 Absolute Maximum Ratings

Supply Voltage to Ground Potential .... –0.5V to V_{DD} +0.3V
Voltage Input to High Speed Differential Pins .... –0.5V to V_{DD}
Voltage Input to Low Speed Pins (SCL, SDA) .... –0.5V to +3.6V
Voltage Input to Low Speed Pins (AUXP/N, SBU1, SBU2) .... –0.5V to +3.6V
Voltage Input to EN .... –0.5V to V_{DD} +0.3V
Storage Temperature .... –65°C to +150°C
Junction Temperature .... 125°C
ESD HBM .... ±2000V
ESD CDM .... ±500V

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to beyond the absolute maximum rating conditions for extended periods may affect interoperability and degradation of device reliability and performance.

5.2 Recommended Operating Conditions

Over operating temperature range (unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max	Units
V_{DD}	VDD Supply Voltage	1.71	1.8	1.89	V
V_{DD_Noise}	Supply Noise up to 50 MHz(1)			50	mVpp
V_{RX_CM}	Input source common-mode noise			150	mVpp
$C_{ac\_coupling}$	System AC coupling capacitance	75		265	nF
T_A	Ambient Temperature, Industrial I-temp range	-40(1)		+85	°C

Notes:
(1) The minimum temperature -40°C can be guaranteed by design

5.3 Thermal Information

Symbol	Parameter	32-pin X2QFN	Unit
Theta JA	Junction-to-ambient resistance	42.09	°C/W

5.4 Power Consumption

Over operating temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
$I_{ON\_USB\_2DP}$	Current in 1-port USB3.2 Gen 2x1 & 2-lane DP1.4/DP2.1 (UHBR10)	EN = 1, HPD = active, 1 port USB 3.2 Gen 2x1 & 2 Lane DP mode		160	220	mA
I_{ON_4DP}	Current in DP mode by 4 Lane, VDD=1.8V	EN = 1, HPD = active, 4 Lane DP mode, Lane count = 4		160	220	mA
I_{ON_USBx1}	Current in USB3.2 Gen 2x1 U0 mode, VDD = 1.8V	EN = 1, USB3.2 Gen2x1 U0 mode		80	110	mA
I_{ON_USBx2}	Current in USB3.2 Gen 2x2 U0 mode, VDD = 1.8V	EN = 1, USB3.2 Gen2x2 U0 mode		160	220	mA

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
I_{U3_Gen2x1}	Average Current in USB3.2 Gen 2x1 U3 mode, VDD = 1.8V (per channel)	EN = 1, USB3.2 Gen2x1 U3 mode		0.9	1.5	mA
I_{D3}	Current in D3 Power saving mode, VDD = 1.8V	EN = 1, HPD = active, 4 Lane DP mode, Enter D3 mode		1.2	1.7	mA
I_{unplug}	Current in Unplug mode, VDD = 1.8V	EN = 1		700	1000	uA
I_{ENB}	Disabled mode	EN = 0		25	50	uA

5.5 AC/DC Characteristics

(VDD = 1.8V ± 5% TA = -40 to 85°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage		1.71	1.8	1.89	V
USB3.2 Receiver (RX) Electrical Specification						
$C_{RX\text{-}PARASITIC}$	Rx input capacitance	At 5GHz			1.0	pF
$R_{RX\text{-}DIFF\text{-}DC}$	DC Differential Input Impedance		72		120	Ω
$R_{RX\text{-}SINGLE\text{-}DC}$	DC single ended input impedance to guarantee RxDet	Measured with respect to GND over a voltage of 500mV max	18		30	Ω
$Z_{RX\text{-}HIZ\text{-}DC\text{-}PD}$	DC input CM input impedance for V>0 during reset or power down	(Vcm = 0 to 500mV)	25			kΩ
$V_{RX\text{-}CM\text{-}AC\text{-}P}$	Rx common mode peak voltage	AC up to 5GHz			150	mVpeak
$T_{RX\_TJ\ (5G)}$	USB3.2 Gen2 Rx total jitter	Measured after RX EQ of Scope at 5GHz (Figure 5, 6)			0.394	UI
$T_{RX\_DJ(5G)}$	USB3.2 Gen2 Rx deterministic jitter	Measured after RX EQ of Scope at 5GHz (Figure 5, 6)			0.21	UI
$T_{RX\_TJ\ (2.5G)}$	USB3.2 Gen1 Rx total jitter	Measured after RX EQ of Scope at 2.5GHz (Figure 5, 6)			0.45	UI
$T_{RX\_DJ(2.5G)}$	USB3.2 Gen1 Rx deterministic jitter	Measured after RX EQ of Scope at 2.5GHz (Figure 5, 6)			0.285	UI
USB3.2 Transmitter (TX) Electrical Specification						
$C_{TX\text{-}PARASITIC}$	Tx input capacitance				1.1	pF
$V_{TX\text{-}DIFF\text{-}PP\_5G}$	Output differential p-p voltage Swing	Differential Swing $\|V_{TX\text{-}D+} - V_{TX\text{-}D-}\|$ at -1dB compression point of 5GHz		0.9		Vppd
$V_{TX\text{-}DIFF\text{-}PP\_100M}$	Output differential p-p voltage Swing	Differential Swing $\|V_{TX\text{-}D+} - V_{TX\text{-}D-}\|$ at -1dB compression point of 100MHz		0.91		Vppd
$R_{TX\text{-}DIFF\text{-}DC}$	DC Differential TX Impedance		72		120	Ω
$V_{TX\text{-}RCV\text{-}DET}$	The amount of Voltage change allowed during RxDet	Type-C Tx Spec +/- 60mA			600	mV

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$I_{TX\text{-}SHORT}$	Transmitter short circuit current to ground		-60		60	mA
$R_{TX\text{-}DC\text{-}CM}$	Common mode DC output Impedance		18		30	Ω
$V_{TX\text{-}C}$	Common-Mode Voltage	$\mid V_{TX\text{-}D+} + V_{TX\text{-}D-} \mid /2$	V_{DD}-1V		V_{DD}	V
$V_{TX\text{-}CM\text{-}AC\text{-}PP\text{-}ACTIVE}$	Active mode TX AC common mode voltage	$V_{TX\text{-}D+} + V_{TX\text{-}D-}$ for both time and amplitude			100	mVpp
$V_{TX\text{-}CM\text{-}DC\text{-}Active\text{-}Idle\text{-}Delta}$ (1)	Common mode delta voltage $\mid Avg_{U0} (\mid V_{TX\text{-}D+} + V_{TX\text{-}D-} \mid)/2 - Avg_{U1} (\mid V_{TX\text{-}D+} + V_{TX\text{-}D-} \mid)/2 \mid$	Between U0 and U1/U2/U3			200	mVpeak
High-Speed Channel Electrical Specification						
t_{pd}	Channel latency	From input pin to output pin		150	300	Ps
G_{P_USB}	Peaking gain (Compensation at 5GHz, relative to 100MHz, 100mVp-p sine wave input)	EQ<2:0> = 000 EQ<2:0> = 001 EQ<2:0> = 010 EQ<2:0> = 011 EQ<2:0> = 100 EQ<2:0> = 101 EQ<2:0> = 110 EQ<2:0> = 111		1.1 2.2 3.6 5.4 7.4 8.8 10.3 11.4		dB
		Variation around typical	-2		+2	dB
G_{P_DP}	Peaking gain (Compensation at 4.05GHz, relative to 100MHz, 100mVp-p sine wave input)	EQ<2:0> = 000 EQ<2:0> = 001 EQ<2:0> = 010 EQ<2:0> = 011 EQ<2:0> = 100 EQ<2:0> = 101 EQ<2:0> = 110 EQ<2:0> = 111		0.6 1.4 2.4 4.0 5.9 7.3 8.9 10		dB
		Variation around typical	-2		+2	dB
G_F	Flat gain (100MHz, EQ<2:0>=000)	FG<1:0> = 00 FG<1:0> = 01 FG<1:0> = 10 FG<1:0> = 11		-4 -2 0 +2		dB
		Variation around typical	-2		+2	dB
V_{sw_100M}	Output linear swing (at 100MHz)	EQ<2:0>=000		910		mVppd
V_{sw_5G}	Output linear swing (at 5GHz)	EQ<2:0>=000		900		mVppd
D_{DNEXT} (2)	Differential near-end crosstalk	100MHz to 5GHz		-40		dB
D_{DFEXT} (2)	Differential far-end crosstalk	100MHz to 5GHz		-40		dB

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{NOISE_IN}	Input-referred noise	100MHz to 5GHz, EQ<2:0> = 000, FG<1:0> = 10, Figure 5-5		0.5		mV_{RMS}
		100MHz to 5GHz, EQ<2:0> = 111, FG<1:0> = 10, Figure 5-5		0.3		
V_{NOISE_OUT}	Output-referred noise	100MHz to 5GHz, EQ<2:0> = 000, FG<1:0> = 10, Figure 5-5		0.3		mV_{RMS}
		100MHz to 5GHz, EQ<2:0> = 111, FG<1:0> = 10, Figure 5-5		0.3		
S11DM	I/P Differential Mode Return loss (DP) AP_RX2P/N, AP_RX1N/P	4.05GHz		-14.5		dB
		5GHz		-12.7		
S11DM	I/P Differential Mode Return loss (USB/DP) AP_TX2P/N, AP_TX-1N/P	4.05GHz		-12.35		dB
		5GHz		-10.7		
S11CM	I/P Common Mode Return loss (DP) AP_RX2P/N, AP_RX1N/P	4.05GHz		-16.3		dB
		5GHz		-15		
S11CM	I/P Common Mode Return loss (USB/DP) AP_TX2P/N, AP_TX-1N/P	4.05GHz		-12.6		dB
		5GHz		-10.3		
S22DM	O/P Differential Mode Return loss (DP) AP_RX2P/N, AP_RX1N/P	4.05GHz		-13.6		dB
		5GHz		-12.1		
S22DM	O/P Differential Mode Return loss (USB/DP) AP_TX2P/N, AP_TX-1N/P	4.05GHz		-11.3		dB
		5GHz		-9.6		
S22CM	O/P Common Mode Return loss (DP) AP_RX2P/N, AP_RX1N/P	4.05GHz		-19.7		dB
		5GHz		-16.7		
S22CM	O/P Common Mode Return loss (USB/DP) AP_TX2P/N, AP_TX-1N/P	4.05GHz		-12		dB
		5GHz		-9.7		
LFPS and Unplug Detectors Electrical Specification						
F_{TH}	LFPS frequency detector	Detect the frequency of the input CLK pattern	100		400	MHz
$V_{RX\text{-}LFPS\text{-}DET\text{-}DIFF\text{-}P}$	LFPS detect threshold	LFPS signal threshold in U1/U2/U3 mode, the input impedance is set to 50Ω	100		300	mVppd
V_{TH_UPLUG}	LFPS Unplug mode detect threshold	LFPS signal threshold in Unplug mode. The input impedance is set to 78KΩ.	200		600	mVppd
T_{RXDECT_ON}	RX_DET response time	RX termination changes from 78KΩ to 50Ω			15	mS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T_{ON_SAVE}	Ton from USB power saving mode to active mode (U1/U2/U3 to U0)	Resume time from U1/U2/U3 back to U0 from LFPS detection. The termination resistor remains at 50Ω.			5	µS
DisplayPort Electrical Specification						
$V_{TX\text{-}C}$	Common-Mode Voltage	$\lvert V_{TX\text{-}D+} + V_{TX\text{-}D-} \rvert /2$	V_{DD}-1V		V_{DD}	V
$V_{TX\text{-}AC\text{-}CM\_HBR\_RBR}$	TX AC common mode voltage for HRB and RBR.	Measured using an 8b/10b pattern with 50% transition density			20	mVrms
$V_{TX\text{-}AC\text{-}CM\_HBR2}$	TX AC common mode voltage for HBR2				30	mVrms
$V_{TX\text{-}DIFFp\text{-}p\text{-}Level0}$	Differential peak-to-peak output voltage swing Level 0	Tested with Pre-emphasis at Level 0 = 0dB Level 1 = 3.5dB Level 2 = 6.0 dB	0.34	0.4	0.46	V
$V_{TX\text{-}DIFFp\text{-}p\text{-}Level1}$	Differential peak-to-peak output voltage swing Level 1		0.51	0.6	0.68	V
$V_{TX\text{-}DIFFp\text{-}p\text{-}Level2}$	Differential peak-to-peak output voltage swing Level 2		0.69	0.8	0.92	V
Tj_Tx Differential Noise Budget	HBR3 (8.1Gbps)	Measured at Tx output pins			0.27	UI
	HBR2 (5.4Gbps)				0.27	UI
	HBR (2.7Gbps)				0.294	UI
	RBR (1.62Gbps)				0.18	UI
AUX Channel Crossbar Switch and AUX Listener Electrical Specification						
V_{AUXDC}	AUX switch voltage range		0		3.3	V
$V_{AUX\text{-}DIFF\_PEAK}$	AUX switch peak-to-peak voltage		0.29		1.38	V
BW	-3dB bandwidth		100			MHz
Ron	The Resistance of AUX On	VCC = 1.8V; VI = 0 to 0.4V for AUXp; VI = 2.4V to 3.6V for AUXn; Tests shall be performed in both normal and inverted orientations.			10	Ω
Con	Input capacitance at SBU1, SBU2, AUXP or AUXN				10	pF
Ileak	Input leakage current at SBU1, SBU2, AUXP or AUXN	Measured at Vin(max) = 1.8V			15	µA
Ioff	Back current protection limit	When VDD is OFF and input voltage is 1.8V			10	uA
$VT_{(AUX\_listener)}$	Threshold of the AUX listener	VCC = 1.8V	100		220	mV_{PPd}

Note:
1. Measured using a vector-network analyzer (VNA) with -15dbm power level applied to the adjacent input. The VNA detects the signal at the output of the victim channel. All other inputs and outputs are terminated with 50Ω.
2. Subtract the Channel Gain from the Total Gain to get the Actual Crosstalk

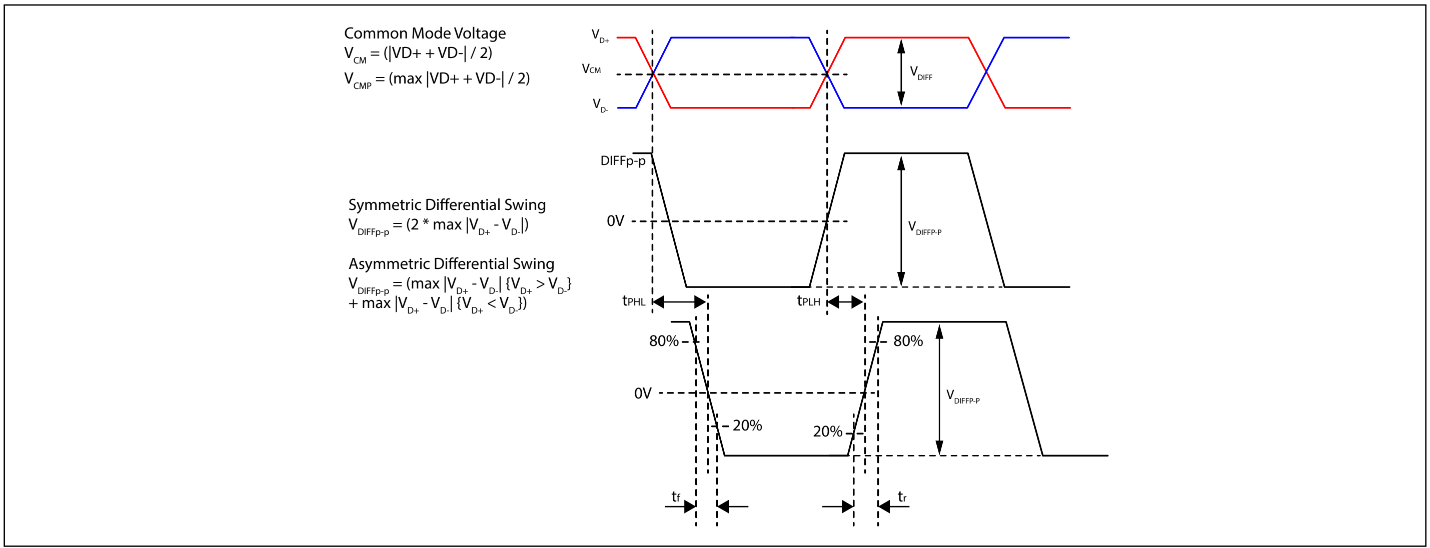


Figure 5-1 Definition of Peak-to-peak Differential Voltage

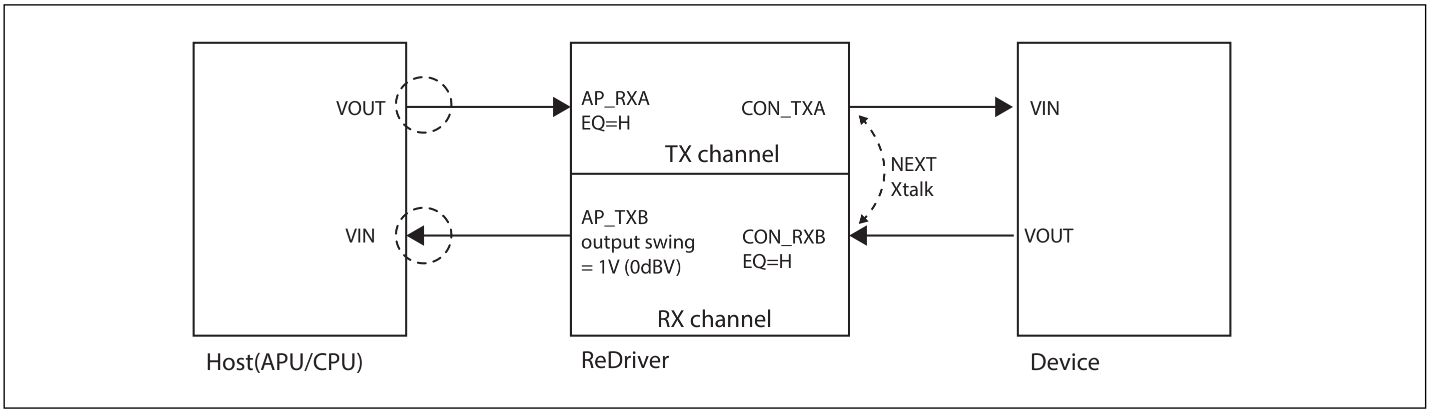


Figure 5-2 NEXT Crosstalk Definition

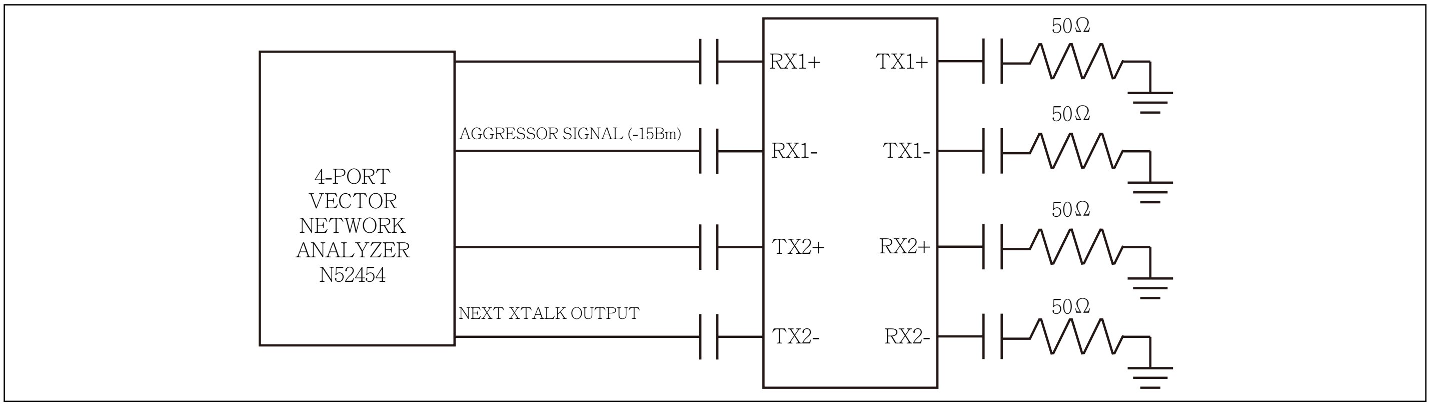


Figure 5-3 NEXT Channel-isolation Test Configuration

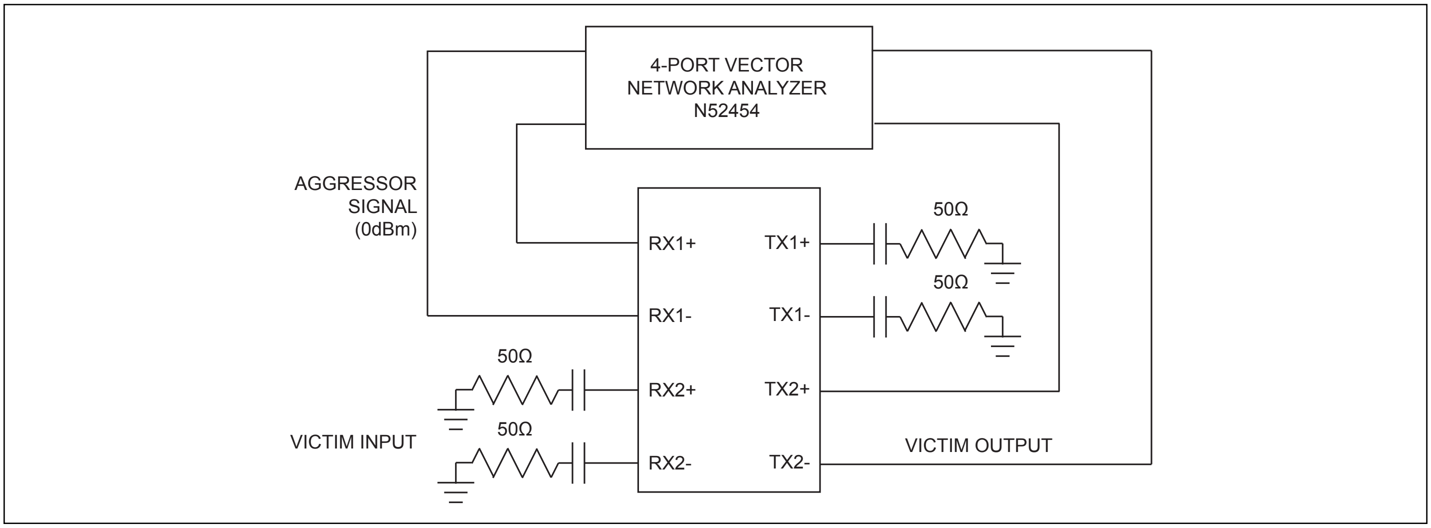


Figure 5-4 FEXT Channel-isolation Test Configuration

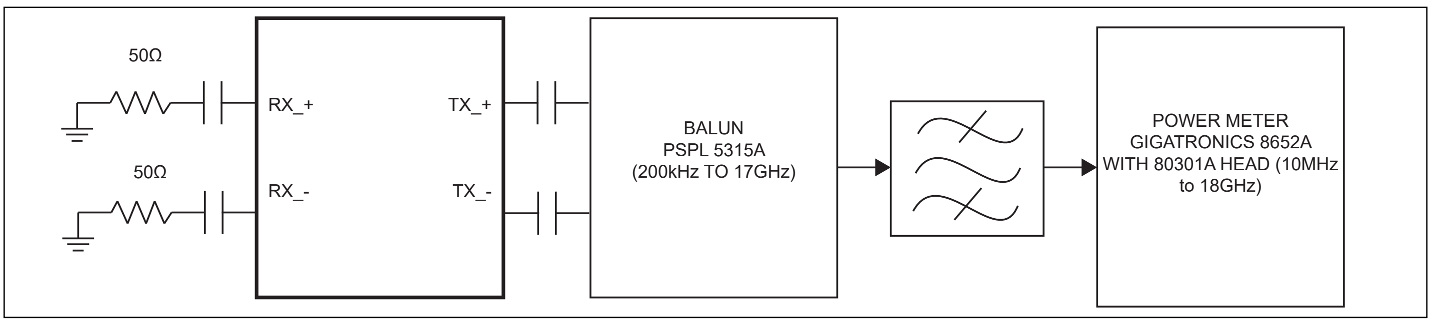
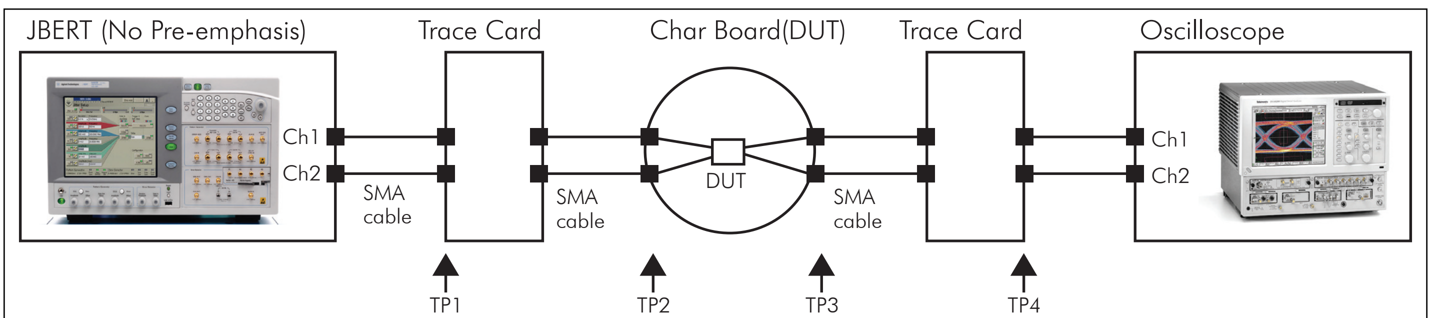


Figure 5-5 Noise Test Configuration



1) Trace card between TP1 and TP2 is designed to emulate 6-48" of FR4. Trace width -4 mils,100Ω differnetial impedance
2) All jitter is measured at a BER of 10-9
3) Residual jitter reflects the total jitter measured at TP4 jitter minus TP1 jitter
4) VDD = 3.3V, RT = 50Ω
5) The input signal from JBERT does not have any pre-emphasis.

Figure 5-6 AC Electrical Parameter Test Setup

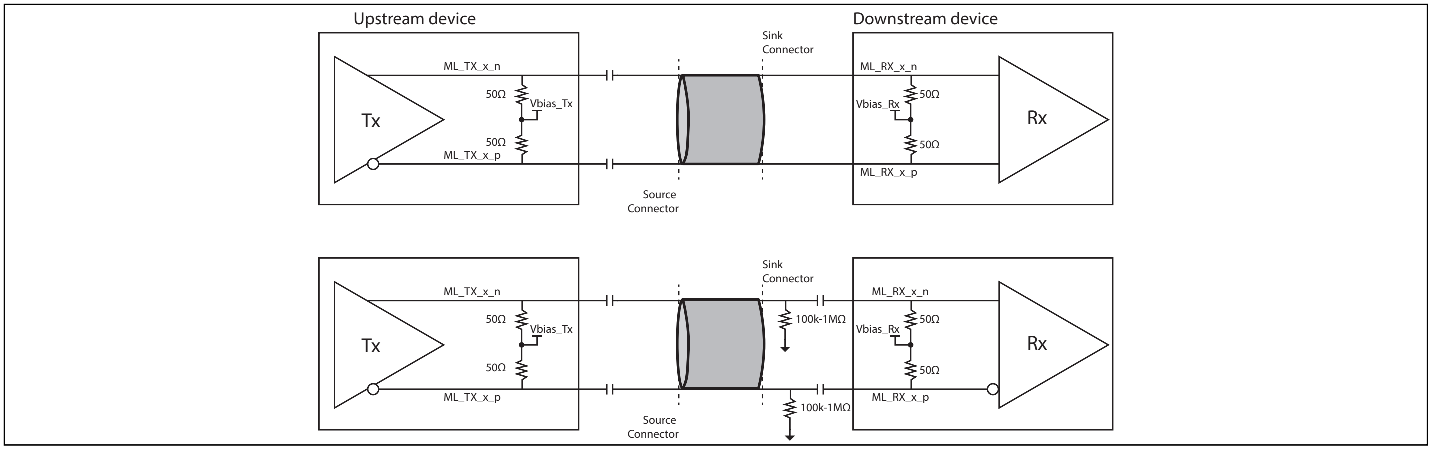


Figure 5-7 High-speed Chanel Test Circuit

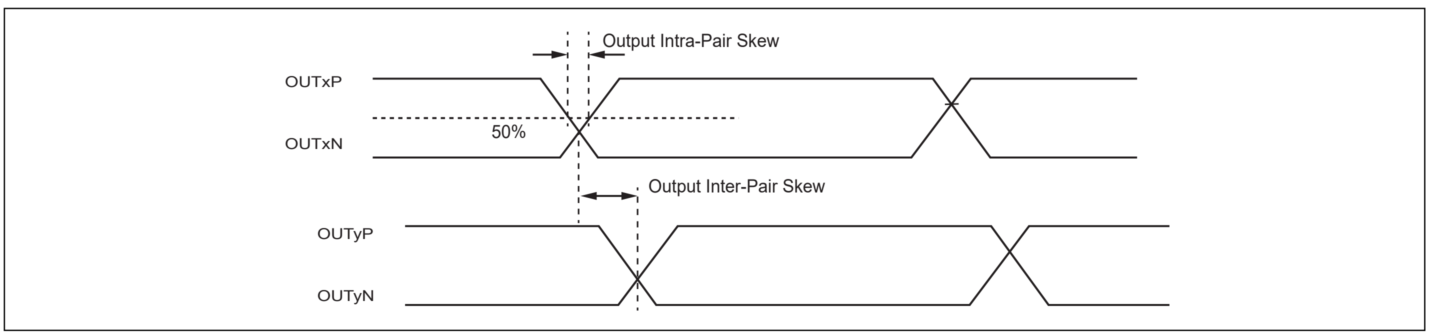


Figure 5-8 Intra and Inter-pair Differential Skew Definition

5.3 I2C Electrical Specification and Timing

5.3.1 Characteristics of the SDA and SCL I/O stages

Symbol	Parameter	Conditions	Min	Max	Units
V_{IL}	LOW-level input voltage		−0.5	0.4	V
V_{IH}	HIGH-level input voltage		1.2		V
V_{hys}	Hysteresis of Schmitt trigger inputs		0.05VDD		V
V_{OL}	LOW-level output voltage	Open-drain or open-collector at 3mA sink current; VDD >2V	0	0.4	V
I_{OL}	LOW-level output current	V_{OL} = 0.4V	20		mA
t_{of}	Output fall time from V_{IHmin} to V_{ILmax}		12	120	ns
t_{SP}	Pulse width of spikes that must be suppressed by the input filter		0	50	ns
I_I	Input current each I/O pin	0.1VDD < V_I < 0.9VDDmax	−10	+10	uA
C_I	Capacitance for each I/O pin			10	pF
f_{SCL}	SCL clock frequency		10	1000	kHz
$t_{HD;STA}$	Hold time (repeated) START condition	After this period, the first clock pulse is generated.	0.26		us
t_{LOW}	LOW period of the SCL clock		0.5		us
t_{HIGH}	HIGH period of the SCL clock		0.26		us
$t_{SU;STA}$	Set-up time for a repeated START condition		0.26		us
$t_{SU;DAT}$	Data set-up time		50		ns
Tr	Rise time of both SDA and SCL signals			120	ns
Tf	Fall time of both SDA and SCL signals		12	120	ns
$t_{SU;STO}$	Set-up time for STOP condition		0.26		us
t_{BUF}	Bus free time between a STOP and START condition		0.5		us
Cb	Capacitive load for each bus line			550	pF
$t_{VD;DAT}$	Data valid time			0.45	us
$t_{VD;ACK}$	Data valid acknowledge time			0.45	us

Characteristics of the SDA and SCL bus lines for Standard and Fast mode devices

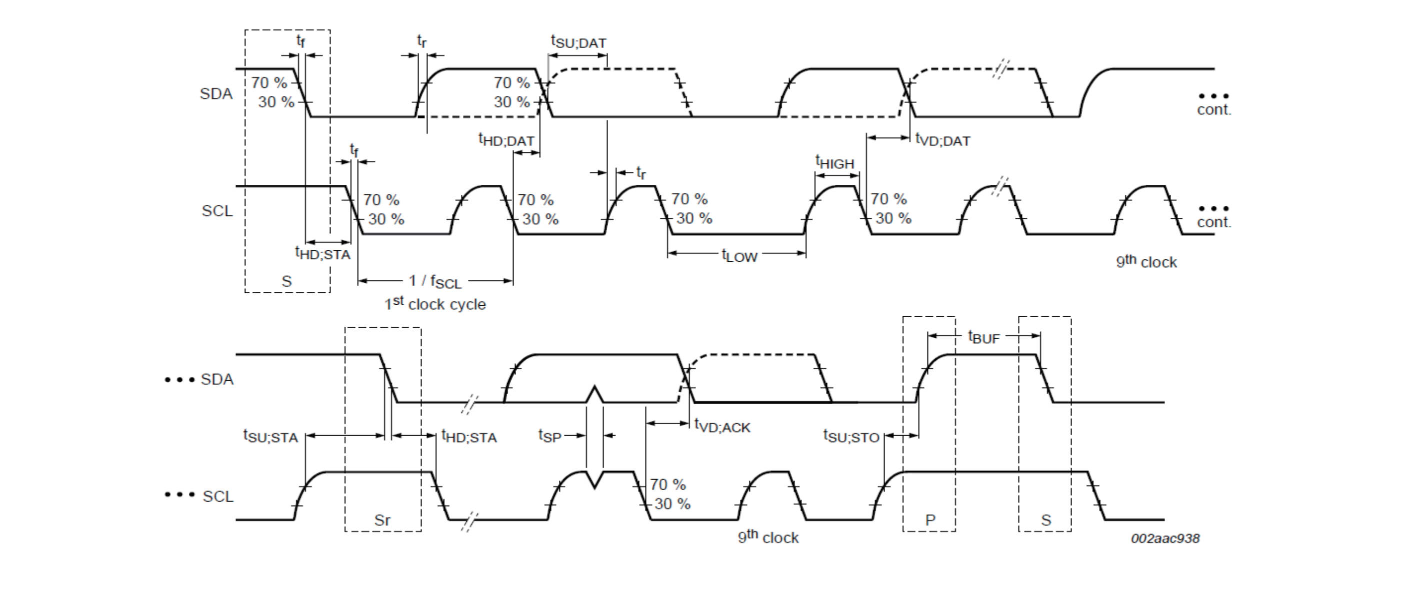


Figure 5-9 Definition of Timing for F/S-mode Devices on the I2C Bus

6. Applications

Note:
Information in the following applications sections is not part of the component specification, and does not warrant its accuracy or completeness. Customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

6.1 Type-C AC-cap Connection Diagram

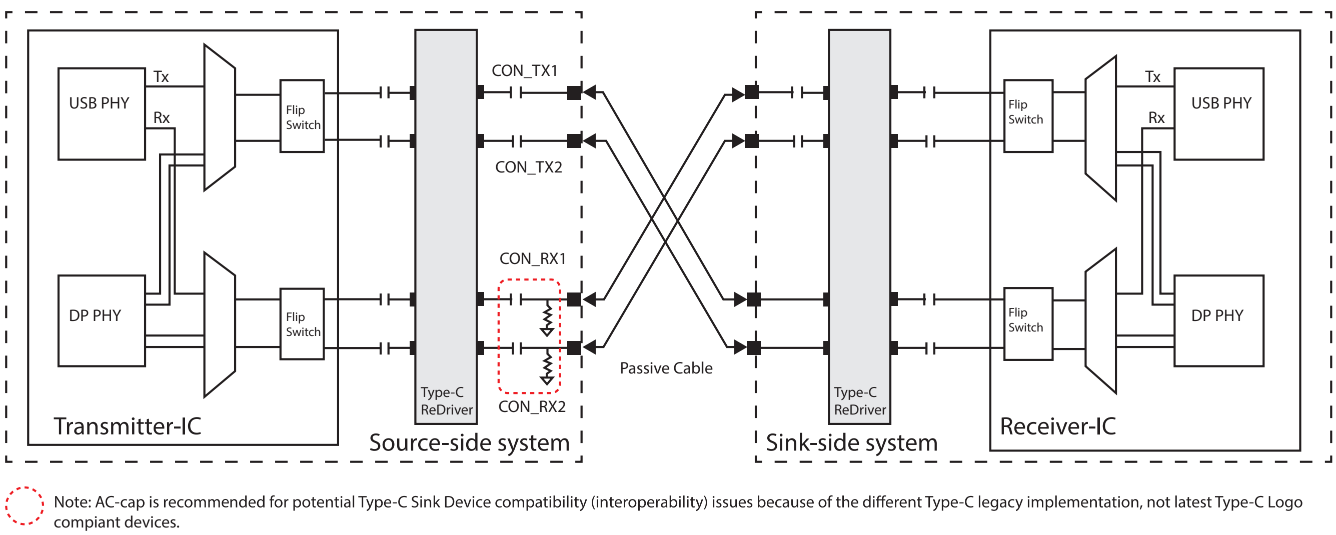
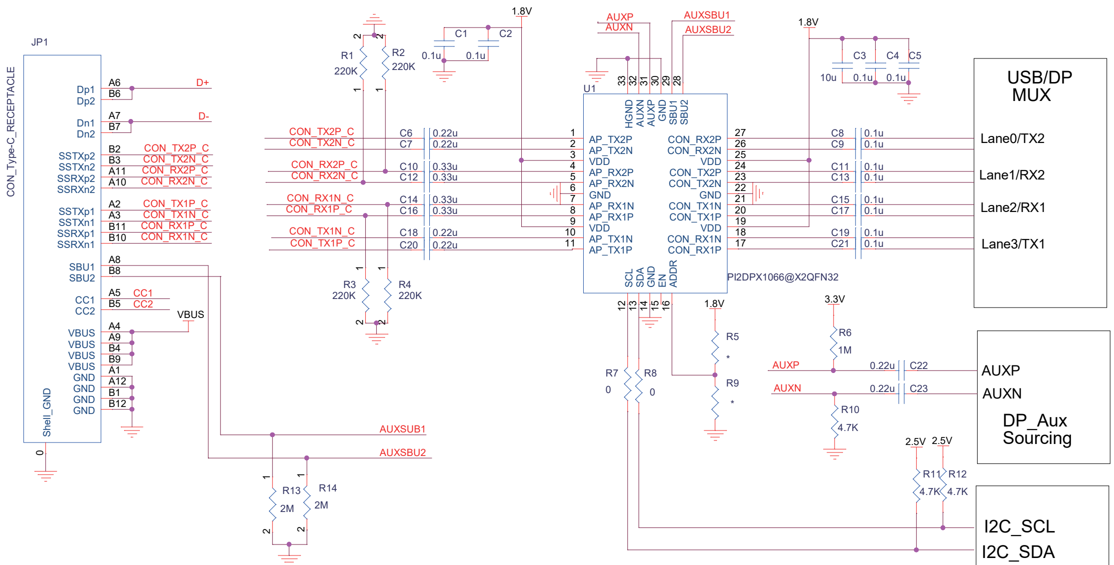


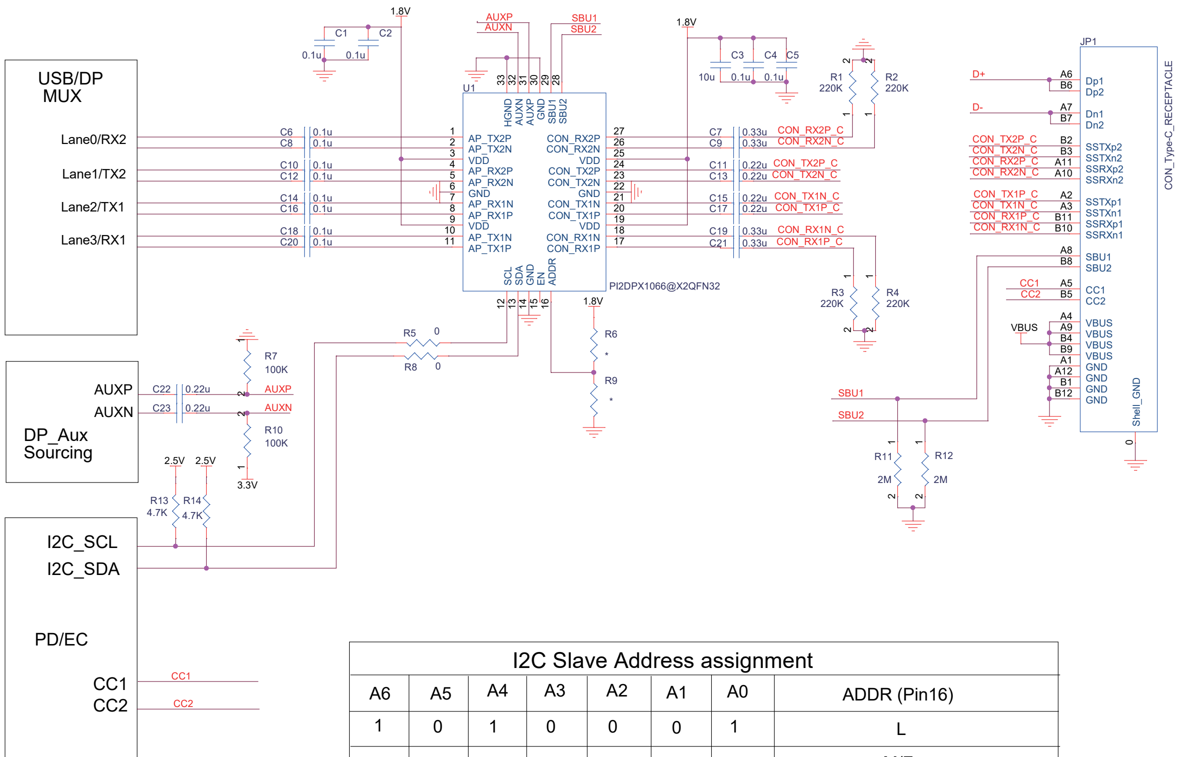
Figure 6-1 Type-C Coupling Capacitor Connection Diagram

6.2 Reference Application Schematics



I2C Slave Address assignment							
A6	A5	A4	A3	A2	A1	A0	ADDR (Pin16)
1	0	1	0	0	0	1	L
1	0	1	0	0	1	0	M/F
1	0	1	0	1	0	0	H

Figure 6-2 Reference EVB Demo Board Application Schematic - Sink Receptacle Application Circuit



I2C Slave Address assignment							
A6	A5	A4	A3	A2	A1	A0	ADDR (Pin16)
1	0	1	0	0	0	1	L
1	0	1	0	0	1	0	M/F
1	0	1	0	1	0	0	H

Figure 6-3 Reference EVB Demo Board Application Schematic - Source Application Circuit

6.3 PCB Layout Guideline

6.3.1 General Power and Ground Guideline

To provide a clean power supply for Diodes high-speed device, few recommendations are listed below:

- Power (VDD) and ground (GND) pins should be connected to corresponding power planes of the printed circuit board directly without passing through any resistor.
- The thickness of the PCB dielectric layer should be minimized such that the VDD and GND planes create low inductance paths.
- One low-ESR 0.1uF decoupling capacitor should be mounted at each VDD pin or should supply bypassing for at most two VDD pins. Capacitors of smaller body size, i.e. 0402 package, is more preferable as the insertion loss is lower. The capacitor should be placed next to the VDD pin.
- One capacitor with capacitance in the range of 4.7uF to 10uF should be incorporated in the power supply decoupling design as well. It can be either tantalum or an ultra-low ESR ceramic.
- A ferrite bead for isolating the power supply for Diodes high-speed device from the power supplies for other parts on the printed circuit board should be implemented.
- Several thermal ground vias must be required on the thermal pad. 25-mil or less pad size and 14-mil or less finished hole are recommended.

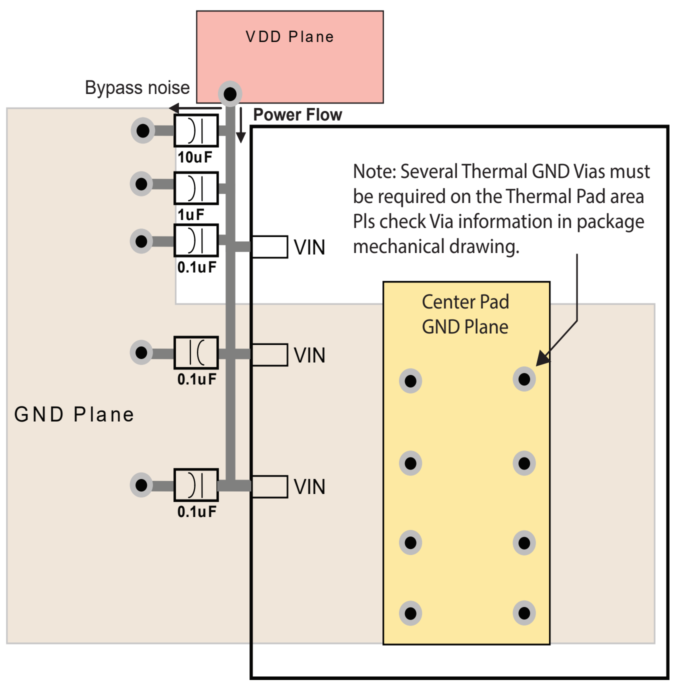


Figure 6-4 Decoupling Capacitor Placement Diagram

6.3.2 High-speed Differential Signal Routing

Well-designed layout is essential to prevent signal reflection:

- For 90Ω differential impedance, width-spacing-width micro-strip of 6-7-6 mils is recommended; for 100Ω differential impedance, width-spacing-width micro-strip of 5-7-5 mils is recommended.
- Differential impedance tolerance is targeted at ±15%.

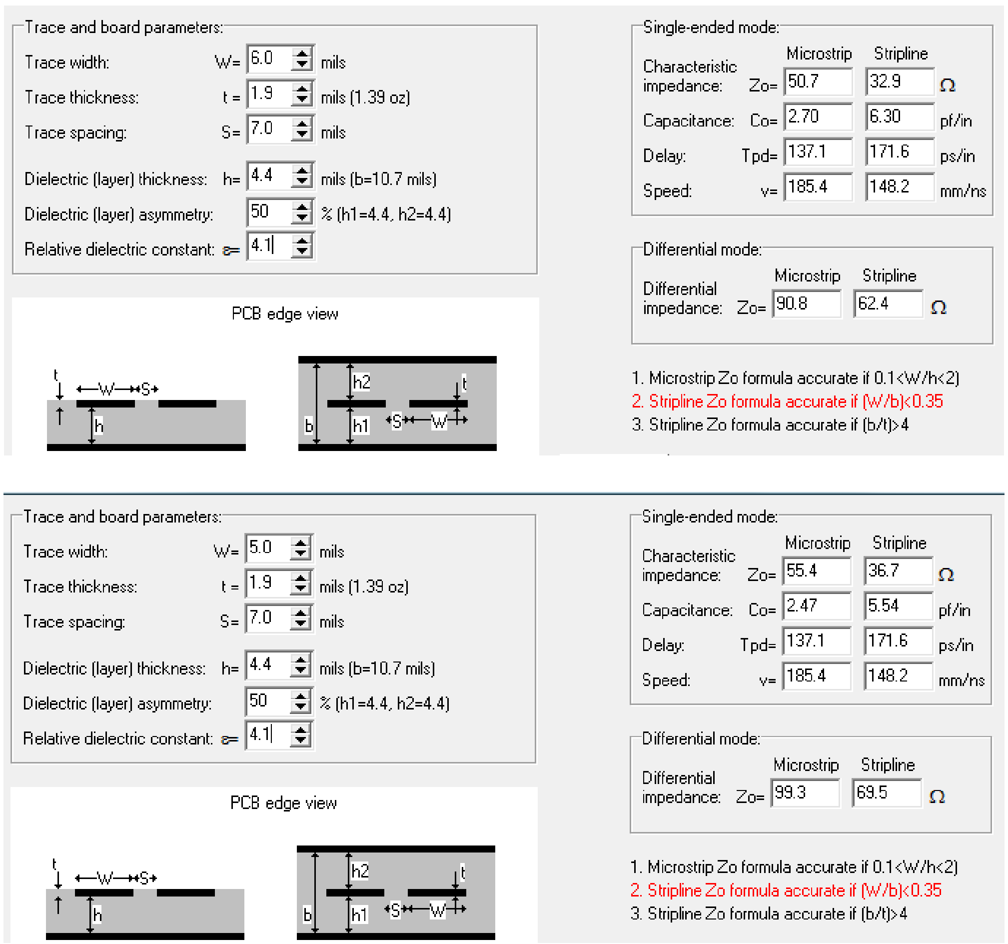


Figure 6-5 Trace Width and Clearance of Micro-strip and Strip-line

- For micro-strip, using 1/2oz Cu is fine. For strip-line in 6+ PCB layers, 1oz Cu is more preferable.

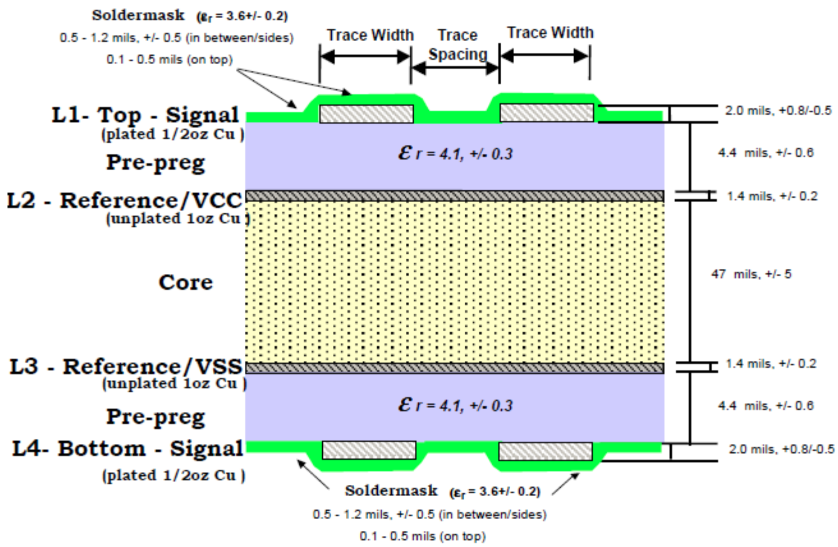


Figure 6-6 4-Layer PCB Stack-up Example

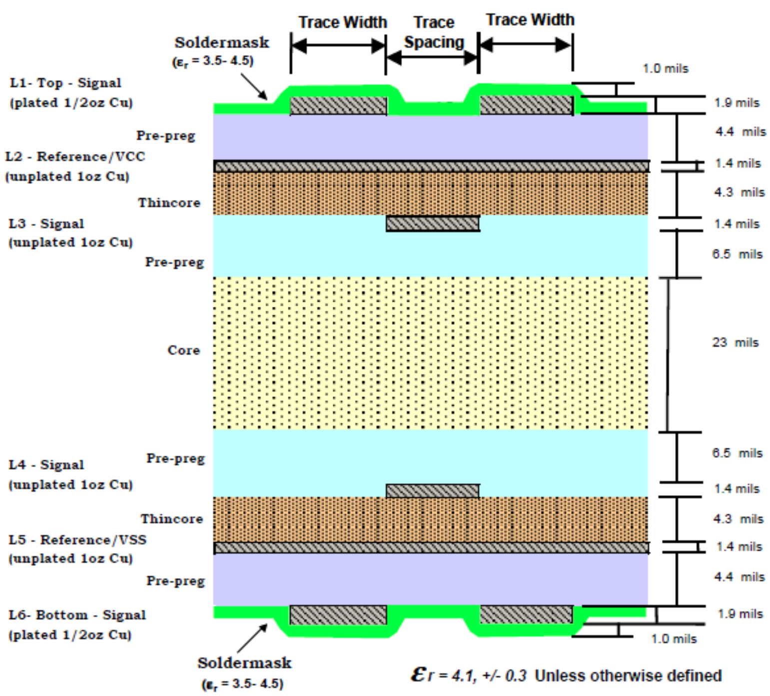


Figure 6-7 6-Layer PCB Stack-up Example

- Ground referencing is highly recommended. If unavoidable, stitching capacitors of 0.1uF should be placed when reference plane is changed.

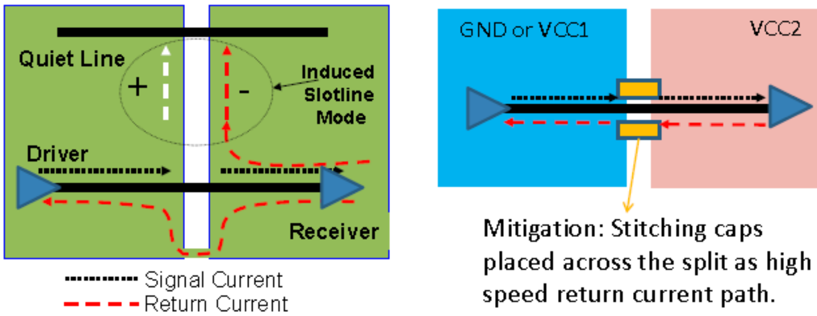


Figure 6-8 Stitching Capacitor Placement

- To keep the reference unchanged, stitching vias must be used when changing layers.
- Differential pair should maintain symmetrical routing whenever possible. The intra-pair skew of micro-strip should be less than 5 mils.

- To keep the reference unchanged, stitching vias must be used when changing layers.
- Differential pair should maintain symmetrical routing whenever possible. The intra-pair skew of micro-strip should be less than 5 mils.

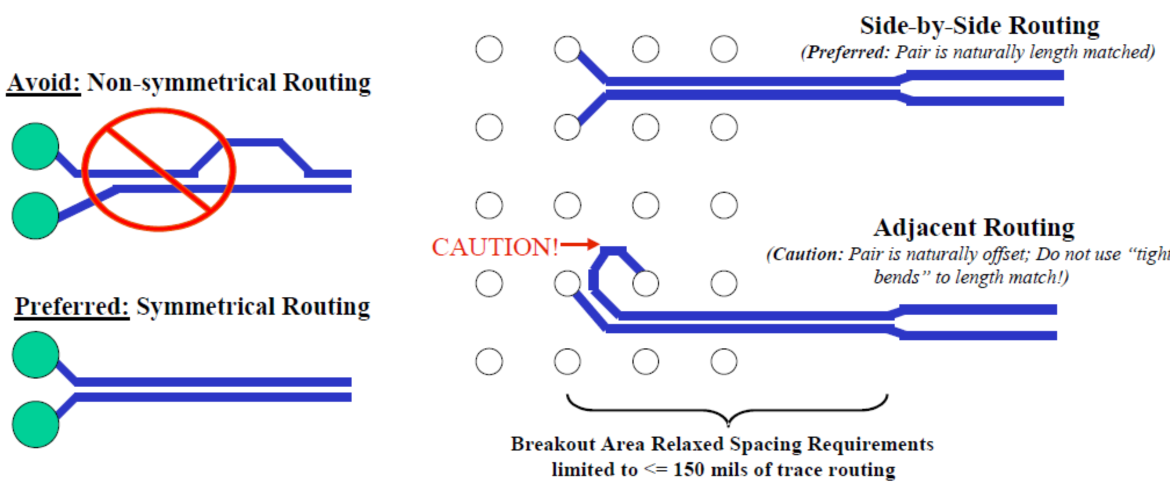


Figure 6-9 Layout Guidance of Matched Differential Pair

- For minimal crosstalk, inter-pair spacing between two differential micro-strip pairs should be at least 20 mils or 4 times the dielectric thickness of the PCB.
- Wider trace width of each differential pair is recommended in order to minimize the loss, especially for long routing. More consistent PCB impedance can be achieved by a PCB vendor if trace is wider.
- Differential signals should be routed away from noise sources and other switching signals on the printed circuit board.
- To minimize signal loss and jitter, tight bend is not recommended. All angles α should be at least 135 degrees. The inner air gap A should be at least 4 times the dielectric thickness of the PCB.

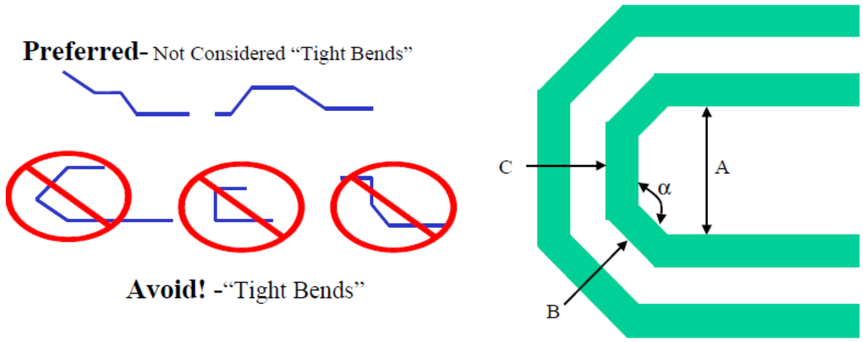


Figure 6-10 Layout Guidance of Bends

- Stub creation should be avoided when placing shunt components on a differential pair.

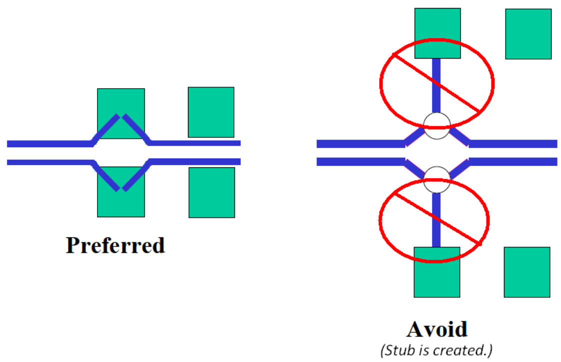


Figure 6-11 Layout Guidance of Shunt Component

- Placement of series components on a differential pair should be symmetrical.

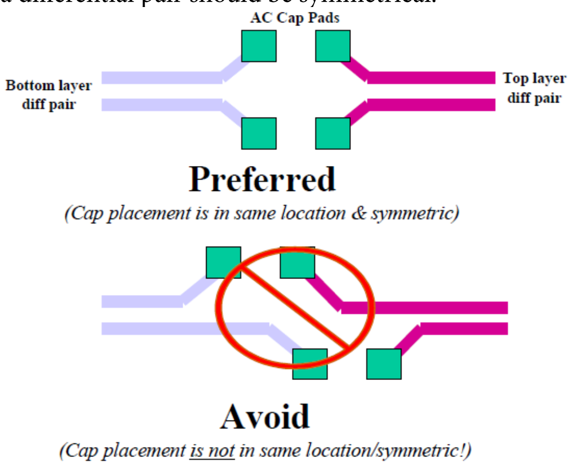


Figure 6-12 Layout Guidance of Series Component

- Stitching vias or test points must be used sparingly and placed symmetrically on a differential pair.

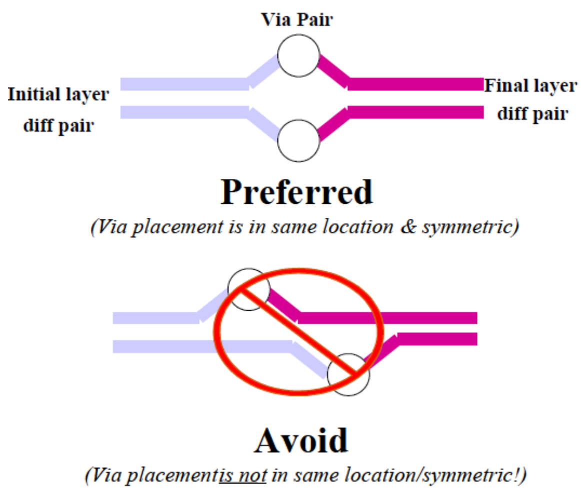
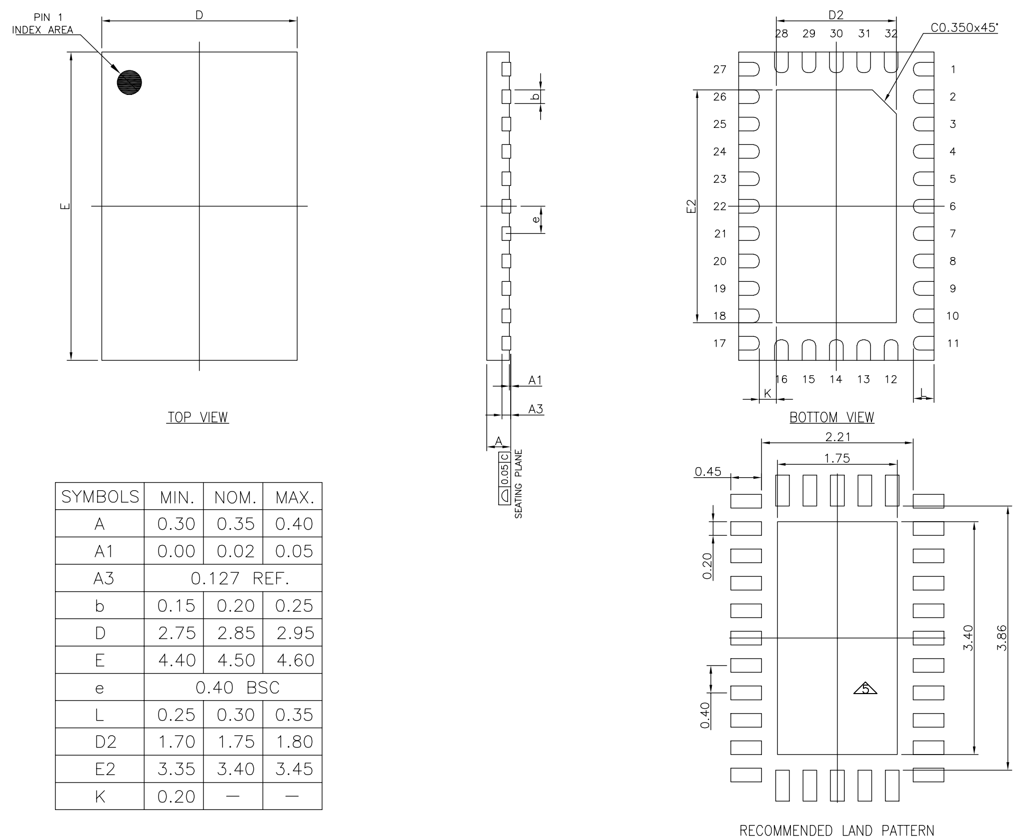


Figure 6-13 Layout Guidance of Stitching Via

7. Mechanical/Packaging Information

7.1 Mechanical Outline



SYMBOLS	MIN.	NOM.	MAX.
A	0.30	0.35	0.40
A1	0.00	0.02	0.05
A3	0.127 REF.		
b	0.15	0.20	0.25
D	2.75	2.85	2.95
E	4.40	4.50	4.60
e	0.40 BSC		
L	0.25	0.30	0.35
D2	1.70	1.75	1.80
E2	3.35	3.40	3.45
K	0.20	—	—

NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS
3. REFER JEDEC MO-288
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY
5. THERMAL PAD SOLDERING AREA (MESH STENCIL DESIGN IS RECOMMENDED)

DIODES INCORPORATED PERICOM A PRODUCT LINE OF DIODES INCORPORATED ENABLING SERIAL CONNECTIVITY

DATE: 10/28/19

DESCRIPTION: 32-Pin, X2QFN 2.85X4.5mm

PACKAGE CODE: XUA (XUA32)

DOCUMENT CONTROL #: PD-2247 **REVISION: --**

19-0420

Figure 7-1 PI2DPX1066 (32-pin) Package Mechanical Dimension

7.2 Part Marking Information

Our standard product mark follows our standard part number ordering information, except for those products with a speed letter code. The speed letter code mark is placed after the package code letter, rather than after the device number as it is ordered. After electrical test screening and speed binning has been completed, we then perform an "add mark" operation which places the speed code letter at the end of the complete part number.

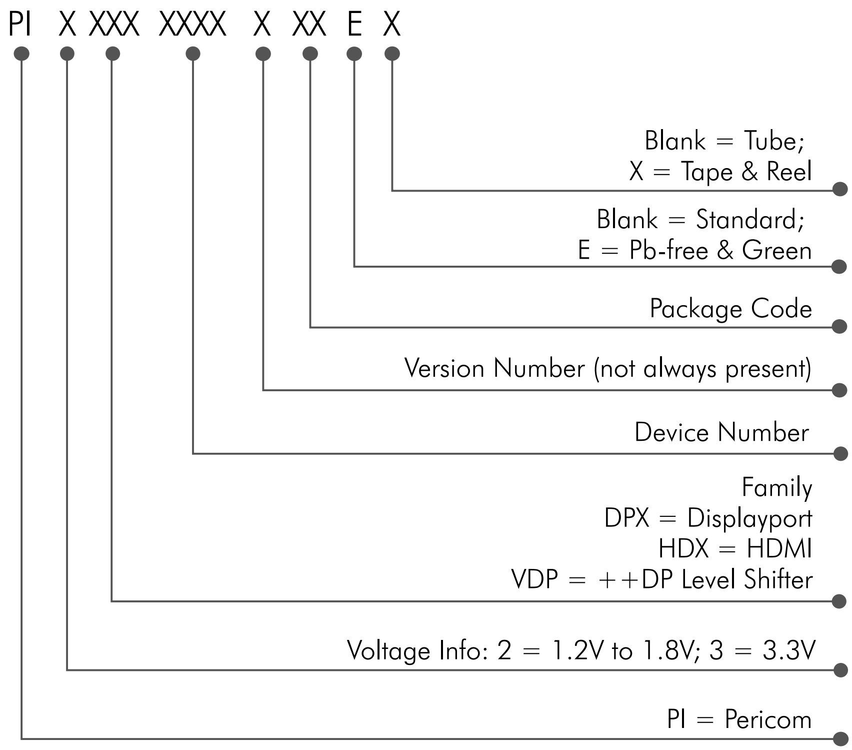
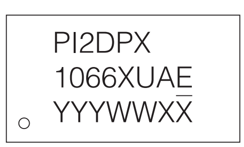


Figure 7-2 Part Naming Information



Y: Die Rev
YY: Year
WW: Week
1st X: Assembly Code
2nd X: Fab Code
Bar above Fab Code means Cu wire

Figure 7-3 Part Marking Information

7.3 Tape & Reel Materials and Design

Carrier Tape

The Pocketed Carrier Tape is made of Conductive Polystyrene plus Carbon material (or equivalent). The surface resistivity is 10^6Ohm/sq. maximum. Pocket tapes are designed so that the component remains in position for automatic handling after cover tape is removed. Each pocket has a hole in the center for automated sensing if the pocket is occupied or not, thus facilitating device removal. Sprocket holes along the edge of the center tape enable direct feeding into automated board assembly equipment. See Figures 7-3 and 7-4 for carrier tape dimensions.

Cover Tape

Cover tape is made of Anti-static Transparent Polyester film. The surface resistivity is 10^7Ohm/Sq. Minimum to 10^{11}Ohm sq. maximum. The cover tape is heat-sealed to the edges of the carrier tape to encase the devices in the pockets. The force to peel back the cover tape from the carrier tape shall be a MEAN value of 20 to 80gm (2N to 0.8N).

Reel

The device loading orientation is in compliance with EIA-481, current version (Figure 7-2). The loaded carrier tape is wound onto either a 13-inch reel, (Figure 7-4) or 7-inch reel. The reel is made of Antistatic High-Impact Polystyrene. The surface resistivity 10^7Ohm/sq. minimum to 10^{11}Ohm/sq. max.

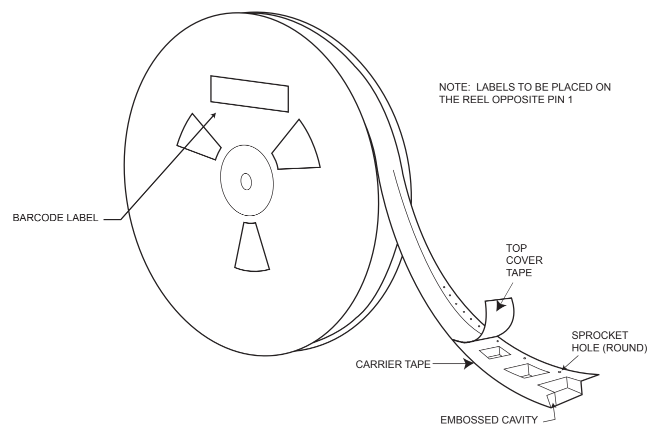


Figure 7-4 Tape & Reel Label Information

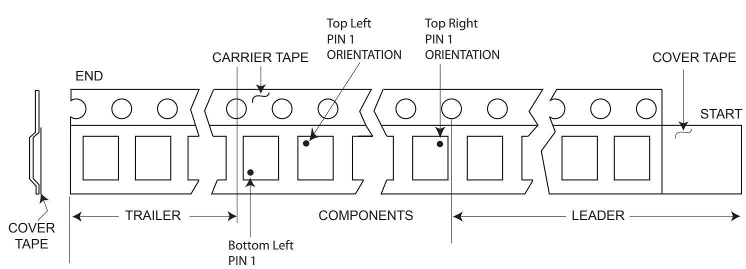


Figure 7-5 Tape Leader and Trailer Pin 1 Orientations

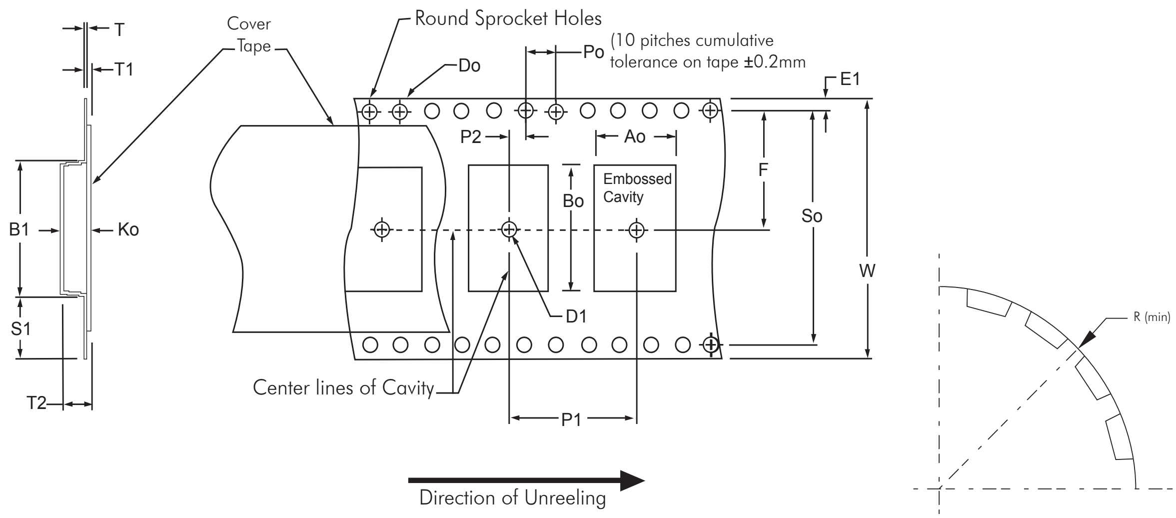


Figure 7-6 Standard Embossed Carrier Tape Dimensions

Table 7-1. Constant Dimensions

Tape Size	D_0	D_1 (Min)	E_1	P_0	P_2	R (See Note 2)	S_1 (Min)	T (Max)	T_1 (Max)
8mm	1.5 +0.1 -0.0	1.0	1.75 ± 0.1	4.0 ± 0.1	2.0 ± 0.05	25	0.6	0.6	0.1
12mm		1.5				30			
16mm					2.0 ± 0.1				
24mm									
32mm		2.0				50	N/A (See Note 3)		
44mm					2.0 ± 0.15				

Table 7-2. Variable Dimensions

Tape Size	P_1	B_1 (Max)	E_2 (Min)	F	So	T_2 (Max.)	W (Max)	A_0, B_0, & K_0
8mm	Specific per package type. Refer to FR-0221 (Tape and Reel Packing Information)	4.35	6.25	3.5 ± 0.05	N/A (see note 4)	2.5	8.3	See Note 1
12mm		8.2	10.25	5.5 ± 0.05		6.5	12.3	
16mm		12.1	14.25	7.5 ± 0.1		8.0	16.3	
24mm		20.1	22.25	11.5 ± 0.1		12.0	24.3	
32mm		23.0	N/A	14.2 ± 0.1	28.4± 0.1		32.3	
44mm		35.0	N/A	20.2 ± 0.15	40.4 ± 0.1	16.0	44.3	

Notes:

1. A0, B0, and K0 are determined by component size. The cavity must restrict lateral movement of component to 0.5mm maximum for 8mm and 12mm wide tape and to 1.0mm maximum for 16,24,32, and 44mm wide carrier. The maximum component rotation within the cavity must be limited to 20o maximum for 8 and 12 mm carrier tapes and 10o maximum for 16 through 44mm.
2. Tape and components will pass around reel with radius "R" without damage.
3. S1 does not apply to carrier width ≥32mm because carrier has sprocket holes on both sides of carrier where Do≥S1.
4. So does not exist for carrier ≤32mm because carrier does not have sprocket hole on both side of carrier.

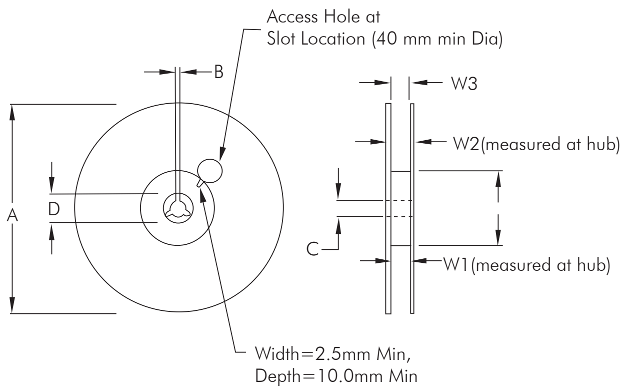


Figure 7-7 Reel Dimensions

Table 7-3. Reel Dimensions by Tape Size

Tape Size	A	N (Min) See Note A	W_1	W_2(Max)	W_3	B (Min)	C	D (Min)
8mm	178 ±2.0mm or 330±2.0mm	60 ±2.0mm or 100±2.0mm	8.4 +1.5/-0.0 mm	14.4 mm	Shall Accommodate Tape Width Without Interference	1.5mm	13.0 +0.5/-0.2 mm	20.2mm
12mm			12.4 +2.0/-0.0 mm	18.4 mm				
16mm	330 ±2.0mm	100 ±2.0mm	16.4 +2.0/-0.0 mm	22.4 mm				
24mm			24.4 +2.0/-0.0 mm	30.4 mm				
32mm			32.4 +2.0/-0.0 mm	38.4 mm				
44mm			44.4 +2.0/-0.0 mm	50.4 mm				

Note:

1. A. If reel diameter A=178 ±2.0mm, then the corresponding hub diameter (N(min) will by 60 ±2.0mm. If reel diameter A=330±2.0mm, then the corresponding hub diameter (N(min)) will by 100±2.0mm.

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