ULTRA-LOW VOLTAGE, AUTO-DIRECTION SENSING, 4-BIT LEVEL SHIFTER

Description

The LXS0204/LXS0204L is a 4-bit, configurable, dual-supply, bi-directional, auto-sensing translator that does not require a directional control pin. The A and B ports are designed to track two different power supply rails, V_{CCA} and V_{CCB} respectively. The V_{CCA} supply rail is configurable from 0.72V to 1.98V. The V_{CCB} supply rail is configurable from 1.65V to 5.5V. This allows voltage logic signals on the V_{CCA} side to be translated into higher or equal value voltage logic signals on the V_{CCB} side.

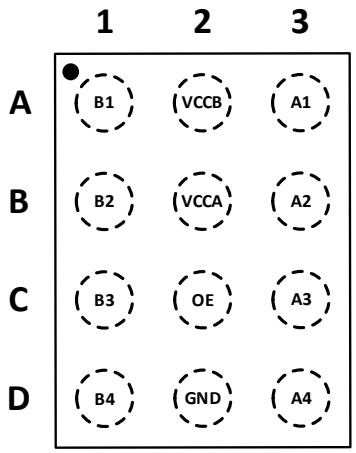
The translator has integrated 10kΩ pullup resistors on the Port A lines and Port B lines for up to 150 pF loading. The integrated pullup resistors are used to pull up the I/O lines to either V_{CCA} or V_{CCB}.

Port A and OE are referenced to V_{CCA} and port B is referenced to V_{CCB}. A LOW level at pin OE causes all I/Os to be a high-impedance OFF-state. Power-off protection is implemented to prevent the current from passing through the device when it is powered down.

The LXS0204/LXS0204L is an excellent match for open-drain applications such as the I2C communication bus. For push-pull applications, the LXS0204L disables the internal pullup resistors during logic-low and re-enables the internal pullup resistors during logic-high, thereby reducing static power consumption.

Pin Assignments

Transparent
Top View



U-WLB1014-12
(Type JC)

Features

- 0.72V to 1.98V on A Port, and 1.65V to 5.5V on B Port
- V_{CCA} must be less than or equal to V_{CCB}
- High Speed with 24Mb/s Data Rate for Push-Pull Applications
  - 27Mb/s Data Rate with 30pF (V_{CCA} = 1.2V, V_{CCB} = 1.8V)
- High Speed with 2Mb/s Data Rate for Open-Drain Applications
- Supports I2C High-Speed Mode (3.4MHz) with up to 150pF ($V_{CCA} \geq$ 1.08V)
- No Direction-Control Signal Needed
- Low Bit-to-Bit Skew
- Non-Preferential Power-Up Sequencing
- ESD Protection
  - HBM JEDEC JS-001-2023 Class 3A Exceeds 4000V
  - CDM JEDEC JS-002-2022 Class C3 Exceeds 1000V
- Latch-Up JESD78 200mA
- Integrated 10kΩ Pullup Resistors
- Packaging (Pb-Free & Green):
  - 12-Pin, 1.385mm x 1.035mm, 0.35mm pitch, U-WLB1014-12 (Type JC)
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/**

Applications

- I2C, SMBus, MDIO
- Low-voltage ASIC level translation
- Mobile phones, PDAs, cameras

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Pin Descriptions

Pin Number U-WLB1014-12 (Type JC)	Pin Name	Type	Description
B2	V_{CCA}	Power	A-port supply voltage. 0.72V ≤ V_{CCA} ≤ 1.98V.
A2	V_{CCB}	Power	B-port supply voltage. 1.65V ≤ V_{CCB} ≤ 5.5V.
A3	A1	I/O	Input/output A. Referenced to V_{CCA}.
B3	A2	I/O	Input/output A. Referenced to V_{CCA}.
C3	A3	I/O	Input/output A. Referenced to V_{CCA}.
D3	A4	I/O	Input/output A. Referenced to V_{CCA}.
A1	B1	I/O	Input/output B. Referenced to V_{CCB}.
B1	B2	I/O	Input/output B. Referenced to V_{CCB}.
C1	B3	I/O	Input/output B. Referenced to V_{CCB}.
D1	B4	I/O	Input/output B. Referenced to V_{CCB}.
C2	OE	Input	Output Enable (Active High). Pull OE Low to place all outputs in 3-state mode.
D2	GND	GND	Ground.

Functional Block Diagram

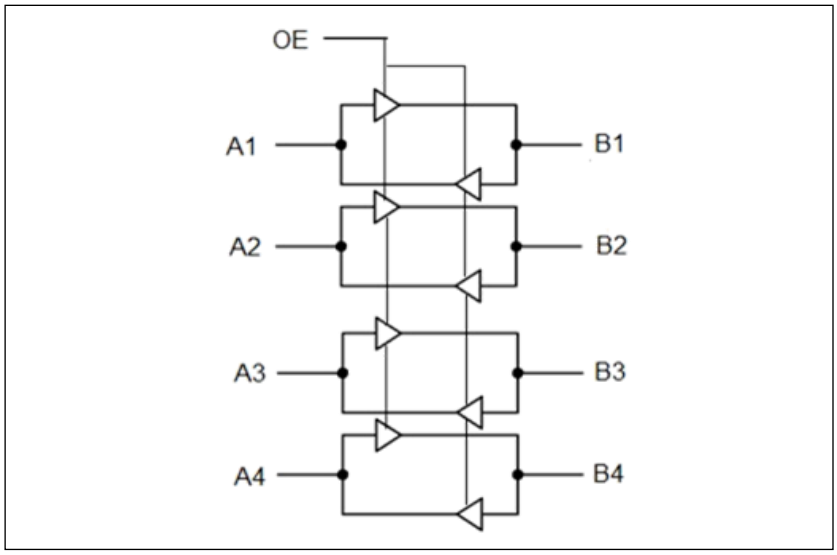


Figure 1. Block Diagram

Absolute Maximum Ratings (Note 4)

Symbol	Parameter	Rating	Unit
T_{STG}	Storage Temperature	-65 to +150	°C
V_{CCA}	DC Supply Voltage Port A	-0.5 to +2.5	V
V_{CCB}	DC Supply Voltage Port B	-0.5 to +6.5	V
V_{EN}	Enable Control DC Input Voltage	-0.3 to +6.5	V
V_{IOA}	Port A DC Input Voltage	-0.5 to +2.5	V
V_{IOB}	Port B DC Input Voltage	-0.5 to +6.5	V
I_O	Continuous Output Current	40	mA

Note: 4. Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to *Absolute Maximum Ratings* for extended periods can affect device reliability.

Recommended Operating Conditions

Symbol	Parameter		Min	Typ	Max	Unit
V_{CCA}	V_{CCA} Positive DC Supply Voltage		0.72	—	1.98	V
V_{CCB}	V_{CCB} Positive DC Supply Voltage		1.65	—	5.5	V
V_{EN}	Enable Control Pin Voltage		GND	—	5.5	V
V_{IOA}	Port A I/O Pin Voltage		GND	—	V_{CCA}	V
V_{IOB}	Port B I/O Pin Voltage		GND	—	V_{CCB}	V
$\Delta t/\Delta v$	Input Transition Rise or Fall Time	A or B port Push-Pull Driving, (V_{CCA} = 0.72V to 1.98V, V_{CCB} = 1.65V to 5.5V)	—	—	10	ns/V
		OE (V_{CCA} = 0.72V to 1.98V, V_{CCB} = 1.65V to 5.5V)	—	—	10	ns/V
T_A	Operating Temperature Range		-40	—	+85	°C

DC Electrical Characteristics (-40°C ≤ T_A ≤ +85°C, unless otherwise specified.) (Note 5)

Symbol	Parameter	Test Conditions	V_{CCA}	V_{CCB}	Min	Typ	Max	Unit
V_{IHB}	B Port Input HIGH Voltage	—	0.72V to 1.98V	1.65V to 5.5V	V_{CCB}*0.7	—	—	V
V_{ILB}	B Port Input LOW Voltage	—	0.72V to 1.98V	1.65V to 5.5V	—	—	0.15	V
V_{IHA}	A Port Input HIGH Voltage	—	0.72V to 1.98V	1.65V to 5.5V	V_{CCA}*0.7	—	—	V
V_{ILA}	A Port Input LOW Voltage	—	0.72V to 1.98V	1.65V to 5.5V	—	—	0.13	V
V_{IHOE}	Control Pin Input HIGH Voltage	—	0.91V to 1.98V	1.65V to 5.5V	V_{CCA} x 0.65	—	—	V
			0.72V to 0.9V	1.65V to 5.5V	V_{CCA} x 0.7	—	—	
V_{ILOE}	Control Pin Input LOW Voltage	—	0.72V to 1.98V	1.65V to 5.5V	—	—	V_{CCA} x 0.35	V
V_{OHB}	B Port Output HIGH Voltage	B port source current = -10µA	0.72V to 1.98V	1.65V to 5.5V	V_{CCB} x 0.8	—	—	V
V_{OLB}	B Port Output LOW Voltage	B port sink current = 1mA	0.72V to 1.98V	1.65V to 5.5V	—	—	0.3	V
V_{OHA}	A Port Output HIGH Voltage	A port source current = -10µA	0.72V to 1.98V	1.65V to 5.5V	V_{CCA} x 0.8	—	—	V
V_{OLA}	A Port Output LOW Voltage	A port sink current = 1mA	0.72V to 1.98V	1.65V to 5.5V	—	—	0.3	V
I_{QVCB}	V_{CCB} Supply Current	V_{IA} = V_{OA} = V_{CCA}, V_{IB} = V_{OB} = floating	0.72V to 1.98V	1.65V to 5.5V	—	—	24	µA
			1.98V	0	-1	—	—	
			0	5.5V	—	—	18	
I_{QVCA}	V_{CCA} Supply Current	V_{IA} = V_{OA} = V_{CCA}, V_{IB} = V_{OB} = floating	0.72V to 1.98V	1.65V to 5.5V	—	—	8.5	µA
			1.98V	0	—	—	4.7	
			0	5.5V	-1	—	—	
I_{ILA}	Port A Input Mode LOW Current (LXS0204L)	OE = V_{CCA}, V_{IAX} = 0, V_{OBX} = floating	0.72V to 1.98V	1.65V to 5.5V	—	—	±1	µA
I_{ILB}	Port B Input Mode LOW Current (LXS0204L)	OE = V_{CCA}, V_{IBX} = 0, V_{OAX} = floating			—	—	±1	µA
I_{OZ}	I/O Tri-State Output Mode Leakage Current	—	0.72V to 1.98V	1.65V to 5.5V	—	—	±2	µA
I_{OFF}	Power-Off Leakage Current	Port A	0	0V to 5.5V	—	—	±2.8	µA
		Port B	0V to 1.98V	0	—	—	±2	
R_{PU}	Pullup Resistors I/O	Port A	0.72V to 1.98V	1.65V to 5.5V	—	10	—	kΩ
		Port B			—	10	—	kΩ

Note: 5. All units are production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.

AC Electrical Characteristics (I/O test circuits, CLOAD = 15pF, driver output impedance ≤ 50Ω, RLOAD = 1MΩ, unless otherwise specified. For LXS0204L open-drain application, an external 2.2kΩ pullup resistor is placed between Port A and V_{CCA}. For LXS0204 open-drain application, no external 2.2kΩ pullup resistor is placed between Port A and V_{CCA}.)

V_{CCA} = 0.95V

Symbol	Parameter	Test Conditions	V_{CCB} = 1.8V		V_{CCB} = 3.3V		V_{CCB} = 5.0V		Unit
			Min	Max	Min	Max	Min	Max	
$t_{PHL-A-B}$	Propagation Delay	Push-pull driving	—	20	—	11.1	—	13.5	ns
		Open-drain driving (LXS0204)	—	5.3	—	9.4	—	13.8	
		Open-drain driving (LXS0204L)	—	5.5	—	9.5	—	13.5	
$t_{PLH-A-B}$		Push-pull driving	—	14.8	—	12.5	—	12.2	
		Open-drain driving (LXS0204)	—	58.6	—	36.3	—	29.2	
		Open-drain driving (LXS0204L)	—	42.1	—	38.2	—	37.2	
$t_{PHL-B-A}$	Propagation Delay	Push-pull driving	—	9.2	—	5.2	—	6.7	ns
		Open-drain driving (LXS0204)	—	3.9	—	4.5	—	4.9	
		Open-drain driving (LXS0204L)	—	3.3	—	3.6	—	4.0	
$t_{PLH-B-A}$		Push-pull driving	—	8.8	—	2.9	—	1.4	
		Open-drain driving (LXS0204)	—	3	—	3.3	—	4.6	
		Open-drain driving (LXS0204L)	—	3	—	3.3	—	4.6	
t_{en}	Enable Time	—	—	200	—	200	—	200	ns
t_{dis}	Disable Time	—	—	230	—	230	—	230	ns
t_{RB}	B Port Rise Time	Push-pull driving	2.6	17	0.5	14	0.42	20	ns
		Open-drain driving (LXS0204)	5.9	98.9	0.6	17.7	0.5	1.2	
		Open-drain driving (LXS0204L)	4.4	72.5	0.5	11.5	0.4	2.1	
t_{FB}	B Port Fall Time	Push-pull driving	1.6	14.2	2.8	13.8	3.2	24	ns
		Open-drain driving (LXS0204)	2.8	6.4	4.0	10.5	5.7	15.8	
		Open-drain driving (LXS0204L)	2.7	6.8	4.5	12	6.8	18.3	
t_{RA}	A Port Rise Time	Push-pull driving	1.7	15.3	2.2	15.1	1.8	11.1	ns
		Open-drain driving (LXS0204)	21	138.3	16.9	82.4	14.3	64.3	
		Open-drain driving (LXS0204L)	21.5	103	24.9	94.8	26.3	92.6	
t_{FA}	A Port Fall Time	Push-pull driving	0.9	18	0.7	9	0.6	9	ns
		Open-drain driving (LXS0204)	2.3	4.4	2.2	4.7	2.6	5.1	
		Open-drain driving (LXS0204L)	2.2	4.4	2.3	4.9	2.4	5.5	
t_{SKEW}	Channel-to-Channel Skew	Push-pull driving	—	1	—	1	—	1	ns
f_{DATA}	Maximum Data Rate	Push-pull driving	24	—	24	—	24	—	Mbps
		Open-drain driving	2	—	2	—	2	—	

AC Electrical Characteristics (I/O test circuits, CLOAD = 15pF, driver output impedance ≤ 50Ω, RLOAD = 1MΩ, unless otherwise specified. For LXS0204L open-drain application, an external 2.2kΩ pullup resistor is placed between Port A and V_{CCA}. For LXS0204 open-drain application, no external 2.2kΩ pullup resistor is placed between Port A and V_{CCA}.) (continued)

V_{CCA} = 1.2V

Symbol	Parameter	Test Conditions	V_{CCB} = 1.8V		V_{CCB} = 3.3V		V_{CCB} = 5.0V		Unit
			Min	Max	Min	Max	Min	Max	
$t_{PHL-A-B}$	Propagation Delay	Push-pull driving	—	5.1	—	8.2	—	11.9	ns
		Open-drain driving (LXS0204)	—	4.5	—	7.9	—	11.9	
		Open-drain driving (LXS0204L)	—	4.6	—	7.8	—	11.2	
$t_{PLH-A-B}$		Push-pull driving	—	7.4	—	4.1	—	3.7	
		Open-drain driving (LXS0204)	—	38.7	—	24.4	—	19.1	
		Open-drain driving (LXS0204L)	—	27.1	—	23.0	—	21.2	
$t_{PHL-B-A}$	Propagation Delay	Push-pull driving	—	4.0	—	4.5	—	5.8	ns
		Open-drain driving (LXS0204)	—	3.6	—	4.1	—	4.5	
		Open-drain driving (LXS0204L)	—	3.7	—	4.6	—	5.0	
$t_{PLH-B-A}$		Push-pull driving	—	6.7	—	0.4	—	0.3	
		Open-drain driving (LXS0204)	—	0.3	—	0.2	—	0.1	
		Open-drain driving (LXS0204L)	—	0.3	—	0.1	—	0.1	
t_{en}	Enable Time	—	—	200	—	200	—	200	ns
t_{dis}	Disable Time	—	—	230	—	230	—	230	ns
t_{RB}	B Port Rise Time	Push-pull driving	2.2	9.7	0.5	5.5	0.4	1.2	ns
		Open-drain driving (LXS0204)	5.8	93.7	0.6	18.9	0.5	1.2	
		Open-drain driving (LXS0204L)	4.3	64.3	0.5	15.3	0.4	1.2	
t_{FB}	B Port Fall Time	Push-pull driving	2.3	5.8	3.0	13.1	4.5	15.4	ns
		Open-drain driving (LXS0204)	2.3	5.7	3.0	9.7	4.3	14.7	
		Open-drain driving (LXS0204L)	2.3	5.7	3.0	9.7	4.3	14.7	
t_{RA}	A Port Rise Time	Push-pull driving	2.0	8.6	1.7	4.0	1.7	3.8	ns
		Open-drain driving (LXS0204)	15.7	122.2	13.7	71.1	12.1	52.0	
		Open-drain driving (LXS0204L)	14.5	84.7	16.8	76.3	20.0	74.0	
t_{FA}	A Port Fall Time	Push-pull driving	2.1	4.6	2.1	4.8	2.2	5.4	ns
		Open-drain driving (LXS0204)	2.3	4.3	2.2	4.4	2.2	4.7	
		Open-drain driving (LXS0204L)	2.1	4.5	2.2	4.9	2.2	5.4	
t_{SKEW}	Channel-to-Channel Skew	Push-pull driving	—	1	—	1	—	1	ns
f_{DATA}	Maximum Data Rate	Push-pull driving	24	—	24	—	24	—	Mbps
		Open-drain driving	2	—	2	—	2	—	

AC Electrical Characteristics (I/O test circuits, CLOAD = 15pF, driver output impedance ≤ 50Ω, RLOAD = 1MΩ, unless otherwise specified. For LXS0204L open-drain application, an external 2.2kΩ pullup resistor is placed between Port A and V_{CCA}. For LXS0204 open-drain application, no external 2.2kΩ pullup resistor is placed between Port A and V_{CCA}.) (continued)

V_{CCA} = 1.8V

Symbol	Parameter	Test Conditions	V_{CCB} = 3.3V		V_{CCB} = 5.0V		Unit
			Min	Max	Min	Max	
$t_{PHL-A-B}$	Propagation Delay	Push-pull driving	—	5.4	—	6.8	ns
		Open-drain driving (LXS0204)	—	4.7	—	6.9	
		Open-drain driving (LXS0204L)	—	9.6	—	10	
$t_{PLH-A-B}$		Push-pull driving	—	7.1	—	7.5	
		Open-drain driving (LXS0204)	—	208	—	198	
		Open-drain driving (LXS0204L)	—	208	—	198	
$t_{PHL-B-A}$	Propagation Delay	Push-pull driving	—	4.5	—	5.5	ns
		Open-drain driving (LXS0204)	—	3.4	—	3.7	
		Open-drain driving (LXS0204L)	—	4.4	—	4	
$t_{PLH-B-A}$		Push-pull driving	—	4.5	—	0.5	
		Open-drain driving (LXS0204)	—	140	—	102	
		Open-drain driving (LXS0204L)	—	140	—	102	
t_{en}	Enable Time	—	—	200	—	200	ns
t_{dis}	Disable Time	—	—	230	—	230	ns
t_{RB}	B Port Rise Time	Push-pull driving	1.08	9.1	0.46	7.6	ns
		Open-drain driving (LXS0204)	0.56	106	0.44	58	
		Open-drain driving (LXS0204L)	0.56	106	0.44	58	
t_{FB}	B Port Fall Time	Push-pull driving	2.1	16.2	2.8	16.2	ns
		Open-drain driving (LXS0204)	2.1	16.2	2.7	16.2	
		Open-drain driving (LXS0204L)	2.1	16.2	2.7	16.2	
t_{RA}	A Port Rise Time	Push-pull driving	1.4	9.3	1.4	7.6	ns
		Open-drain driving (LXS0204)	3.5	132	3.3	95	
		Open-drain driving (LXS0204L)	3.5	132	3.3	95	
t_{FA}	A Port Fall Time	Push-pull driving	1.9	6	1.7	13.3	ns
		Open-drain driving (LXS0204)	2	6.4	2	6.1	
		Open-drain driving (LXS0204L)	2	6.4	2	6.1	
t_{SKEW}	Channel-to-Channel Skew	Push-pull driving	—	1	—	1	ns
f_{DATA}	Maximum Data Rate	Push-pull driving	24	—	24	—	Mbps
		Open-drain driving	2	—	2	—	

Test Circuits

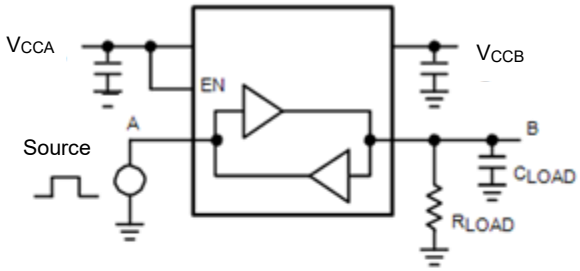


Figure 2. Rail-to-Rail Driving A

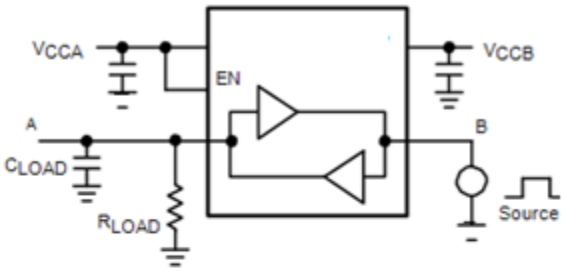


Figure 3. Rail-to-Rail Driving B

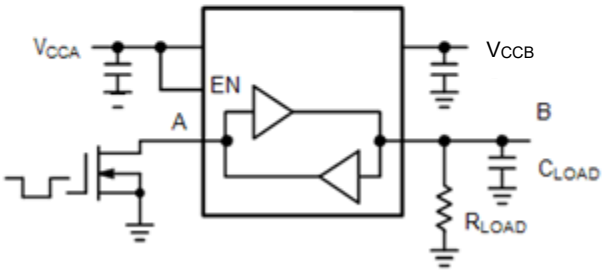


Figure 4. Open-Drain Driving A

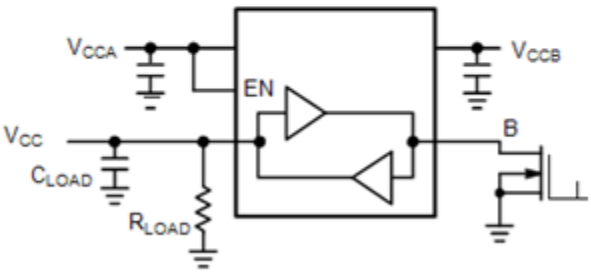
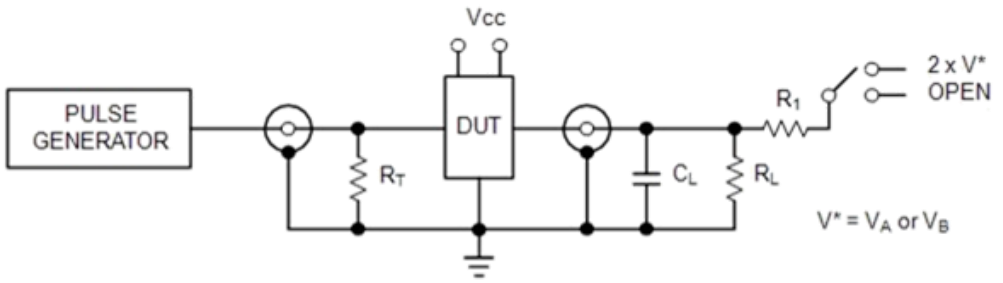


Figure 5. Open-Drain Driving B

Test Circuits (continued)



Test	Switch
t_{PZH}, t_{PHZ}	Open
t_{PZL}, t_{PLZ}	2 x V*

C_L = 15 pF or equivalent (Includes jig and probe capacitance)
R_L = R_1 = 50 kΩ or equivalent
R_T = Z_{OUT} of pulse generator (typically 50 Ω)
V* = V_A or V_B for A or B measurements, respectively.

Figure 6. Test Circuit for Enable/Disable Time Measurement

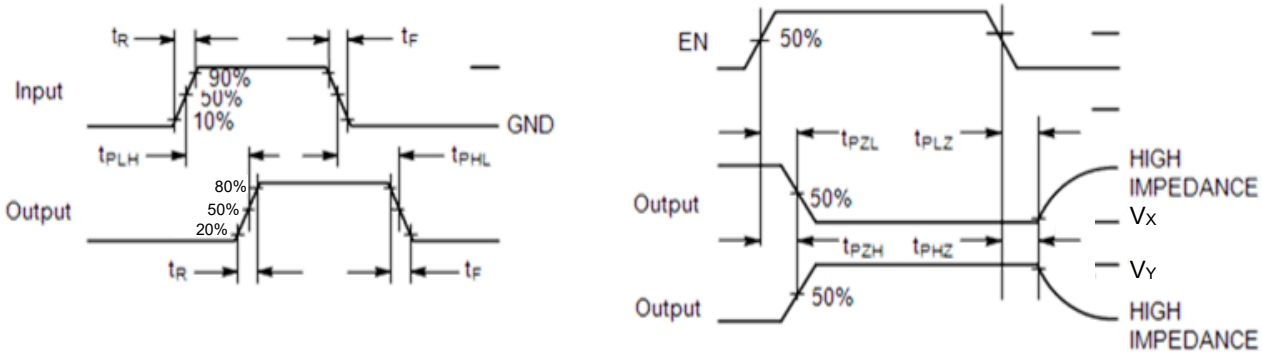


Figure 7. Timing Definitions for Propagation Delays and Enable/Disable Measurement

Definition of V_X and V_Y

Supply Voltage	Output	
V_{CCO}	V_X	V_Y
0.72V	V_{OL} + 0.1V	V_{OH} – 0.1V
0.95V	V_{OL} + 0.1V	V_{OH} – 0.1V
1.2V +/- 0.12V	V_{OL} + 0.1V	V_{OH} – 0.1V
1.8V +/- 0.15V	V_{OL} + 0.15V	V_{OH} – 0.15V
2.5V +/- 0.2V	V_{OL} + 0.15V	V_{OH} – 0.15V
3.3V +/- 0.3V	V_{OL} + 0.3V	V_{OH} – 0.3V
5V +/- 0.5V	V_{OL} + 0.3V	V_{OH} – 0.3V

Functional Description

Level Translator Architecture

The LXS0204/LXS0204L is a 4-bit configurable, dual-supply, bi-directional, auto-sensing translator that does not require a directional control pin. The A-port operating voltage range is from 0.72V to 1.98V, and the B-port operating voltage range is from 1.65V to 5.5V.

The translator has integrated a 10kΩ pullup resistor on port A and port B. The integrated pullup resistors are used to pull the I/O lines to either V_{CCA} or V_{CCB}. When OE goes low, the pullup resistors are disabled. There is an nMOS transistor that connects the A port and B port. When either A port or B port is pulled low externally, the nMOS transistor will turn on and pull the other port low. When both A port and B port are not pulled low externally, the pullup resistors will pull both ports to their corresponding VCC. In addition, each output has integrated a one-shot rising-edge detector to turn on the pMOS transistor within a short duration to improve the low-to-high transition.

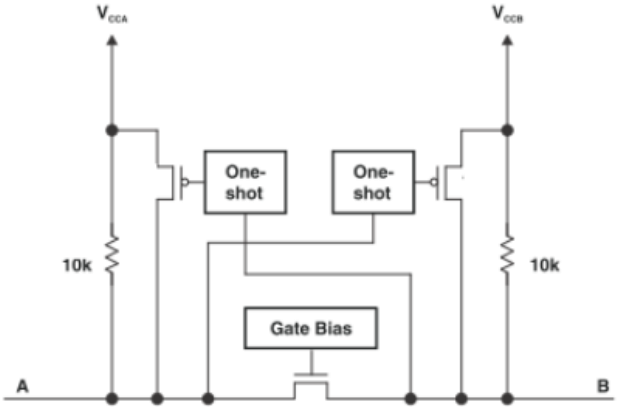


Figure 8. Architecture

Pullup Resistors

The translator has integrated two pullup resistors at both ports A and B of each channel to maintain the logic-high level at V_{CCA} or V_{CCB} if no external pulldown driver turns on. The pullup resistors are also responsible to pull up the ports initially before the internal one-shot pMOS transistors turn on.

The LXS0204L has an additional feature in which the internal pullup resistors are disabled during a logic-low level on Port A or Port B. This reduces the static power consumption during a logic-low state. The internal pullup resistors are re-enabled during a logic-high level on Port A and or Port B. Please note that using the LXS0204L in open-drain applications requires the use of external pullup resistors to initially pull the ports high. This is because the LXS0204L's internal pullup resistors are disabled during a logic-low state and are not available to pull the ports HIGH themselves. Using the LXS0204L in push-pull applications does not require the use of external pullup resistors.

Input Driver Requirements

The rise (t_R) and fall (t_F) timing parameters of the open-drain outputs depend on the magnitude of the pullup resistors. In addition, the propagation time (t_{PD}) and maximum data rate depend on the impedance of the device that is connected to the translator. The timing parameters and DC output voltages listed in the data sheet assume that the output impedance of the drivers connected to the translator is less than 50Ω and no external pullup resistors are connected. Drivers with lower output impedance may be needed in order to maintain low V_{OL} if small external pullup resistors are used.

Output Enable (OE)

The LXS0204/LXS0204L has an Output Enable pin (OE) that enables the device by setting HIGH. Driving the Output Enable pin to a low logic level minimizes the power consumption of the device and sets all I/Os in high-impedance OFF state. Normal translation operation occurs when the OE pin is equal to a logic-high signal. The OE pin is referenced to the V_{CCA} supply and can tolerate the V_{CCB} voltage.

Power Supply Guidelines

During normal operation, supply voltage V_{CCA} must be less than or equal to V_{CCB}. The sequencing of the power supplies will not damage the device during the power-up operation. For optimal performance, 0.01µF to 0.1µF decoupling capacitors should be used on the V_{CCA} and V_{CCB} power supply pins. Ceramic capacitors are a good design choice to filter and bypass any noise signals on the voltage lines to the ground plane of the PCB. The noise immunity will be maximized by placing the capacitors as close as possible to the supply and ground pins, along with minimizing the PCB connection traces.

Ordering Information

LXS0204 X X – X

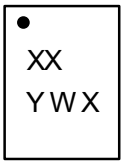
Feature	Package	Packing
(Blank): Static Internal Rpu L: Disable Internal Rpu During Logic-Low	CBA12: U-WLB1014-12 (Type JC)	7: Tape & Reel

Orderable Part Number	Feature	Package	Package Code	Packing	
				Qty.	Carrier
LXS0204CBA12-7	Static Internal Pullup Resistors	U-WLB1014-12 (Type JC)	CBA12	3,000	Tape & Reel
LXS0204LCBA12-7	Disable Internal Pullup Resistors During Logic-Low	U-WLB1014-12 (Type JC)	CBA12	3,000	Tape & Reel

Marking Information

U-WLB1014-12 (Type JC)

(Top View)



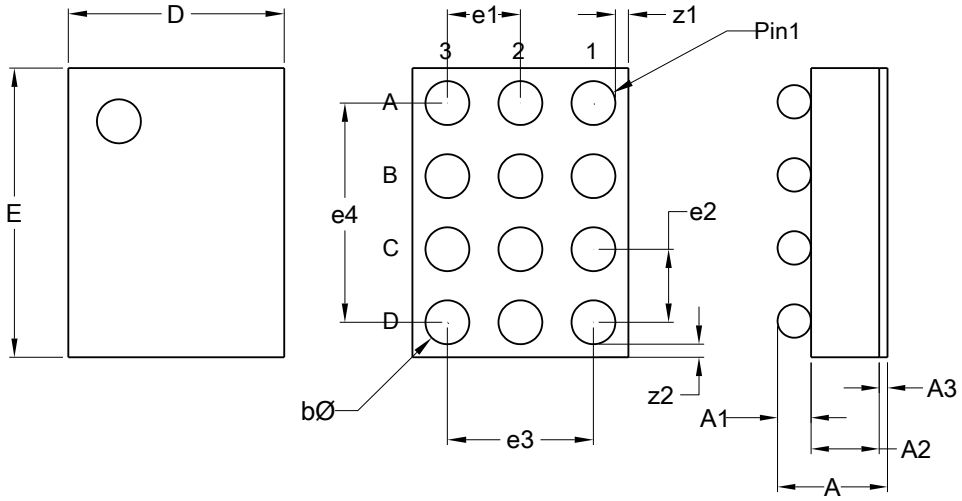
XX : Identification Code
Y : Year : 0~9
W : Week : A~Z : week 1~26 ;
a~z : week 27~52; z represents week 52 and 53
X : Internal Code

Orderable Part Number	Package	Identification Code
LXS0204CBA12-7	U-WLB1014-12 (Type JC)	P2
LXS0204LCBA12-7	U-WLB1014-12 (Type JC)	P5

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-WLB1014-12 (Type JC)

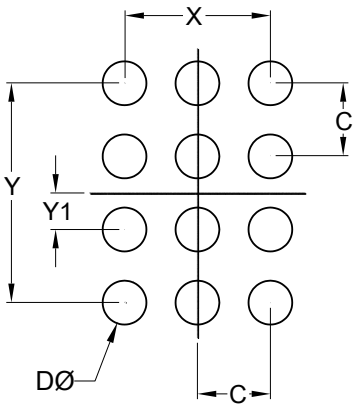


U-WLB1014-12 (Type JC)			
Dim	**Min**	**Max**	**Typ**
A	0.489	0.565	0.527
A1	0.140	0.180	0.160
A2	0.313	0.339	0.326
A3	0.035	0.045	0.040
b	0.191	0.231	0.211
D	1.020	1.050	1.035
E	1.370	1.400	1.385
e1	--	--	0.350
e2	--	--	0.350
e3	--	--	0.700
e4	--	--	1.050
z1	--	--	0.063
z2	--	--	0.063
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-WLB1014-12 (Type JC)



Dimensions	Value (in mm)
C	0.350
D	0.211
X	0.700
Y	1.050
Y1	0.175

Mechanical Data

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: SnAgCu Balls, Solderable per MIL-STD-202, Method 208 e1
- Weight: 0.00295 grams (Approximate)

IMPORTANT NOTICE

1. DIODES INCORPORATED (Diodes) AND ITS SUBSIDIARIES MAKE NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARDS TO ANY INFORMATION CONTAINED IN THIS DOCUMENT, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION).

2. The Information contained herein is for informational purpose only and is provided only to illustrate the operation of Diodes' products described herein and application examples. Diodes does not assume any liability arising out of the application or use of this document or any product described herein. This document is intended for skilled and technically trained engineering customers and users who design with Diodes' products. Diodes' products may be used to facilitate safety-related applications; however, in all instances customers and users are responsible for (a) selecting the appropriate Diodes products for their applications, (b) evaluating the suitability of Diodes' products for their intended applications, (c) ensuring their applications, which incorporate Diodes' products, comply the applicable legal and regulatory requirements as well as safety and functional-safety related standards, and (d) ensuring they design with appropriate safeguards (including testing, validation, quality control techniques, redundancy, malfunction prevention, and appropriate treatment for aging degradation) to minimize the risks associated with their applications.

3. Diodes assumes no liability for any application-related information, support, assistance or feedback that may be provided by Diodes from time to time. Any customer or user of this document or products described herein will assume all risks and liabilities associated with such use, and will hold Diodes and all companies whose products are represented herein or on Diodes' websites, harmless against all damages and liabilities.

4. Products described herein may be covered by one or more United States, international or foreign patents and pending patent applications. Product names and markings noted herein may also be covered by one or more United States, international or foreign trademarks and trademark applications. Diodes does not convey any license under any of its intellectual property rights or the rights of any third parties (including third parties whose products and services may be described in this document or on Diodes' website) under this document.

5. Diodes' products are provided subject to Diodes' Standard Terms and Conditions of Sale (https://www.diodes.com/about/company/terms-and-conditions/terms-and-conditions-of-sales/) or other applicable terms. This document does not alter or expand the applicable warranties provided by Diodes. Diodes does not warrant or accept any liability whatsoever in respect of any products purchased through unauthorized sales channel.

6. Diodes' products and technology may not be used for or incorporated into any products or systems whose manufacture, use or sale is prohibited under any applicable laws and regulations. Should customers or users use Diodes' products in contravention of any applicable laws or regulations, or for any unintended or unauthorized application, customers and users will (a) be solely responsible for any damages, losses or penalties arising in connection therewith or as a result thereof, and (b) indemnify and hold Diodes and its representatives and agents harmless against any and all claims, damages, expenses, and attorney fees arising out of, directly or indirectly, any claim relating to any noncompliance with the applicable laws and regulations, as well as any unintended or unauthorized application.

7. While efforts have been made to ensure the information contained in this document is accurate, complete and current, it may contain technical inaccuracies, omissions and typographical errors. Diodes does not warrant that information contained in this document is error-free and Diodes is under no obligation to update or otherwise correct this information. Notwithstanding the foregoing, Diodes reserves the right to make modifications, enhancements, improvements, corrections or other changes without further notice to this document and any product described herein. This document is written in English but may be translated into multiple languages for reference. Only the English version of this document is the final and determinative format released by Diodes.

8. Any unauthorized copying, modification, distribution, transmission, display or other use of this document (or any portion hereof) is prohibited. Diodes assumes no responsibility for any losses incurred by the customers or users or any third parties arising from any such unauthorized use.

9. This Notice may be periodically updated with the most recent version available at https://www.diodes.com/about/company/terms-and-conditions/important-notice

www.diodes.com