



80V +175°C N-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary

BV _{DSS}	R _{DS(ON)} Max	I _D Max T _A = +25°C
901/	22mΩ @ V _{GS} = 10V	5A
80V	38mΩ @ V _{GS} = 4.5V	4A

Features and Benefits

- 100% Unclamped Inductive Switching (UIS) Test in Production Ensures More Reliable and Robust End Application
- Thermally Efficient Package Cooler Running Applications
- High Conversion Efficiency
- Low R_{DS(ON)} Minimizes On-State Losses
- Low Input Capacitance
- Fast Switching Speed
- < 1.1mm Package Profile Ideal for Thin Applications
- Lead-Free Finish; RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- An automotive-compliant part is available under a separate datasheet (<u>DMTH8022LFDFWQ</u>)

Description and Applications

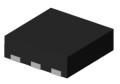
This new generation MOSFET is designed to minimize the on-state resistance (R_{DS(ON)}) yet maintain superior switching performance, making it ideal for high-efficiency power-management applications.

- Power-management functions
- Battery-operated systems and solid-state relays
- Drivers: relays, solenoids, lamps, hammers, displays, memories, transistors, etc.

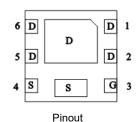
Mechanical Data

- Package: U-DFN2020-6
- Package Material: Molded Plastic, "Green" Molding Compound.
 UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish Matte Tin Solderable per MIL-STD-202, Method 208 (e3)
- Weight: 0.008 grams (Approximate)

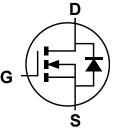
U-DFN2020-6/SWP (Type F)







Bottom View



Top View

Bottom View

Internal Schematic

Ordering Information (Note 4)

Orderable Part Number	Package	Packing		
Orderable Part Number	Package	Qty.	Carrier	
DMTH8022LFDFW-7	U-DFN2020-6/SWP (Type F)	3,000	Reel	
DMTH8022LFDFW-13	U-DFN2020-6/SWP (Type F)	10,000	Reel	

Notes:

- 1. EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant. All applicable RoHS exemptions applied.
- 2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.



Marking Information



80 = Product Type Marking Code YM = Date Code Marking Y = Year (ex: M = 2025) M = Month (ex: 2 = February)

Date Code Key

Year	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036
Code	М	N	Р	R	S	Т	U	V	W	Х	Υ	Z
Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	0	N	D

Maximum Ratings (@TA = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit	
Drain-Source Voltage	V_{DSS}	80	V	
Gate-Source Voltage	V_{GSS}	±20	V	
Continuous Drain Current, V _{GS} = 10V (Note 5)	T _A = +25°C T _A = +100°C	Ιο	5 3.5	А
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)	I _{DM}	52	Α	
Maximum Body Diode Continuous Current (Note 5)	ls	3.4	Α	
Pulsed Body Diode Current (10µs Pulse, Duty Cycle = 1%	lsм	52	Α	
Avalanche Current, L = 1mH	las	8.7	Α	
Avalanche Energy, L = 1mH	Eas	39	mJ	

Thermal Characteristics (@TA = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Total Power Dissipation (Note 6)	P _D	1.16	W
Thermal Resistance, Junction to Ambient (Note 6)	Reja	129	°C/W
Total Power Dissipation (Note 5)	PD	2.5	W
Thermal Resistance, Junction to Ambient (Note 5)	RθJA	60	°C/W
Operating and Storage Temperature Range	TJ, TSTG	-55 to +175	°C

Notes:

^{5.} Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.6. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.



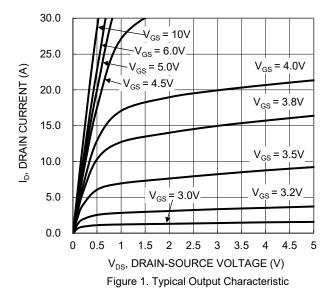
Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition	
OFF CHARACTERISTICS (Note 7)							
Drain-Source Breakdown Voltage	BV _{DSS}	80	_	_	V	V _{GS} = 0, I _D = 1mA	
Zero Gate Voltage Drain Current	IDSS	-	-	1	μA	V _{DS} = 64V, V _{GS} = 0	
Gate-Source Leakage	Igss	-	-	±100	nA	$V_{GS} = \pm 20V, V_{DS} = 0$	
ON CHARACTERISTICS (Note 7)							
Gate Threshold Voltage	Vgs(TH)	1.3	_	2.5	V	V _{DS} = V _{GS} , I _D = 250μA	
Static Drain-Source On-Resistance	D	_	16	22	mΩ	V _{GS} = 10V, I _D = 5A	
Static Drain-Source On-Resistance	R _{DS(ON)}	_	25	38	11122	$V_{GS} = 4.5V, I_D = 4A$	
Diode Forward Voltage	VsD	-	0.8	1.0	V	V _{GS} = 0, I _S = 10A	
DYNAMIC CHARACTERISTICS (Note 8)							
Input Capacitance	C _{iss}	_	591	_	pF	.,	
Output Capacitance	Coss	ı	214	_	n- I	$V_{DS} = 40V$, $V_{GS} = 0$ f = 1MHz	
Reverse Transfer Capacitance	Crss	_	15	_	pF	1 - 1101112	
Gate Resistance	Rg	_	1.38	_	Ω	V _{DS} = 0, V _{GS} = 0, f = 1MHz	
Total Gate Charge (V _{GS} = 4.5V)	Qg	-	5.6	_	nC		
Total Gate Charge (V _{GS} = 10V)	Qg	ı	11.3	_	nC	V _{DS} = 40V. I _D = 7.5A	
Gate-Source Charge	Qgs	ı	2.6	_	nC	VDS - 40V, ID - 7.5A	
Gate-Drain Charge	Q_{gd}	_	2.3	_	nC		
Turn-On Delay Time	t _{D(ON)}	_	13	_	ns		
Turn-On Rise Time	t _R	-	34	_	ns	V _{DD} = 40V	
Turn-Off Delay Time	t _{D(OFF)}	_	11	_	ns	$V_{GS} = 4.5V, R_g = 2.7\Omega$ $I_D = 10A$	
Turn-Off Fall Time	tϝ	_	13	_	ns		
Reverse-Recovery Time	t _{RR}	_	24	_	ns	I 7 FA di/dt _ 100 A/us	
Reverse-Recovery Charge	Qrr	_	14	_	nC	I _F = 7.5A, di/dt = 100A/μs	

Notes:

^{7.} Short duration pulse test used to minimize self-heating effect. 8. Guaranteed by design. Not subject to product testing.





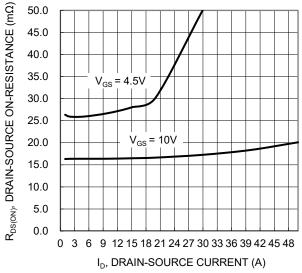


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

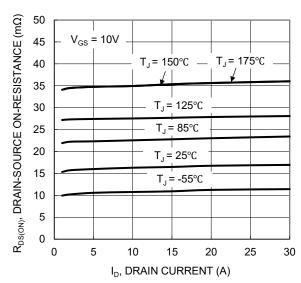


Figure 5. Typical On-Resistance vs. Drain Current and Temperature

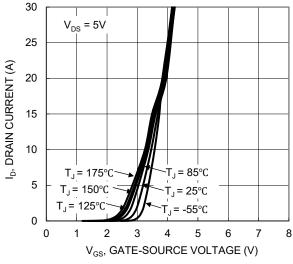


Figure 2. Typical Transfer Characteristic

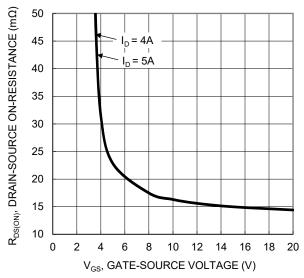


Figure 4. Typical Transfer Characteristic

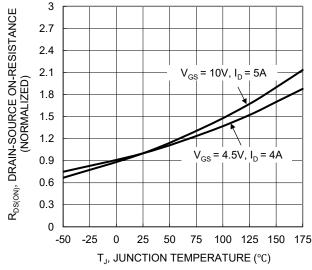


Figure 6. On-Resistance Variation with Temperature



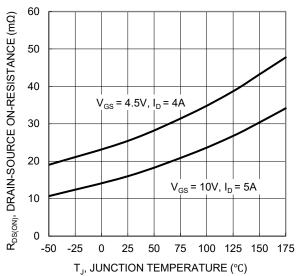


Figure 7. On-Resistance Variation with Temperature

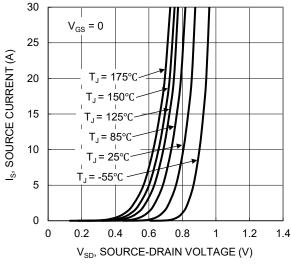


Figure 9. Diode Forward Voltage vs. Current

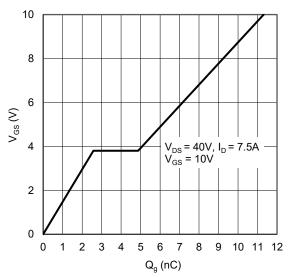


Figure 11. Gate Charge

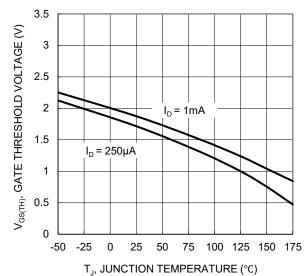


Figure 8. Gate Threshold Variation vs. Junction Temperature

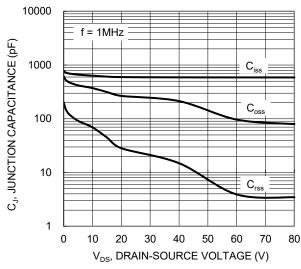


Figure 10. Typical Junction Capacitance

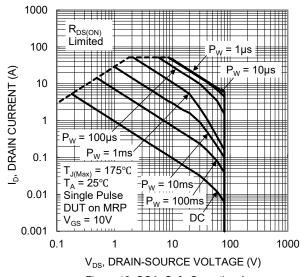


Figure 12. SOA, Safe Operation Area



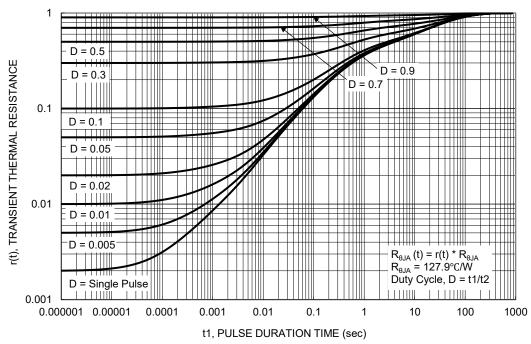


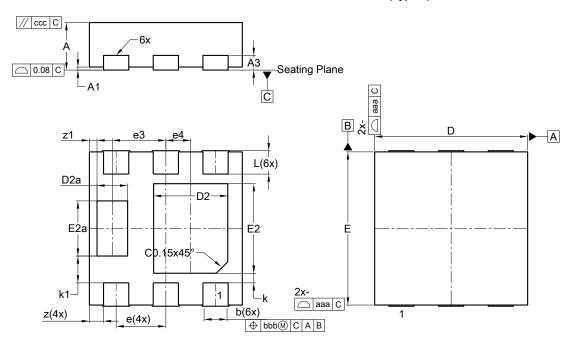
Figure 13. Transient Thermal Resistance



Package Outline Dimension

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-DFN2020-6/SWP (Type F)

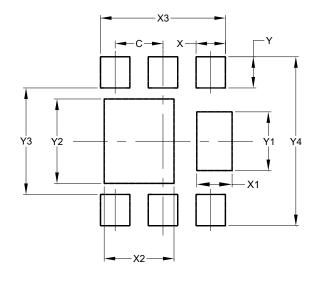


U-DFN2020-6/SWP (Type F)						
Dim	Min	Тур				
Α	0.59	0.65	0.62			
A1	0.00	0.05	0.03			
А3	-	-	0.192			
b	0.28	0.38	0.33			
D	1.95	2.05	2.00			
D2	0.87	1.07	0.97			
D2a	0.35	0.45	0.40			
Е	1.95	2.05	2.00			
E2	1.07	1.27	1.17			
E2a	0.67	0.77	0.72			
е	0.65 BSC					
е3	0.70 BSC					
e4	0	.325 BS	С			
k			0.125			
k1			0.35			
L	0.225	0.355	0.305			
Z	ı	ı	0.185			
z1	-	-	0.10			
aaa	0.250					
bbb	0.100					
CCC	0.100					
All Dimensions in mm						

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-DFN2020-6/SWP (Type F)



Dimensions	Value (in mm)		
С	0.650		
X	0.400		
X1	0.480		
X2	0.950		
Х3	1.700		
Y	0.425		
Y1	0.800		
Y2	1.150		
Y3	1.450		
Y4	2.300		



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