

Product Summary

BV _{DSS}	R _{DS(ON)} Max	I _D T _C = +25°C
60V	5.0mΩ @ V _{GS} = 10V	90A
	7.8mΩ @ V _{GS} = 4.5V	74A

Description and Applications

This MOSFET is designed to minimize the on-state resistance (R_{DS(ON)}) yet maintain superior switching performance, making it ideal for high-efficiency power-management applications.

- Wireless charging
- DC-DC converters
- Power managements

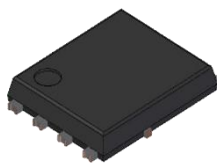
Features and Benefits

- Rated to +175°C – Ideal for High Ambient Temperature Environments
- 100% Unclamped Inductive Switching (UIS) Test in Production – Ensures More Reliable and Robust End Applications
- High Conversion Efficiency
- Low R_{DS(ON)} – Minimizes On-State Losses
- Low Input Capacitance
- Fast Switching Speed
- Wettable Flank for Improved Optical Inspection
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **The DMTH64M2LPDWQ is suitable for automotive applications requiring specific change control; this part is AEC-Q101 qualified, PPAP capable, and manufactured in IATF 16949 certified facilities.**
<https://www.diodes.com/quality/product-definitions/>

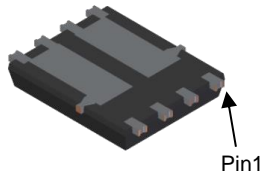
Mechanical Data

- Package: PowerDI®5060-8
- Package Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Finish – Matte Tin Annealed over Copper Leadframe; Solderable per MIL-STD-202, Method 208 @3
- Weight: 0.097 grams (Approximate)

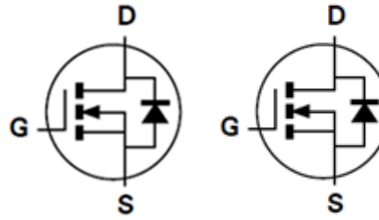
PowerDI5060-8/SWP (Type UXD)



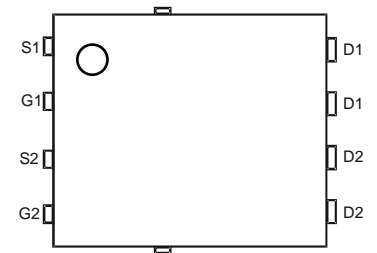
Top View



Bottom View



Internal Schematic



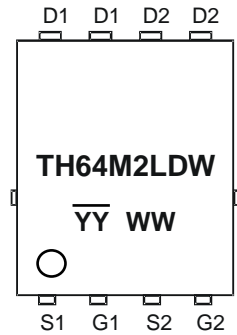
Top View
Pin Configuration

Ordering Information (Note 4)

Orderable Part Number	Package	Packing	
		Qty.	Carrier
DMTH64M2LPDWQ-13	PowerDI5060-8/SWP (Type UXD)	2500	Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
 2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

Marking Information



D11 = Manufacturer's Marking
 TH64M2LDW = Product Type Marking Code
 YYWW = Date Code Marking
 YY = Last Two Digits of Year (ex: 25 = 2025)
 WW = Week Code (01 to 53)

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Drain-Source Voltage		V _{DSS}	60	V
Gate-Source Voltage		V _{GSS}	±20	V
Continuous Drain Current, V _{GS} = 10V (Note 5)	T _A = +25°C	I _D	18	A
	T _A = +100°C		13	
Continuous Drain Current, V _{GS} = 10V (Note 6)	T _C = +25°C	I _D	90	A
	T _C = +100°C		64	
Pulsed Drain Current (10μs Pulse, Duty Cycle = 1%)		I _{DM}	360	A
Maximum Continuous Body Diode Forward Current (Note 6)		I _S	90	A
Pulsed Body Diode Forward Current (10μs Pulse, Duty Cycle = 1%)		I _{SM}	360	A
Avalanche Current, L = 0.1mH		I _{AS}	49	A
Avalanche Energy, L = 0.1mH		E _{AS}	125	mJ

Thermal Characteristics

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)	T _A = +25°C	P _D	2.9	W
Thermal Resistance, Junction to Ambient (Note 5)		R _{θJA}	51	°C/W
Total Power Dissipation (Note 6)	T _C = +25°C	P _D	74	W
Thermal Resistance, Junction to Case (Note 6)		R _{θJC}	2.04	°C/W
Operating and Storage Temperature Range		T _J , T _{STG}	-55 to +175	°C

Notes: 5. Device mounted on FR-4 substrate PC board, 2oz. copper, with thermal bias to bottom layer 1inch square copper plate.
 6. Thermal resistance from junction to soldering point (on the exposed drain pad).

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV _{DSS}	60	—	—	V	V _{GS} = 0, I _D = 250μA
Zero Gate Voltage Drain Current	I _{DSS}	—	—	1	μA	V _{DS} = 48V, V _{GS} = 0
Gate-Source Leakage	I _{GSS}	—	—	±100	nA	V _{GS} = ±20V, V _{DS} = 0
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	V _{GS(TH)}	1.2	—	2.2	V	V _{DS} = V _{GS} , I _D = 250μA
Static Drain-Source On-Resistance	R _{DS(ON)}	—	3.9	5.0	mΩ	V _{GS} = 10V, I _D = 20A
		—	5.4	7.8		V _{GS} = 4.5V, I _D = 20A
Diode Forward Voltage	V _{SD}	—	0.8	1.2	V	V _{GS} = 0, I _S = 20A
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C _{iss}	—	2963	—	pF	V _{DS} = 30V, V _{GS} = 0, f = 1MHz
Output Capacitance	C _{oss}	—	1070	—		
Reverse Transfer Capacitance	C _{rss}	—	68	—		
Gate Resistance	R _g	—	0.97	—	Ω	V _{DS} = 0, V _{GS} = 0, f = 1MHz
Total Gate Charge (V _{GS} = 10V)	Q _g	—	48	—	nC	V _{DD} = 30V, I _D = 13.5A
Total Gate Charge (V _{GS} = 4.5V)	Q _g	—	25	—		
Gate-Source Charge	Q _{gs}	—	8.5	—		
Gate-Drain Charge	Q _{gd}	—	7.2	—		
Turn-On Delay Time	t _{D(ON)}	—	5.2	—	ns	V _{GS} = 10V, V _{DD} = 30V, R _G = 6Ω, I _D = 13.5A
Turn-On Rise Time	t _r	—	22	—		
Turn-Off Delay Time	t _{D(OFF)}	—	55	—		
Turn-Off Fall Time	t _f	—	38	—		
Reverse-Recovery Time	t _{RR}	—	56	—	ns	I _F = 13.5A, di/dt = 300A/μs
Reverse-Recovery Charge	Q _{RR}	—	141	—	nC	

Notes: 7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to product testing.

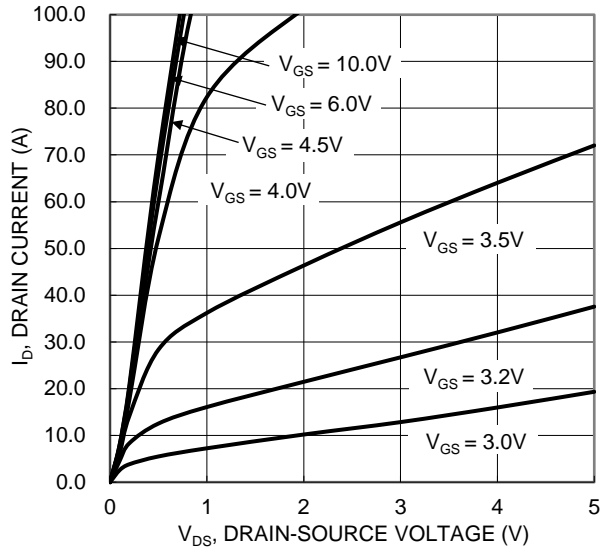


Figure 1. Typical Output Characteristic

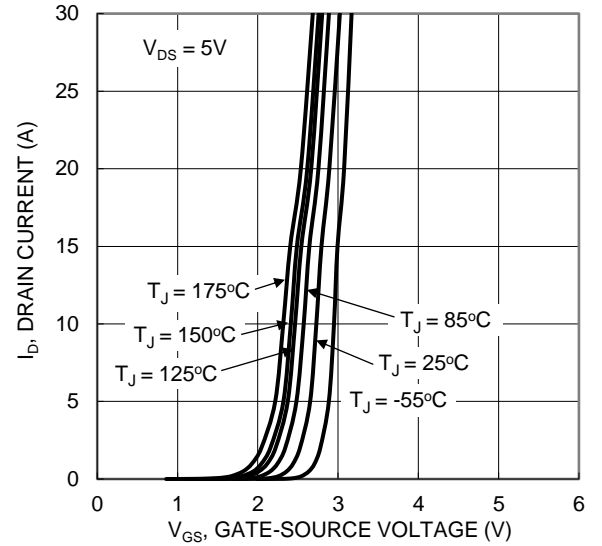


Figure 2. Typical Transfer Characteristic

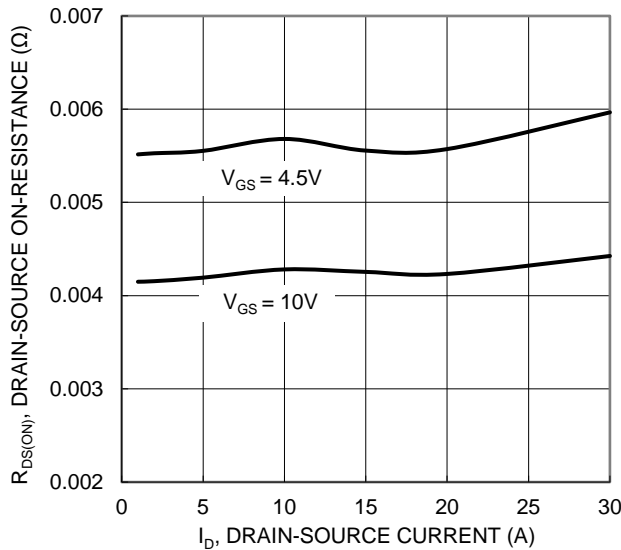


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

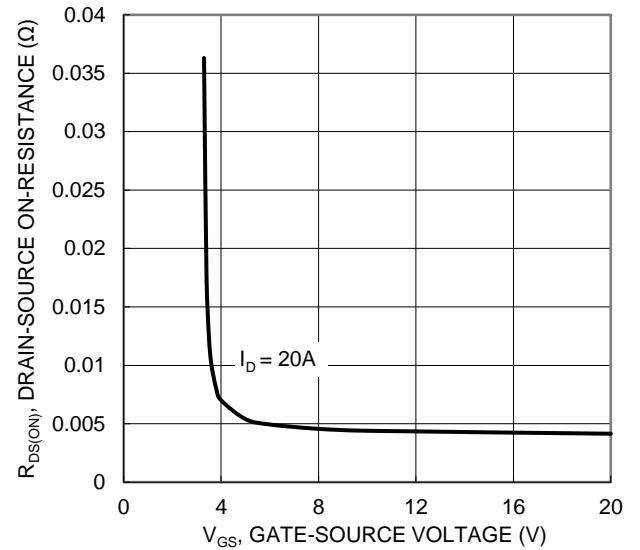


Figure 4. Typical Transfer Characteristic

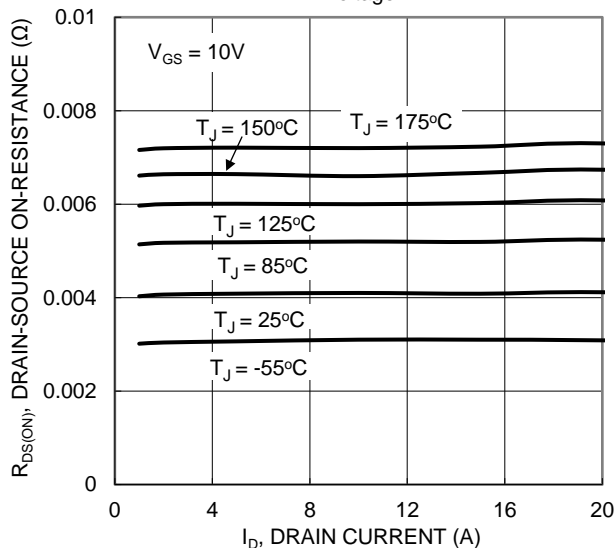


Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature

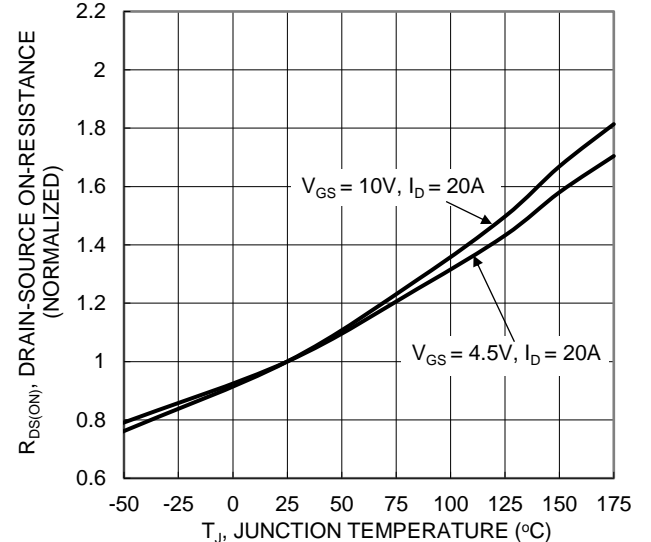


Figure 6. On-Resistance Variation with Junction Temperature

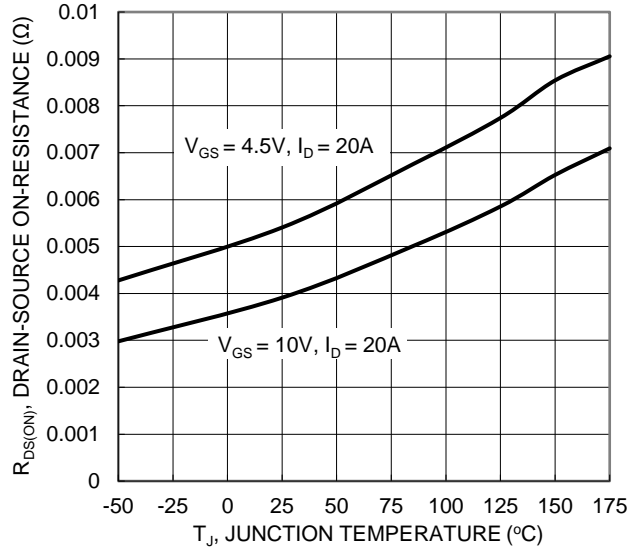


Figure 7. On-Resistance Variation with Junction Temperature

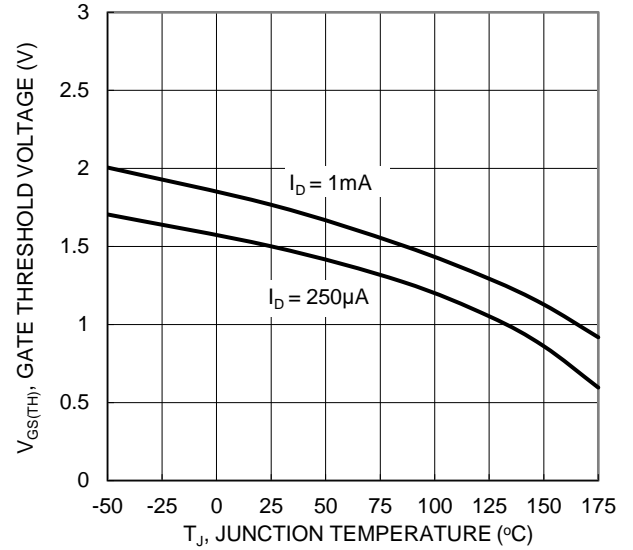


Figure 8. Gate Threshold Variation vs. Junction Temperature

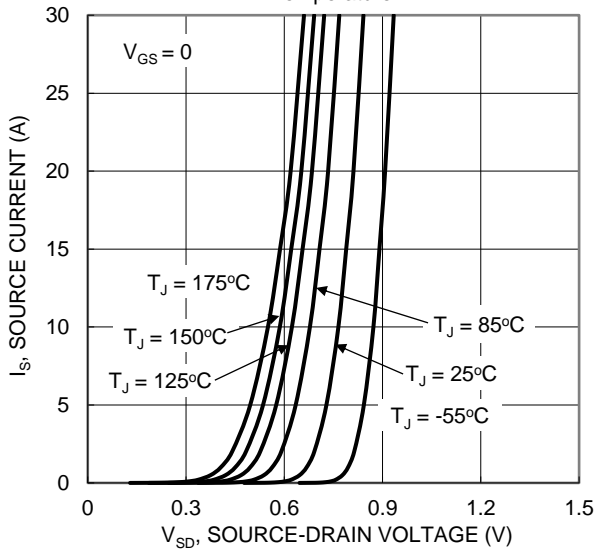


Figure 9. Diode Forward Voltage vs. Current

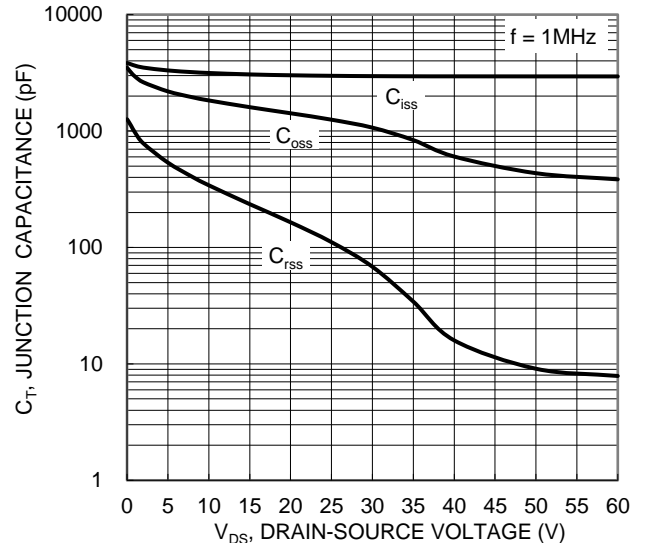


Figure 10. Typical Junction Capacitance

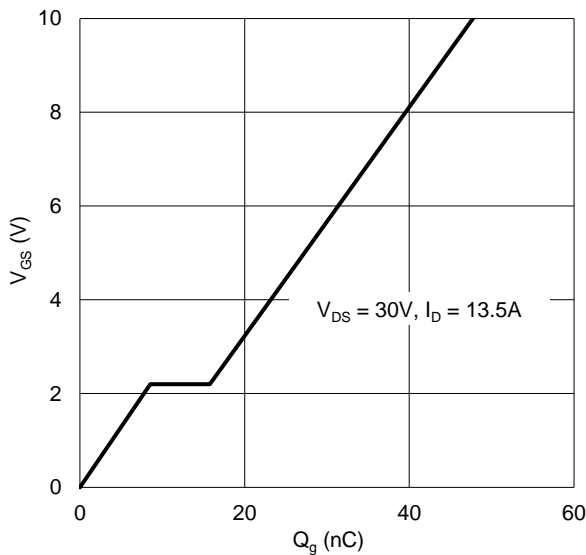


Figure 11. Gate Charge

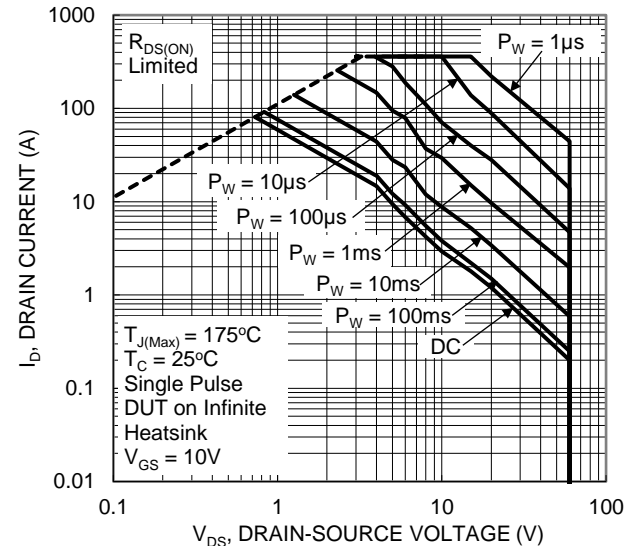


Figure 12. SOA, Safe Operation Area

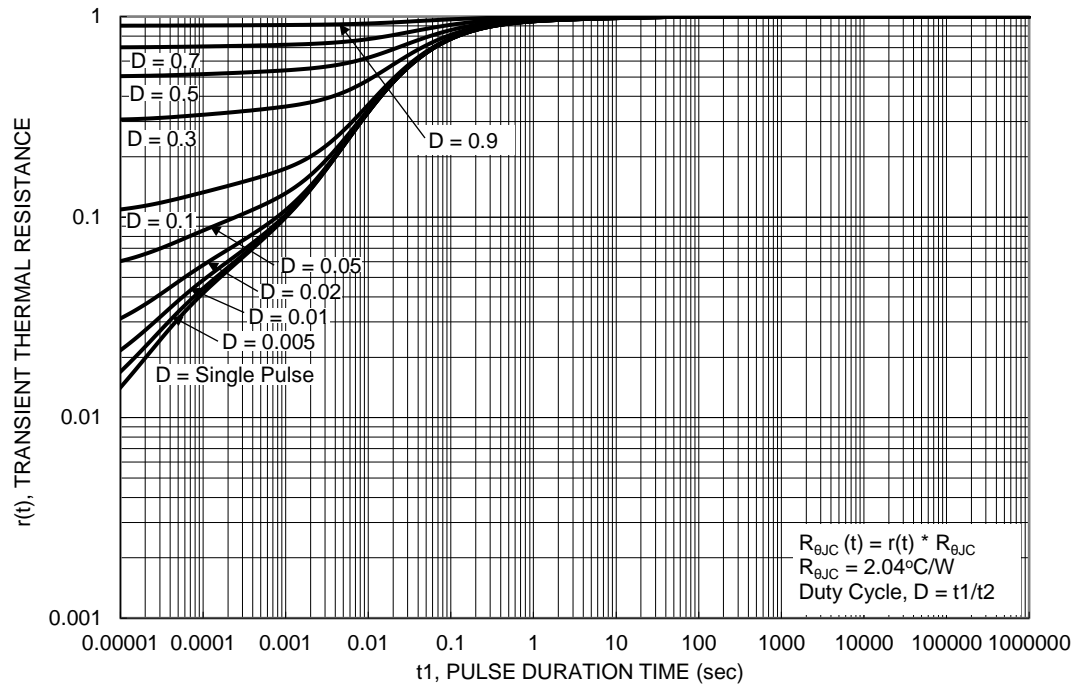
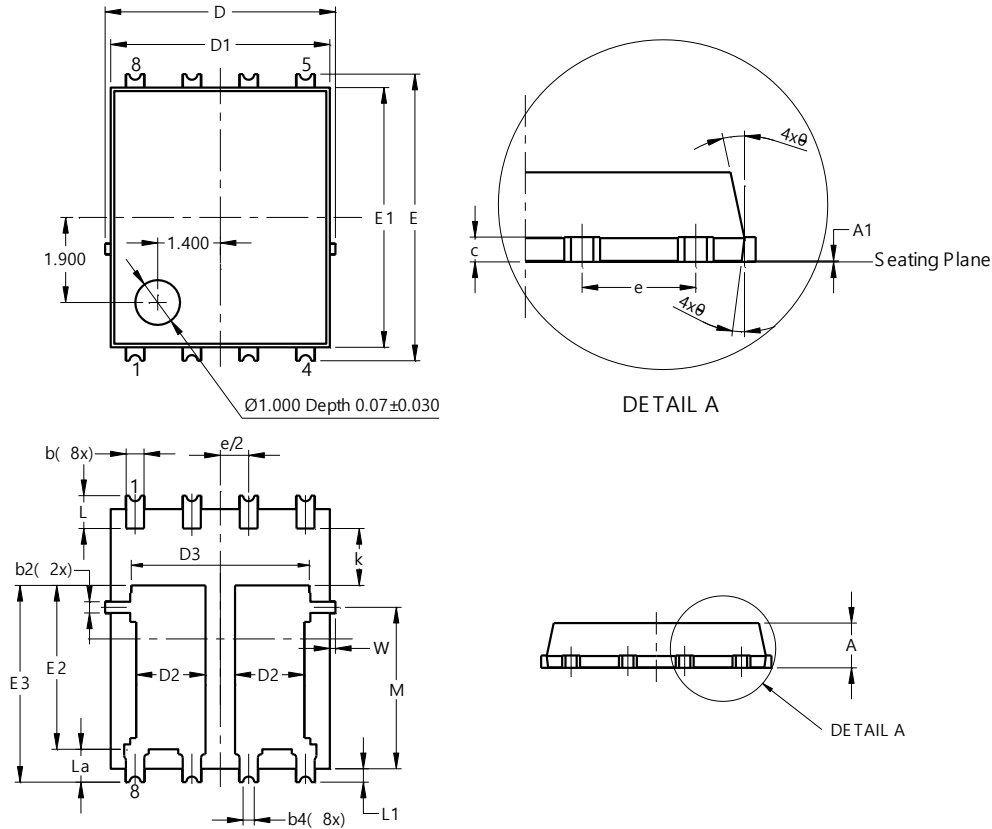


Figure 13. Transient Thermal Resistance

Package Outline Dimensions

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

PowerDI5060-8/SWP (Type UXD)

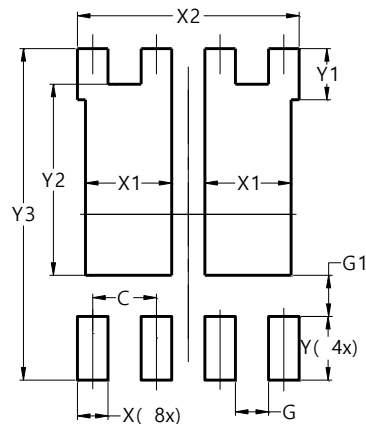


PowerDI5060-8/SWP (Type UXD)			
Dim	Min	Max	Typ
A	0.90	1.10	1.00
A1	0.00	0.05	--
b	0.30	0.50	0.41
b2	0.20	0.35	0.25
b4	0.25REF		
c	0.230	0.330	0.277
D	5.15 BSC		
D1	4.70	5.10	4.90
D2	1.46	1.66	1.55
D3	3.78	4.18	3.98
E	6.40 BSC		
E1	5.60	6.00	5.80
E2	3.46	3.86	3.66
E3	4.195	4.595	4.395
e	1.27BSC		
k	1.05	--	--
L	0.635	0.835	0.735
La	0.635	0.835	0.735
L1	0.200	0.400	0.300
M	3.205	4.005	3.605
W	0.025	0.225	0.125
Ø	10°	12°	11°
Ø1	6°	8°	7°
All Dimensions in mm			

Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

PowerDI5060-8/SWP (Type UXD)



Dimensions	Value (in mm)
C	1.270
G	0.660
G1	0.820
X	0.610
X1	1.720
X2	4.420
Y	1.270
Y1	1.020
Y2	3.810
Y3	6.610

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