

Product Summary

BV _{DSS}	R _{DS(ON)} Max	I _D T _c = +25°C (Note 7)
40V	3.7mΩ @ V _{GS} = 10V	100A

Description and Applications

This MOSFET is designed to minimize the on-state resistance (R_{DS(ON)}) yet maintain superior switching performance, making it ideal for high-efficiency power-management applications.

- Engine management systems
- Body control electronics
- DC-DC converters

Features

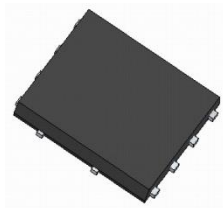
- Rated to +175°C – Ideal For High Ambient Temperature Environments
- 100% Unclamped Inductive Switching – Ensures More Reliable And Robust End Application
- Low R_{DS(ON)} – Minimizes Power Losses
- Low Q_g – Minimizes Switching Losses
- **Lead-Free Finish; RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. “Green” Device (Note 3)**
- **This part is qualified to JEDEC standards (as references in AEC-Q) for High Reliability.**
<https://www.diodes.com/quality/product-definitions/>
- **An automotive-compliant part is available under separate datasheet ([DMTH4005SPSQ](#))**

Mechanical Data

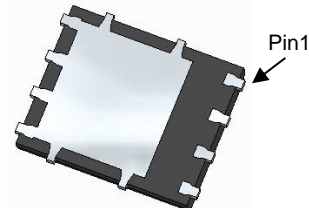
- Package: PowerDI[®]5060-8
- Package Material: Molded Plastic, “Green” Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Finish - Matte Tin Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 ^(E3)
- Weight: 0.097 grams (Approximate)

Site 1:

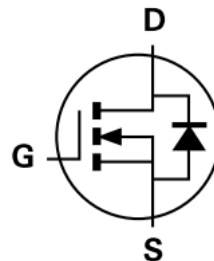
PowerDI5060-8



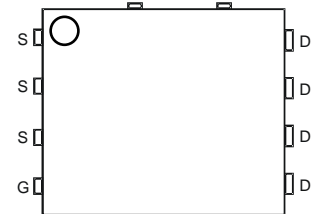
Top View



Bottom View



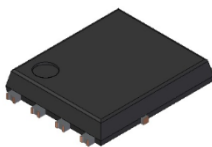
Internal Schematic



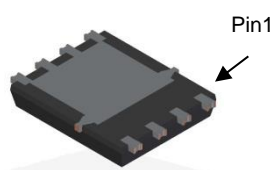
Top View
Pin Configuration

Site 2:

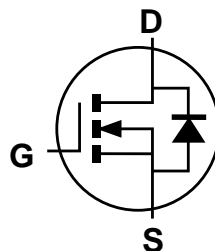
PowerDI5060-8/SWP (Type UX)



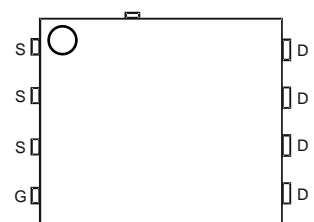
Top View



Bottom View



Internal Schematic



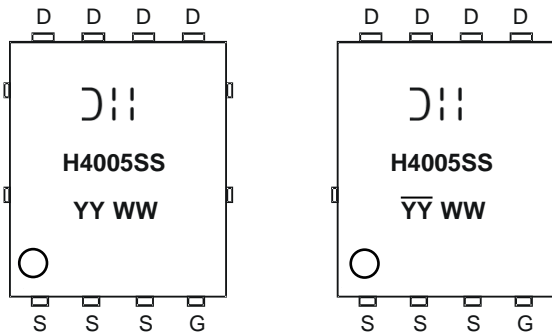
Top View
Pin Configuration

- Notes:
1. EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant. All applicable RoHS exemptions applied.
 2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Ordering Information (Note 4)

Part Number	Package	Packing	
		Qty.	Carrier
DMTH4005SPS-13	PowerDI5060-8	2500	Tape & Reel
DMTH4005SPS-13	PowerDI5060-8/SWP (Type UX)	2500	Tape & Reel

Note: 4. For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

Marking Information


☺|| = Manufacturer's Marking
 H4005SS = Product Type Marking Code
 YYWW = Date Code Marking
 YY or \overline{YY} = Year (ex: 23 = 2023)
 WW = Week (01 to 53)

Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	40	V
Gate-Source Voltage	V_{GSS}	± 20	V
Continuous Drain Current (Note 5)	I_D	20.9 17.5	A
		$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$	
Continuous Drain Current (Notes 6 & 7)	I_D	100 100	A
		$T_C = +25^\circ\text{C}$ $T_C = +100^\circ\text{C}$	
Maximum Continuous Body Diode Forward Current (Note 6)	I_S	100	A
Pulsed Drain Current (10 μs Pulse, Duty Cycle = 1%)	I_{DM}	320	A
Avalanche Current, $L=0.6\text{mH}$	I_{AS}	21	A
Avalanche Energy, $L=0.6\text{mH}$	E_{AS}	132.3	mJ

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Total Power Dissipation (Note 5)	P_D	2.6	W
		$T_A = +25^\circ\text{C}$	
Thermal Resistance, Junction to Ambient (Note 5)	$R_{\theta JA}$	57	$^\circ\text{C/W}$
Total Power Dissipation (Note 6)	P_D	150	W
		$T_C = +25^\circ\text{C}$	
Thermal Resistance, Junction to Case (Note 6)	$R_{\theta JC}$	1	$^\circ\text{C/W}$
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +175	$^\circ\text{C}$

Notes: 5. Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1-inch square copper plate.
 6. Thermal resistance from junction to soldering point (on the exposed drain pad).
 7. Package limited.

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Drain-Source Breakdown Voltage	BV _{DSS}	40	—	—	V	V _{GS} = 0V, I _D = 1mA
Zero Gate Voltage Drain Current	I _{DSS}	—	—	1	μA	V _{DS} = 32V, V _{GS} = 0V
Gate-Source Leakage	I _{GSS}	—	—	±100	nA	V _{GS} = ±20V, V _{DS} = 0V
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	V _{GS(TH)}	2	—	4	V	V _{DS} = V _{GS} , I _D = 250μA
Static Drain-Source On-Resistance	R _{DS(ON)}	—	2.9	3.7	mΩ	V _{GS} = 10V, I _D = 50A
Diode Forward Voltage	V _{SD}	—	0.88	—	V	V _{GS} = 0V, I _S = 50A
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C _{iss}	—	3062	—	pF	V _{DS} = 20V, V _{GS} = 0V, f = 1MHz
Output Capacitance	C _{oss}	—	902.2	—		
Reverse Transfer Capacitance	C _{rss}	—	179.2	—		
Gate Resistance	R _g	—	0.67	—	Ω	V _{DS} = 0V, V _{GS} = 0V, f = 1MHz
Total Gate Charge	Q _g	—	49.1	—	nC	V _{DD} = 20V, I _D = 50A, V _{GS} = 10V
Gate-Source Charge	Q _{gs}	—	10.3	—		
Gate-Drain Charge	Q _{gd}	—	13	—		
Turn-On Delay Time	t _{D(ON)}	—	8.7	—	ns	V _{DD} = 20V, V _{GS} = 10V, I _D = 50A, R _G = 3Ω
Turn-On Rise Time	t _r	—	6.8	—		
Turn-Off Delay Time	t _{D(OFF)}	—	18.6	—		
Turn-Off Fall Time	t _f	—	7.3	—		
Body Diode Reverse Recovery Time	t _{RR}	—	31.8	—	ns	I _F = 50A, di/dt = 100A/μs
Body Diode Reverse Recovery Charge	Q _{RR}	—	26.5	—	nC	

Notes: 8. Short duration pulse test used to minimize self-heating effect.
9. Guaranteed by design. Not subject to product testing.

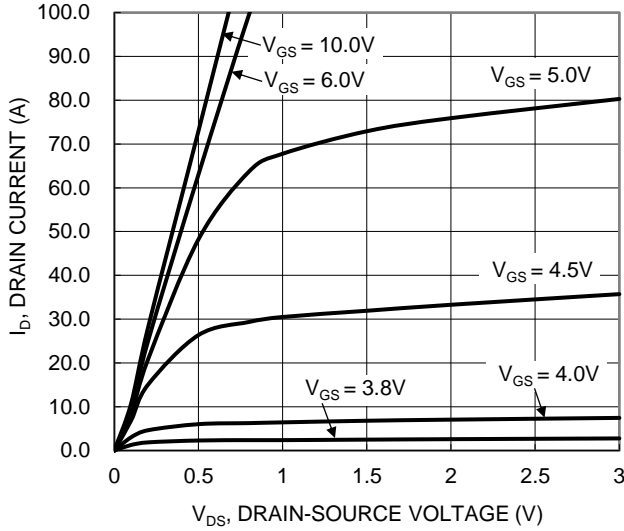


Figure 1 Typical Output Characteristic

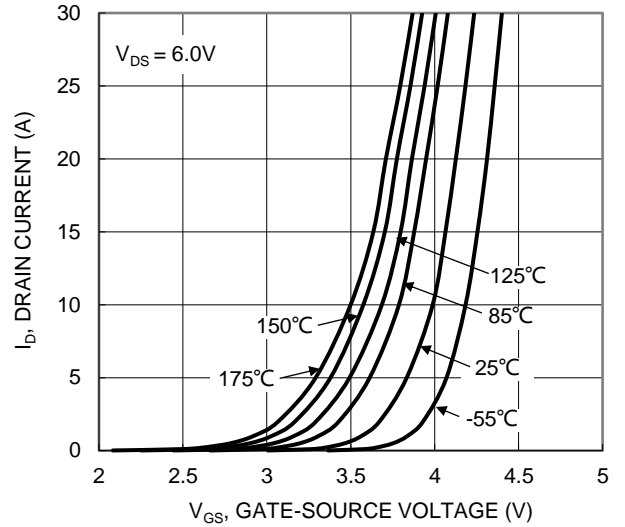


Figure 2 Typical Transfer Characteristic

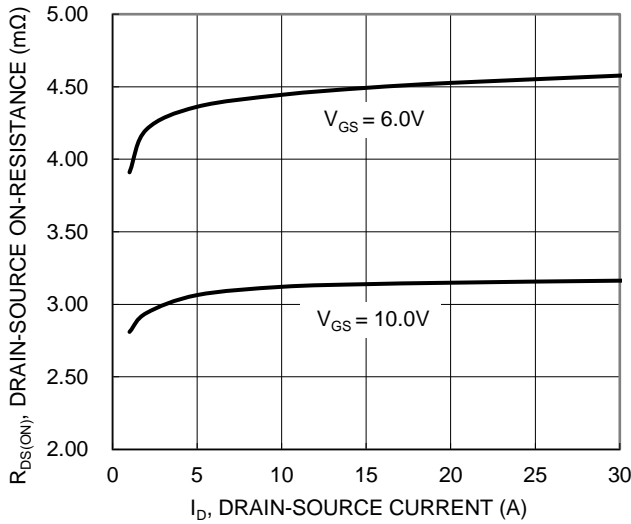


Figure 3 Typical On-Resistance vs. Drain Current and Gate Voltage

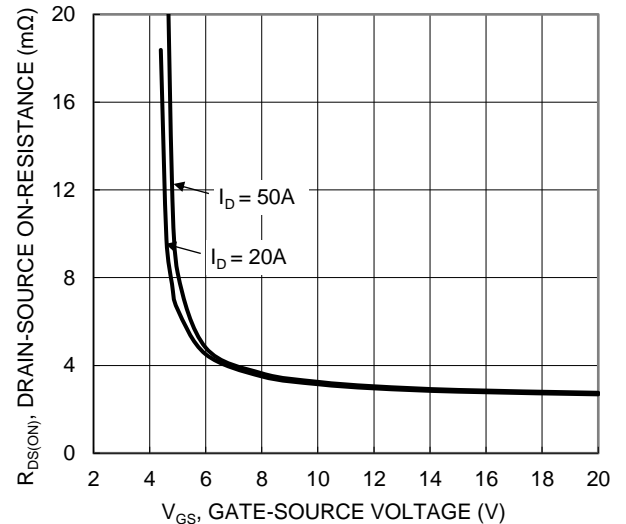


Figure 4 Typical Transfer Characteristic

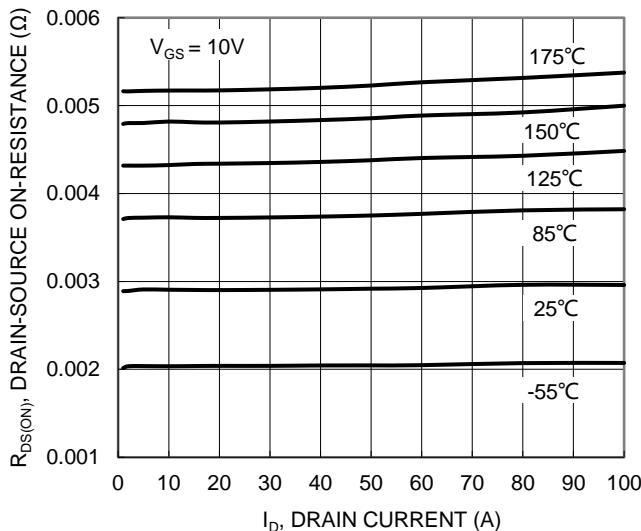


Figure 5 Typical On-Resistance vs. Drain Current and Temperature

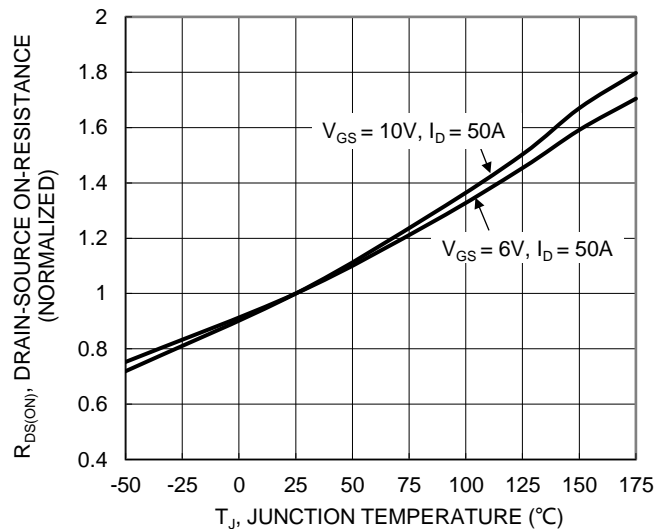


Figure 6 On-Resistance Variation with Temperature

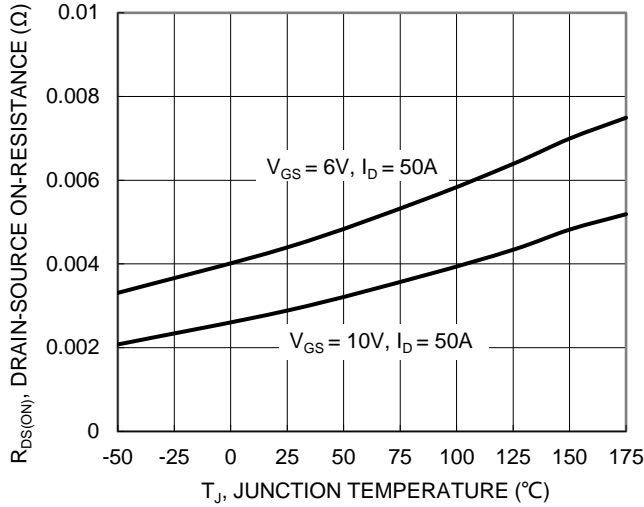


Figure 7 On-Resistance Variation with Temperature

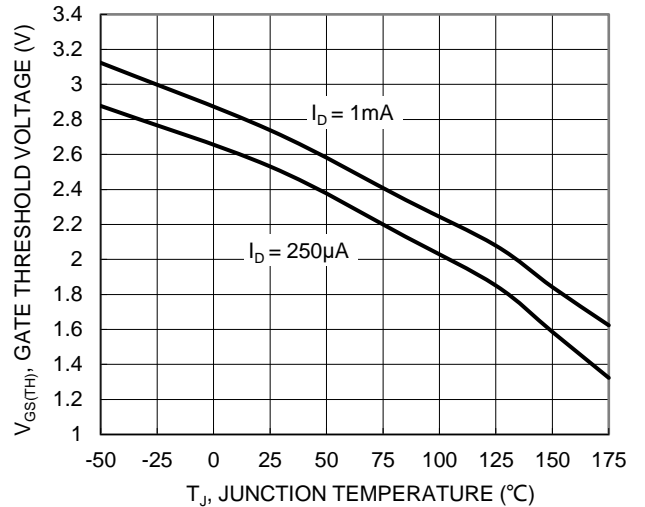


Figure 8 Gate Threshold Variation vs. Temperature

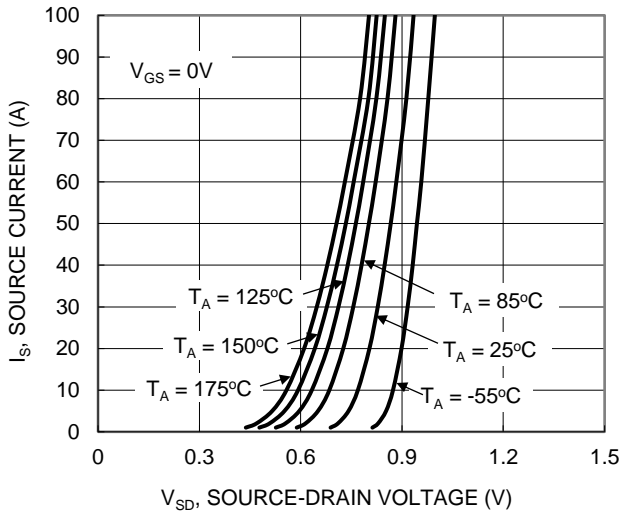


Figure 9 Diode Forward Voltage vs. Current

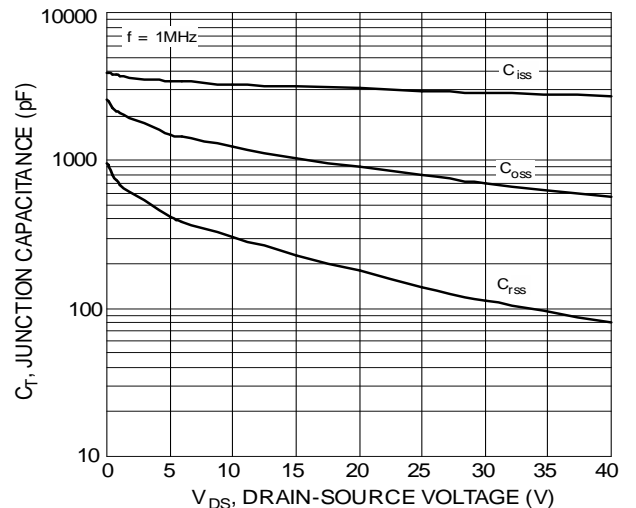


Figure 10 Typical Junction Capacitance

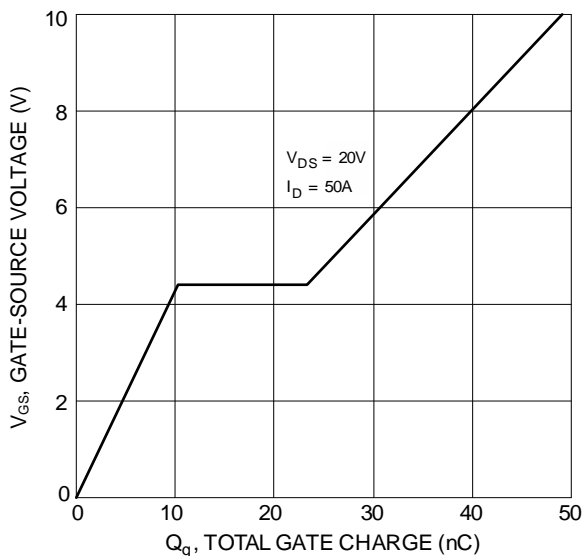


Figure 11 Gate Charge

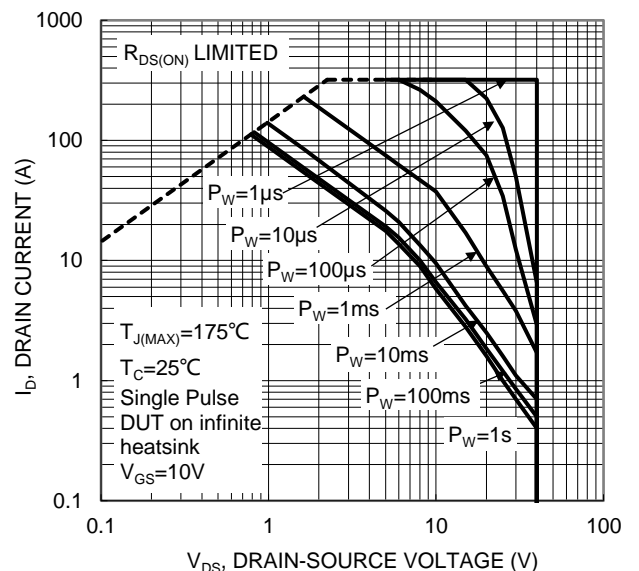


Figure 12 SOA, Safe Operation Area

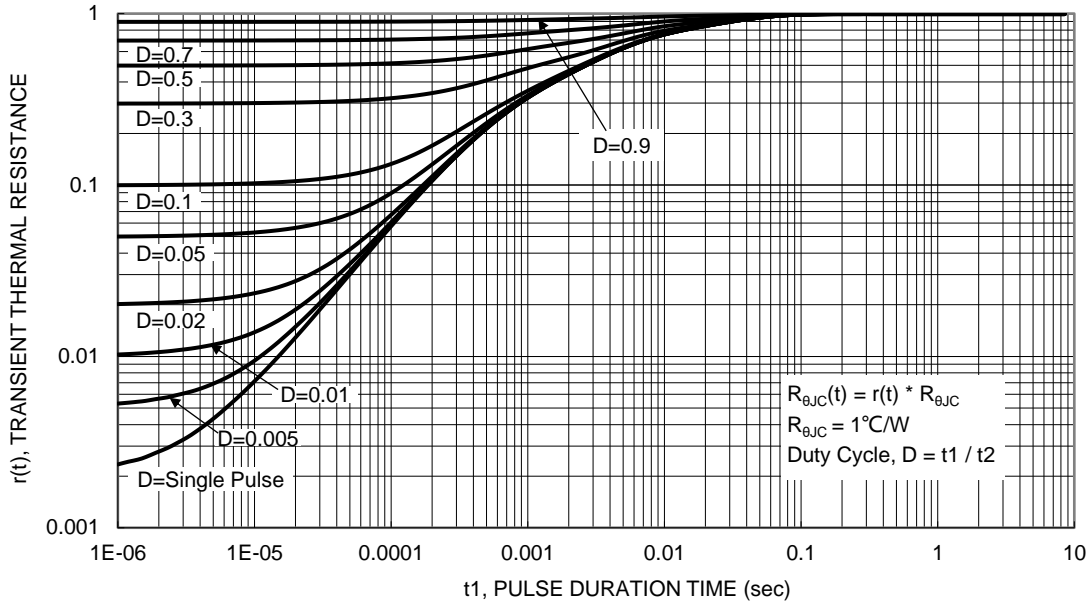


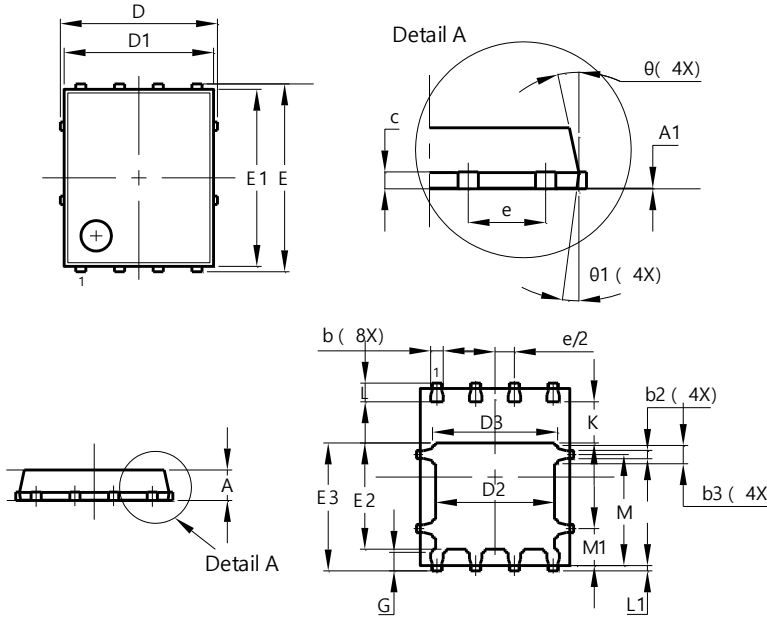
Figure 13. Transient Thermal Resistance

Package Outline Dimensions

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

Site 1:

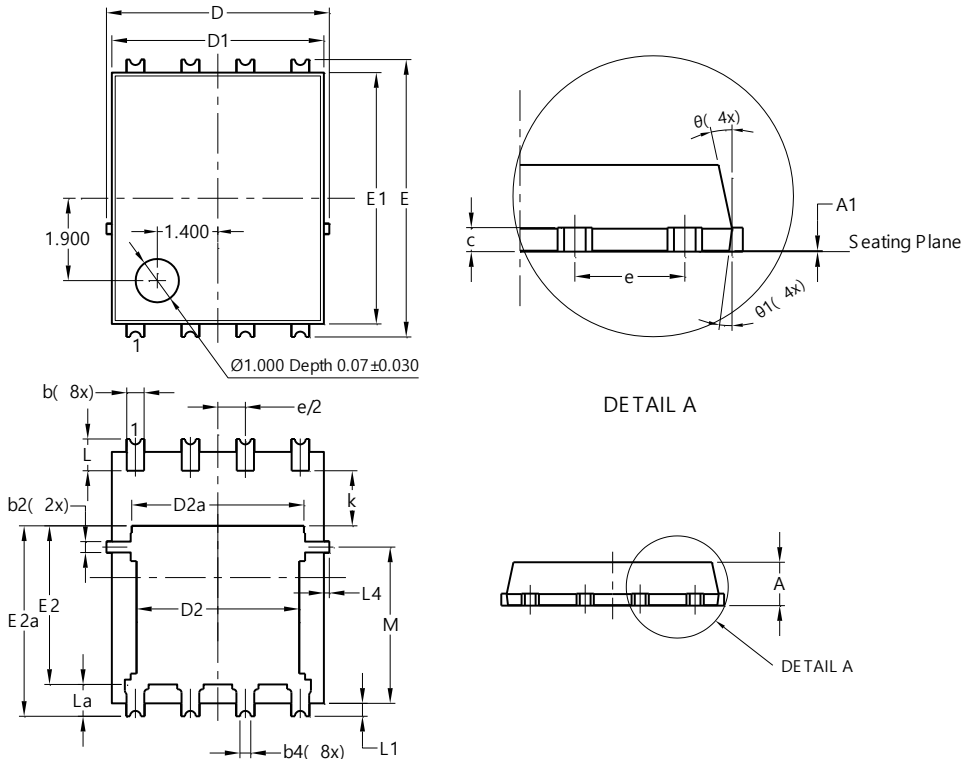
PowerDI5060-8



PowerDI5060-8			
Dim	Min	Max	Typ
A	0.90	1.10	1.00
A1	0.00	0.05	—
b	0.33	0.51	0.41
b2	0.200	0.350	0.273
b3	0.40	0.80	0.60
c	0.230	0.330	0.277
D	5.15 BSC		
D1	4.70	5.10	4.90
D2	3.70	4.10	3.90
D3	3.90	4.30	4.10
E	6.15 BSC		
E1	5.60	6.00	5.80
E2	3.28	3.68	3.48
E3	3.99	4.39	4.19
e	1.27 BSC		
G	0.51	0.71	0.61
K	0.51	—	—
L	0.51	0.71	0.61
L1	0.100	0.200	0.175
M	3.235	4.035	3.635
M1	1.00	1.40	1.21
θ	10°	12°	11°
θ1	6°	8°	7°
All Dimensions in mm			

Site 2:

PowerDI5060-8/SWP (Type UX)



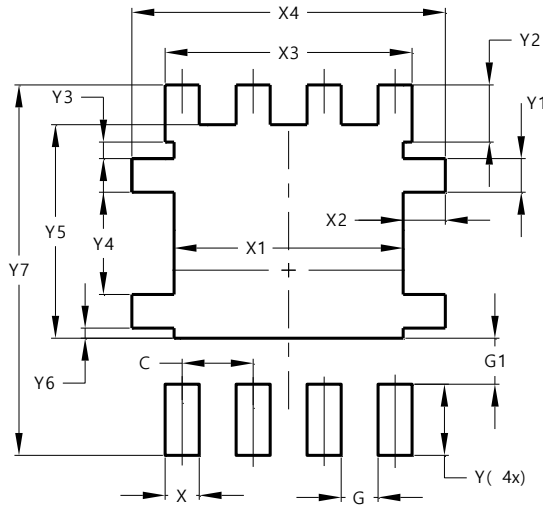
PowerDI5060-8/SWP (Type UX)			
Dim	Min	Max	Typ
A	0.90	1.10	1.00
A1	0	0.05	--
b	0.30	0.50	0.41
b2	0.20	0.35	0.25
b4	0.25REF		
c	0.230	0.330	0.277
D	5.15 BSC		
D1	4.70	5.10	4.90
D2	3.56	3.96	3.76
D2a	3.78	4.18	3.98
E	6.40 BSC		
E1	5.60	6.00	5.80
E2	3.46	3.86	3.66
E2a	4.195	4.595	4.395
e	1.27BSC		
k	1.05	--	--
L	0.635	0.835	0.735
La	0.635	0.835	0.735
L1	0.200	0.400	0.300
L1a	0.050REF		
L4	0.025	0.225	0.125
M	3.205	4.005	3.605
θ	10°	12°	11°
θ1	6°	8°	7°
All Dimensions in mm			

Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

Site 1:

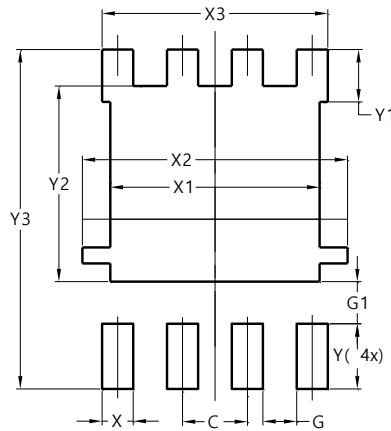
PowerDI5060-8



Dimensions	Value (in mm)
C	1.270
G	0.660
G1	0.820
X	0.610
X1	4.100
X2	0.755
X3	4.420
X4	5.610
Y	1.270
Y1	0.600
Y2	1.020
Y3	0.295
Y4	1.825
Y5	3.810
Y6	0.180
Y7	6.610

Site 2:

PowerDI5060-8/SWP (Type UX)



Dimensions	Value (in mm)
C	1.270
G	0.660
G1	0.820
X	0.610
X1	4.100
X2	5.190
X3	4.420
Y	1.270
Y1	1.020
Y2	3.810
Y3	6.610

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