



DUAL P-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary

BV _{DSS}	R _{D1D2(ON)} TYP	I _{D1D2} T _A = +25°C
-20V	$82m\Omega$ @ $V_{GS} = -4.5V$	-3.0A

Description

This new generation MOSFET has been designed to minimize the onstate resistance (R_{D1D2(ON)}) yet maintain superior switching performance, making it ideal for high-efficiency power-management applications.

Applications

- Battery management
- Load switches
- Battery protections



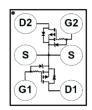
Features and Benefits

- Low Q_g & Q_{gd}
- Dual PMOS in Common-Source Configuration
- Small Footprint 1.5mm × 1.0mm
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.

https://www.diodes.com/quality/product-definitions/

Mechanical Data

- Package: U-WLB1510-6
- Terminal Connections: See Diagram Below
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal: Finish SnAgCu. Solderable per MIL-STD-202 Method 208 (a)
- UBM Opening: 245µm
- Weight: 0.002 grams (Approximate)



Top View

Ordering Information (Note 4)

Orderable Part Number	Packago	Packing		
Orderable Part Number	Package	Qty.	Carrier	
DMP2109UCB6-7	U-WLB1510-6 (Type C)	3000	Tape & Reel	

Notes:

- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
- 2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information



AT = Product Type Marking Code YW = Date Code Marking Y or Y = Year (ex: 5 = 2025)

W or \overline{W} = Week (ex: a = week 27; z represents week 52 and 53)

Date Code Key

Year	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036
Code	5	6	7	8	9	0	1	2	3	4	5	6

Week	1-26	27-52	53
Code	A-Z	a-z	z



Maximum Ratings (@TA = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit	
Drain-Source Voltage		V _D s	-20	V	
Gate-Source Voltage			Vgs	-6	V
Continuous Drain Current (Note 5) V _{GS} = -4.5V	Steady State	T _A = +25°C T _A = +70°C	I _{D1D2}	-2.25 -1.8	А
Continuous Drain Current (Note 6) $V_{GS} = -4.5V$ Steady $T_A = +25^{\circ}C$ State $T_A = +70^{\circ}C$			I _{D1D2}	-3.0 -2.4	А
Continuous Source Pin Current (Note 6)			ls	-1.52	Α
Continuous Gate Clamp Current (Note 6)		lg	-0.5	Α	
Pulsed Source Pin Current (Pulse Duration 10µs, I	sed Source Pin Current (Pulse Duration 10µs, Duty Cycle ≤ 1%)		lsм	-22	Α
Pulsed Gate Clamp Current (Pulse Duration 10μs,	Duty Cycle	e ≤ 1%)	lgм	-7	Α

Thermal Characteristics (@TA = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Total Power Dissipation (Note 5)	PD	0.84	W
Total Power Dissipation (Note 6)	PD	1.2	W
Thermal Resistance, Junction to Ambient (Note 5)	R ₀ JA	152.7	°C/W
Thermal Resistance, Junction to Ambient (Note 6)	Reja	105.4	°C/W
Operating and Storage Temperature Range	TJ, TSTG	-55 to +150	°C

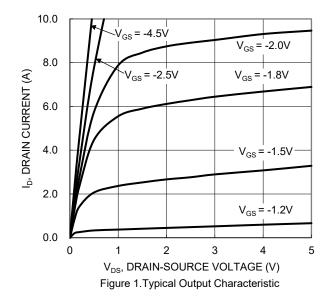
Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition	
DFF CHARACTERISTICS (Note 7)							
Drain-Source Breakdown Voltage	BVDSS	-20	_	_	V	$V_{GS} = 0$, $I_{DS} = -250\mu A$	
Zero Gate Voltage Drain Current @Tc = +25°C	IDSS	_	_	-1	μΑ	V _{DS} = -16V, V _{GS} = 0	
Gate-Source Leakage	I _{GSS}	_	_	-100	nA	$V_{GS} = -6V, V_{DS} = 0$	
ON CHARACTERISTICS (Note 7)							
Gate Threshold Voltage	V _G S(TH)	- 0.5	-0.75	-1.1	V	$V_{DS} = V_{GS}$, $I_{DS} = -250\mu A$	
		_	82	108		$V_{GS} = -4.5V$, $I_{D1D2} = -1A$	
	R _{D1D2(ON)}	_	110	150	mΩ	$V_{GS} = -2.5V$, $I_{D1D2} = -1A$	
Static Drain-Source On-Resistance		_	160	240		V _G S = -1.8V, I _{D1D2} = -1A	
Static Dialii-Source Oil-Resistance		_	42	55		V _{GS} = -4.5V, I _{DS} = -1A	
	RDS(ON)	_	56	80	mΩ	V _G S = -2.5V, I _D S = -1A	
		_	80	120		V _{GS} = -1.8V, I _{DS} = -1A	
DIODE CHARACTERISTICS							
Diode Forward Voltage (Note 6)	VsD	_	-0.72	-1	V	V _{GS} = 0, I _{DS} = -1A	
DYNAMIC CHARACTERISTICS (Note 8)							
Input Capacitance	C _{iss}	_	269	_	pF	\/ 40\/ \/ 0	
Output Capacitance	Coss	_	142	_	pF	V _{DS} = -10V, V _{GS} = 0, - f = 1.0MHz	
Reverse Transfer Capacitance	Crss	_	7.6	_	pF	1 = 1:01/11/12	
Total Gate Charge	Qg	_	2.1	_	nC		
Gate-Source Charge	Qgs	_	0.3	_	nC	V _{GS} = -4.5V, V _{DS} = -10V,	
Gate-Drain Charge	Q_{gd}	_	0.3	_	nC	I _{DS} = -1A	
Gate Charge at V _{TH}	Q _{g(TH)}	_	0.16	_	nC		
Turn-On Delay Time	t _{D(ON)}	_	6	_	ns		
Turn-On Rise Time	t _R		7		ns	$V_{DD} = -10V, V_{GS} = -4.5V,$	
Turn-Off Delay Time	t _D (OFF)	_	34	_	ns	$I_{DS} = -1A, R_G = 30\Omega$	
Turn-Off Fall Time	tF	_	16	_	ns		

Notes:

- 5. Device mounted on FR-4 PCB with minimum recommended pad layout.
- 6. Device mounted on FR-4 material with 1 inch² (6.45cm²), 2 oz. (0.071mm thick) Cu.
- 7. Short duration pulse test used to minimize self-heating effect.
- 8. Guaranteed by design. Not subject to production testing.





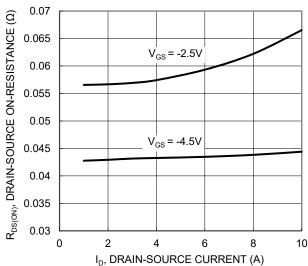


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

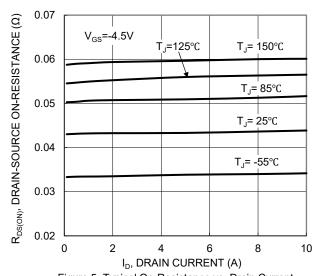


Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature

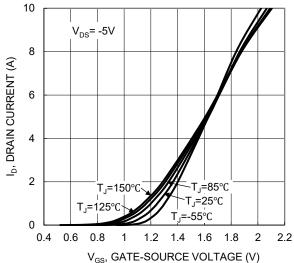


Figure 2. Typical Transfer Characteristic

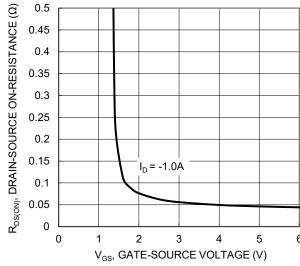


Figure 4. Typical Transfer Characteristic

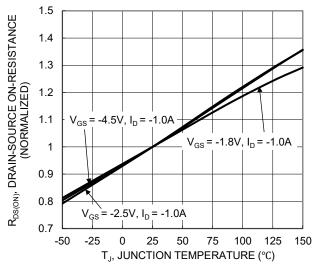


Figure 6. On-Resistance Variation with Junction Temperature



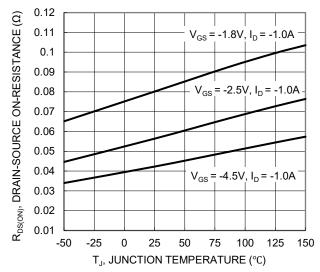


Figure 7. On-Resistance Variation with Junction Temperature

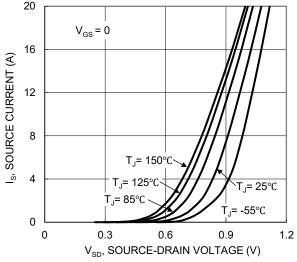
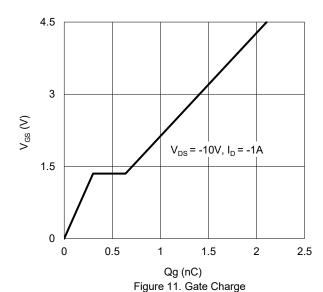


Figure 9. Diode Forward Voltage vs. Current



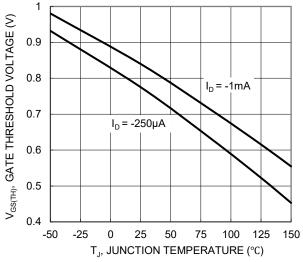


Figure 8. Gate Threshold Variation vs. Junction Temperature

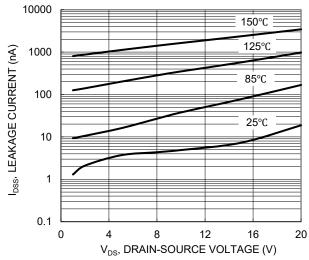


Figure 10. Typical Drain-Source Leakage Current vs.

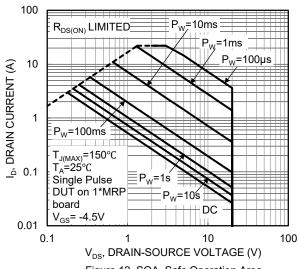


Figure 12. SOA, Safe Operation Area



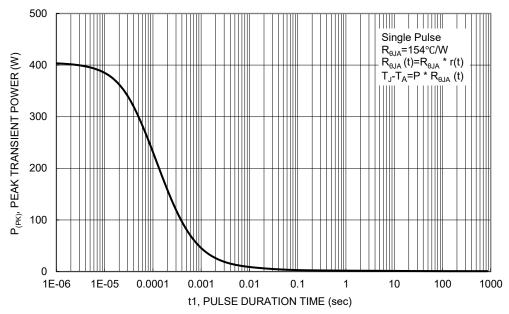


Figure 13. Single Pulse Maximum Power Dissipation

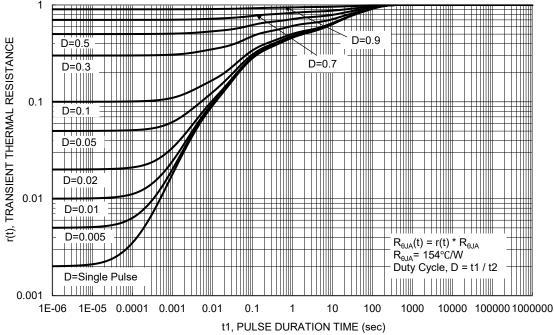


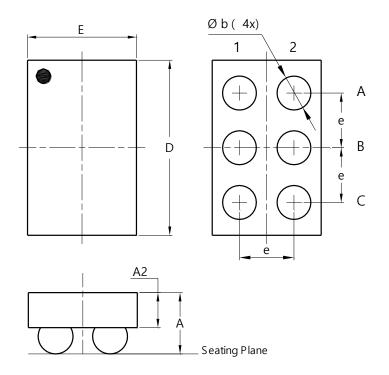
Figure 14. Transient Thermal Resistance



Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-WLB1510-6 (Type C)

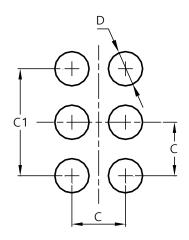


U-WLB1510-6							
	(Туре	(C					
Dim	Min	Max	Тур				
Α	ı	0.625					
A2	1	ı	0.320				
b	0.279	0.341	0.310				
D	1.470	1.520	1.495				
Е	0.970	1.020	0.995				
е	ı	1	0.50				
Co- planarity	<u><</u> 0.038						
All D	imensio	ons in m	ım				

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-WLB1510-6 (Type C)



Dimensions	Value (in mm)		
C	0.50		
C1	1.00		
D	0.30		



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