20V N-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary

BV_{DSS}	$R_{DS(ON)}$ MAX	I_D MAX T_A = +25°C
20V	0.6Ω @ V_{GS} = 4.5V	1.2A
	0.8Ω @ V_{GS} = 2.5V	1.1A
	1.0Ω @ V_{GS} = 1.8V	0.9A

Features

- 0.6mm Profile – Ideal for Low Profile Applications
- PCB Footprint of 4mm^2
- Low Gate Threshold Voltage
- Low On-Resistance
- ESD Protected Gate
- Wettable Flank for Improved Optical Inspection
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **The DMN2451UFDFWQ is suitable for automotive applications requiring specific change control; this part is AEC-Q101 qualified, PPAP capable, and manufactured in IATF 16949 certified facilities.**
  https://www.diodes.com/quality/product-definitions/

Description and Applications

This MOSFET is designed to meet the stringent requirements of automotive applications. It is qualified to AEC-Q101, supported by a PPAP and is ideal for use in:

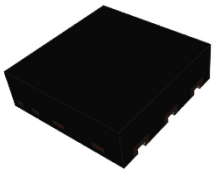
- Power-management functions
- General-purpose interfacing switches

Mechanical Data

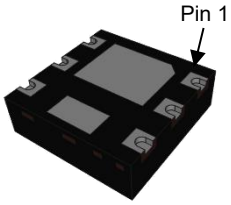
- Package: U-DFN2020-6
- Package Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – NiPdAu over Copper Leadframe. Solderable per MIL-STD-202, Method 208 e4
- Weight: 0.0065 grams (Approximate)

U-DFN2020-6/SWP (Type UXG)

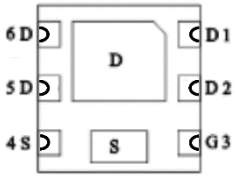
ESD PROTECTED



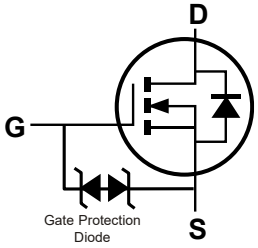
Top View



Bottom View



Pinout
Bottom View



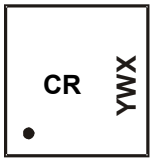
Equivalent Circuit

Ordering Information (Note 4)

Orderable Part Number	Package	Packing	
		Qty.	Carrier
DMN2451UFDFWQ-7	U-DFN2020-6/SWP (Type UXG)	3,000	Tape & Reel
DMN2451UFDFWQ-13	U-DFN2020-6/SWP (Type UXG)	10,000	Tape & Reel

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information



CR = Product Type Marking Code
YWX = Date Code Marking
Y = Year (ex: 5 = 2025)
W = Week (ex: a = Week 27; z Represents Weeks 52 and 53)
X = Internal Code (ex: U = Monday)

Date Code Key

Year	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036
Code	5	6	7	8	9	0	1	2	3	4	5	6

Week	1-26	27-52	53
Code	A-Z	a-z	z

Internal Code	Sun	Mon	Tue	Wed	Thu	Fri	Sat
Code	T	U	V	W	X	Y	Z

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	20	V
Gate-Source Voltage			V_{GSS}	±12	V
Continuous Drain Current (Note 6) V_{GS} = 4.5V	Steady State	T_A = +25°C T_A = +70°C	I_D	1.2 0.7	A
Continuous Drain Current (Note 6) V_{GS} = 2.5V	Steady State	T_A = +25°C T_A = +70°C	I_D	1.1 0.6	A
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)			I_{DM}	3	A
Maximum Body Diode Continuous Current (Note 6)			I_S	1	A

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)		P_D	0.87	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	$R_{\theta JA}$	144	°C/W
Total Power Dissipation (Note 6)		P_D	1.39	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	$R_{\theta JA}$	90	°C/W
Thermal Resistance, Junction to Case (Note 6)		$R_{\theta JC}$	31	°C/W
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Notes: 5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	20	—	—	V	V_{GS} = 0, I_D = 250μA
Zero Gate Voltage Drain Current T_J = +25°C	I_{DSS}	—	—	1	μA	V_{DS} = 20V, V_{GS} = 0
Gate-Source Leakage	I_{GSS}	—	—	±1.0	μA	V_{GS} = ±4.5V, V_{DS} = 0
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(TH)}$	0.45	—	1.0	V	V_{DS} = V_{GS}, I_D = 250μA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	0.27	0.6	Ω	V_{GS} = 4.5V, I_D = 200mA
			0.35	0.8		V_{GS} = 2.5V, I_D = 200mA
			0.52	1.0		V_{GS} = 1.8V, I_D = 100mA
			0.77	1.6		V_{GS} = 1.5V, I_D = 50mA
Diode Forward Voltage	V_{SD}	—	0.7	1.2	V	V_{GS} = 0, I_S = 500mA
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	—	52	—	pF	V_{DS} =16V, V_{GS} = 0, f = 1.0MHz
Output Capacitance	C_{oss}	—	4.8	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	3.1	—	pF	
Gate Resistance	R_g	—	95	—	Ω	V_{DS} = 0, V_{GS} = 0 f = 1.0MHz
Total Gate Charge	Q_g	—	0.7	—	nC	V_{GS} = 4.5V, V_{DS} = 10V, I_D = 250mA
Gate-Source Charge	Q_{gs}	—	0.2	—	nC	
Gate-Drain Charge	Q_{gd}	—	0.1	—	nC	
Turn-On Delay Time	$t_{D(ON)}$	—	3.7	—	ns	V_{DD} = 10V, V_{GS} = 4.5V, R_L = 47Ω, R_G = 10Ω, I_D = 200mA
Turn-On Rise Time	t_R	—	2.4	—	ns	
Turn-Off Delay Time	$t_{D(OFF)}$	—	20.9	—	ns	
Turn-Off Fall Time	t_F	—	5.6	—	ns	

Notes: 7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to product testing.

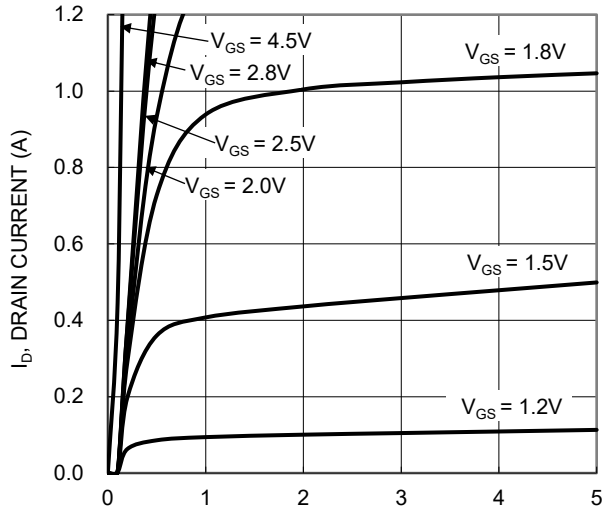


Figure 1. Typical Output Characteristic

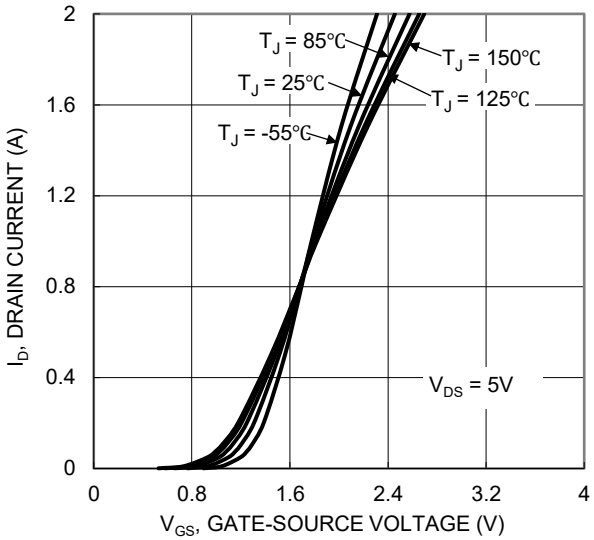


Figure 2. Typical Transfer Characteristic

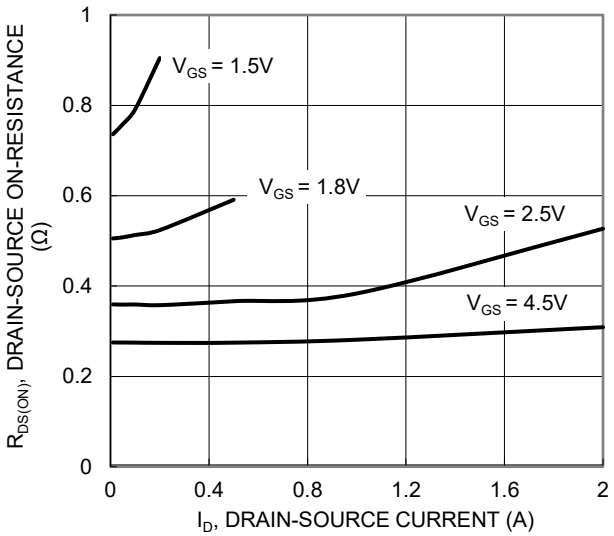


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

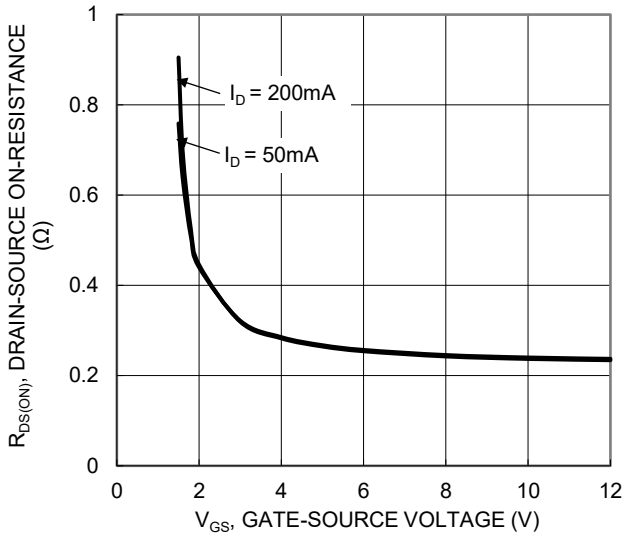


Figure 4. Typical Transfer Characteristic

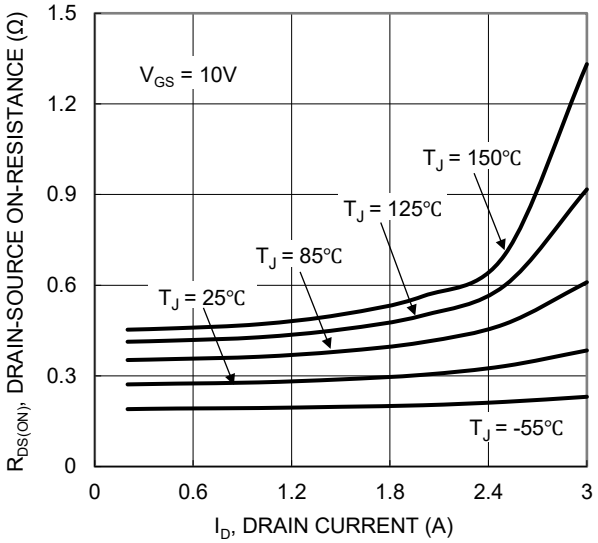


Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature

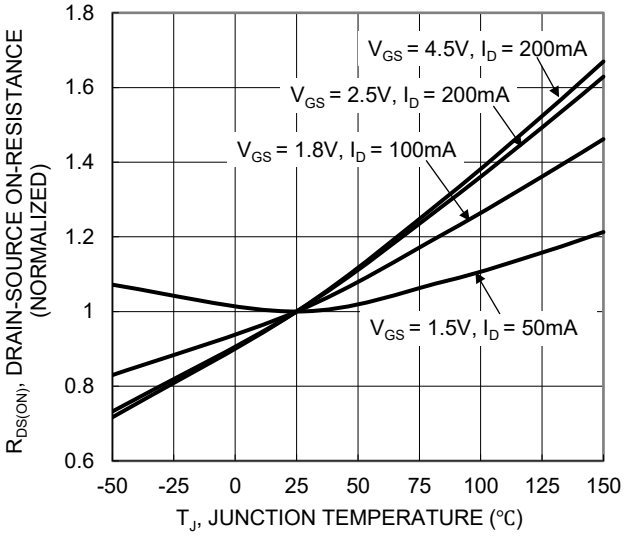


Figure 6. On-Resistance Variation with Temperature

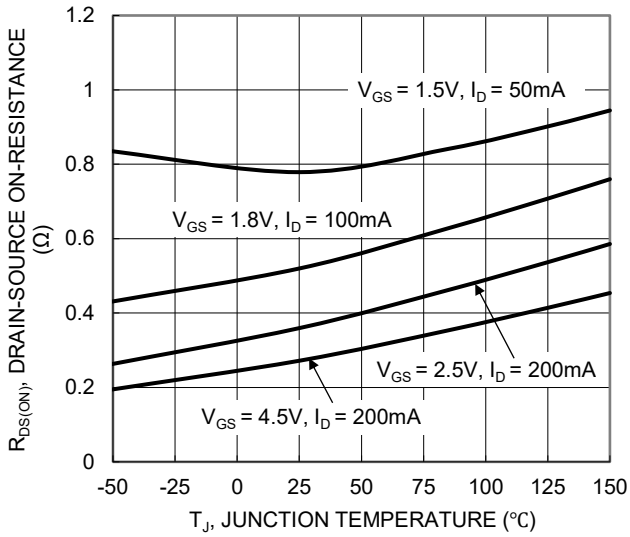


Figure 7. On-Resistance Variation with Temperature

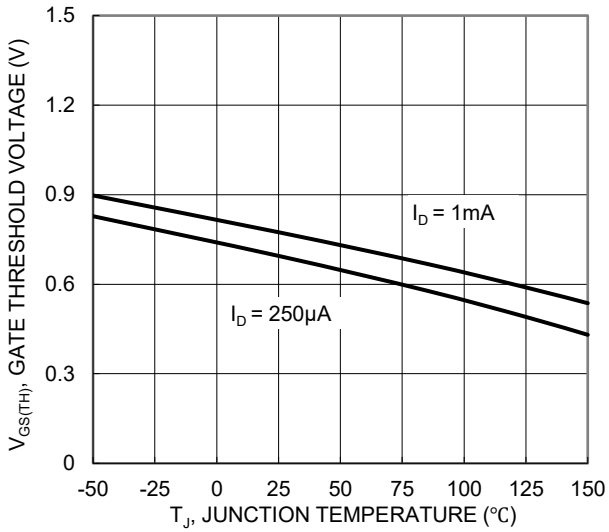


Figure 8. Gate Threshold Variation vs. Junction Temperature

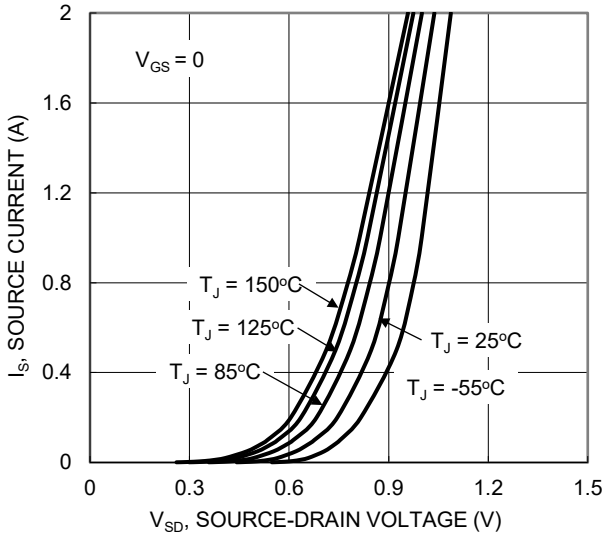


Figure 9. Diode Forward Voltage vs. Current

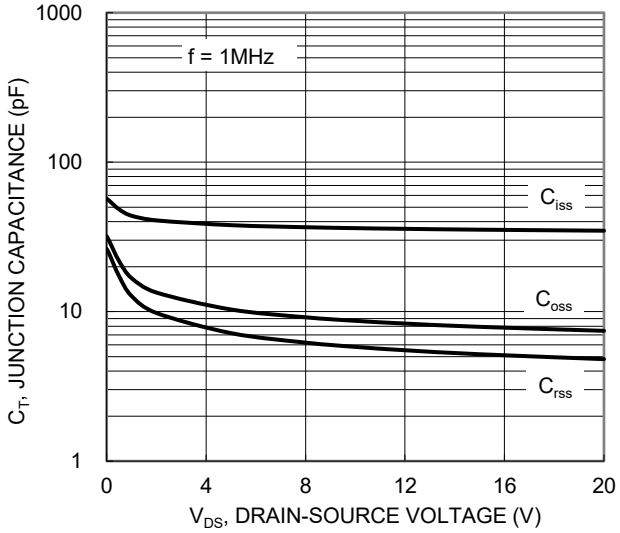


Figure 10. Typical Junction Capacitance

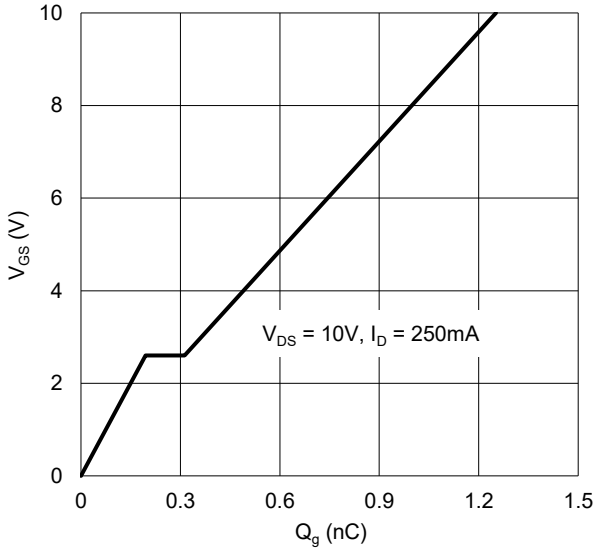


Figure 11. Gate Charge

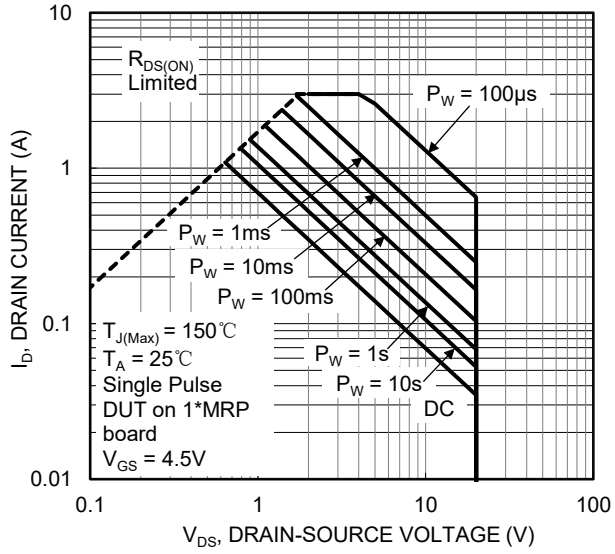


Figure 12. SOA, Safe Operation Area

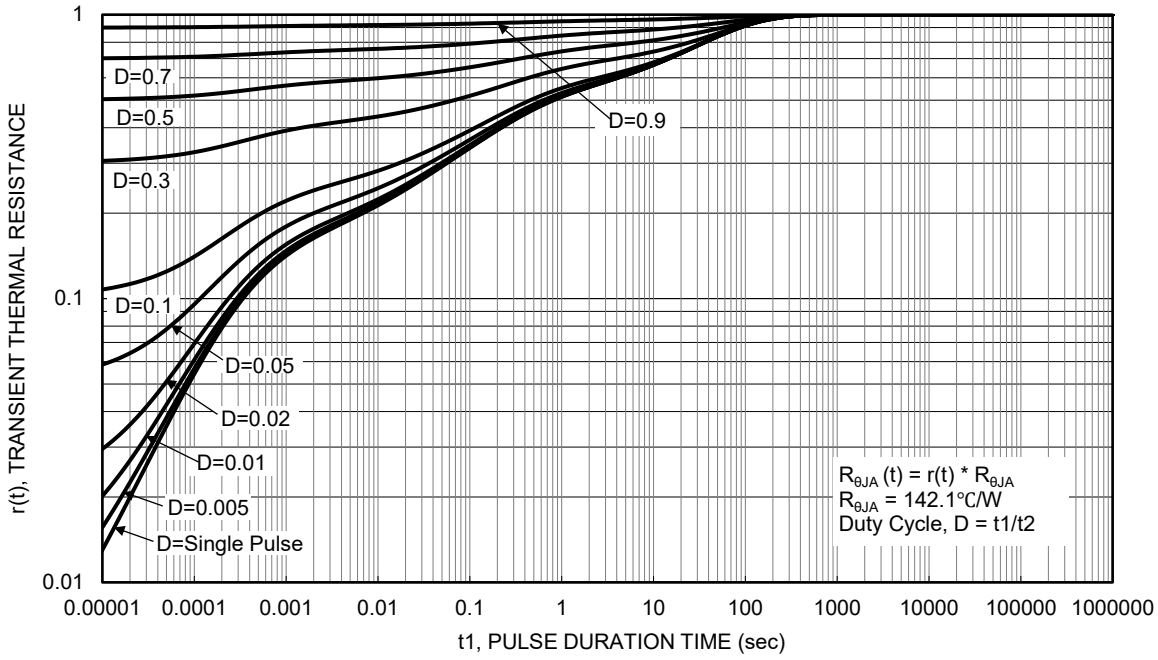
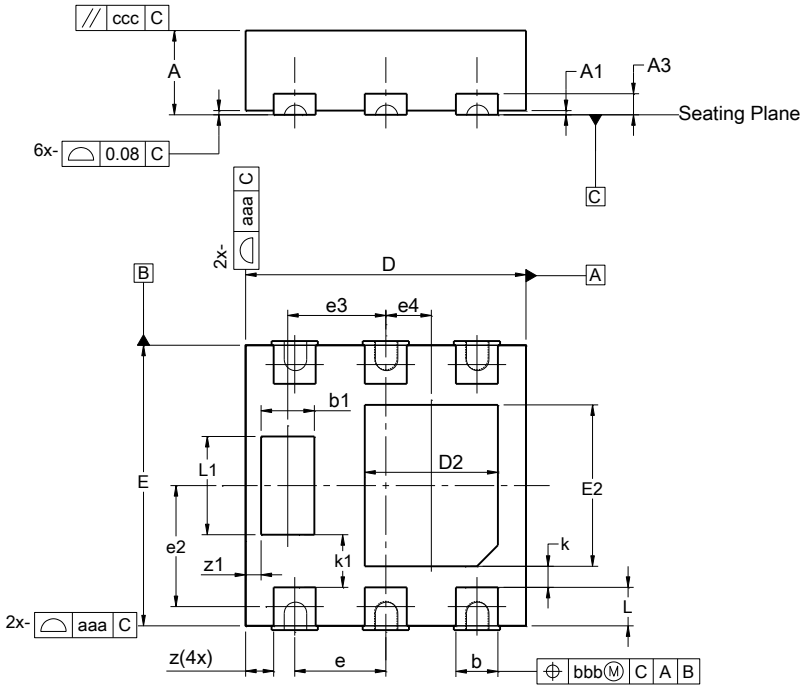


Figure 13. Transient Thermal Resistance

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-DFN2020-6/SWP (Type UXG)

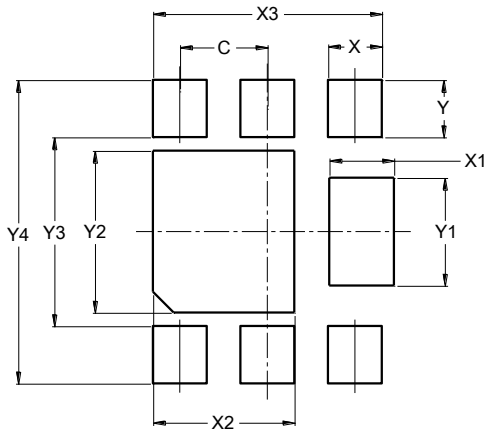


U-DFN2020-6/SWP (Type UXG)			
Dim	**Min**	**Max**	**Typ**
A	0.59	0.65	0.62
A1	0.00	0.05	0.03
A3	—	—	0.152
b	0.28	0.38	0.33
b1	0.35	0.45	0.40
D	1.95	2.05	2.00
D2	0.87	1.07	0.97
E	1.95	2.05	2.00
E2	1.07	1.27	1.17
e	0.65 BSC		
e3	0.70 BSC		
e4	0.325 BSC		
L	0.225	0.325	0.275
L1	0.67	0.77	0.72
k	—	—	0.15
k1	—	—	0.375
z	—	—	0.20
z1	—	—	0.11
aaa	0.25		
bbb	0.10		
ccc	0.10		
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-DFN2020-6/SWP (Type UXG)



Dimensions	Value (in mm)
C	0.650
X	0.350
X1	0.480
X2	1.050
X3	1.700
Y	0.425
Y1	0.800
Y2	1.200
Y3	1.400
Y4	2.250

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