# SINGLE-CHIP SYNC-BUCK CONTROLLER WITH USB PD3.1 SOURCE CONTROLLER

## Description

The APK43070 is a single-chip synchronous buck controller (SBC) with USB Type-C® PD3.1 source controller to support standard power range (SPR)/programmable power supply (PPS) up to 21V, and extended power range (EPR)/adjustable voltage supply (AVS) up to 28V. It is targeted for DC power provider and control of single-port or multiple-port charging applications.

The compact buck controller in APK43070 is a constant frequency synchronous step-down controller with high driving capability, optimized dead time, and high driving gate voltage to cover middle- and high-power charging with integrated drivers for external N-MOSFETs. To further enhance the converter power efficiency, the VIN DC power pass-through mode is supported.

The APK43070 integrates the SBC and PD3.1 decoder functions and results in small footprint and reduced PCB size for high-power-density charging applications. By leveraging the MOS switches of synchronous buck regulation, the PD output MOS switch for each port could be saved to reduce BOM cost.

To support higher power efficiency, extremely low standby power, and smart power sharing for multiple-port applications without the need of external MCU, the APK43070 integrates I2C interface, master/slave addressing scheme, and interrupt/wake-up mechanism. Up to 8 port addresses are supported through resistor selection.

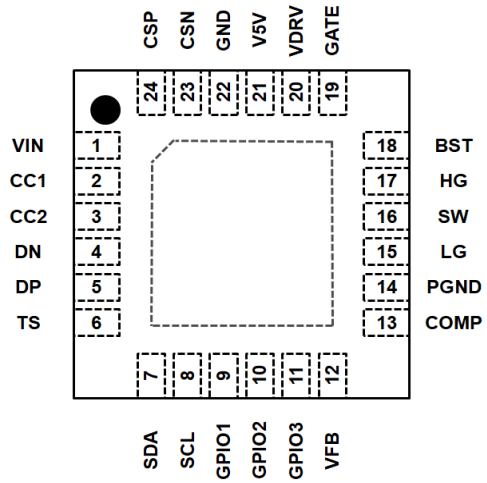
Due to its high-voltage process, the APK43070 offers VBUS short protection on CC1/CC2 pins up to 30V. Meanwhile, the APK43070 provides comprehensive safety protection, including overvoltage protection (OVP), overcurrent protection (OCP), overtemperature protection (OTP), and moisture detection of the connector.

## Applications

- Extremely low standby power multiple-port Type-C PD3.1 SPR and EPR chargers, adapters, power strips or power hubs
- Type-C PD3.1 SPR and EPR charging for high-voltage battery of portable outdoor generators
- Type-C PD3.1 SPR and EPR chargers for general-purpose charging applications

## Pin Assignments

(Top View)




W-QFN4040-24 (Type A1)

## Features

- Single-Chip Buck Controller with Type-C PD3.1 Source Controller
- Support USB PD3.1 EPR/AVS Up to 28V, SPR/PPS Up to 21V
- Operating Switching Frequency is 125kHz/250kHz/400kHz Configurable via GPIO3
- Support Power Sharing Through I2C
- Support High PWM Duty Cycle Up to 95% @125kHz/90% @ 400kHz
- Operating Input Voltage 4V to 36V
- Support Bypass Mode to Enhance Output Power Efficiency
- Frequency Dithering for EMI Restraining
- Support Legacy BC1.2, and QC3.0/4/4+/5.0
- Support External OTP by TS Pin
- Support I2C-Based Topology Up to 8 Ports Without External MCU
- Support I2C Addresses Up to 8 and Assigned by GPIO1
- Support PDO Profiles Selected by GPIO2
- Support Extremely Low Standby Power (< 120μA) with Wake-up
- Support Comprehensive Protection Schemes — OVP, UVP, OCP, OTP and Moisture Detection of the Connector with Autorecovery
- VBUS Short Protection on CC1/CC2 and DP/DN Pins Up to 30V
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/**

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

## Typical Applications Circuit

The APK43070, a high-integration synchronous buck controller with USB PD3.1 EPR decoder, supports either single-port charging or multiple-port charging at optimal system BOM with extremely low standby power consumption.

The buck controller in APK43070 is a constant frequency synchronous step-down controller to cover middle- and high-power charging with integrated low-side and high-side drivers for external N-channel MOSFETs. The internal regulator supplies internal bias rails as well as the MOSFET gate drivers. The PWM control scheme is based on voltage-mode control, and provides output current limiting capability by monitoring the voltage drop across the sense resistor between CSP and CSN pins. During normal operation, the output voltage is internally sensed through a resistive divider at FB pin, and a capacitor connected between VFB and VBUS is needed. The amplifier output pin, COMP, is connected to a compensation circuitry for loop stability. To enhance the converter power efficiency, the VIN DC power pass-through is supported by a bypass mode from the GATE pin.

For multiple ports PD3.1 charging application, the APK43070 supports smart power sharing operation up to 8 ports without the need of an extra MCU. Figure 1 shows the multi-port PD3.1 charging topology with APK43070. It uses I2C interface, interrupt and wake-up mechanism, master/slave addressing scheme, and low standby power design approach to optimize system BOM cost and power efficiency.

All the power sharing operations are going through I2C interface bus to communicate between the master and each slave port. Any attach/detach or event happening will initiate an interrupt signal to wake up the master stage to do adjustment. The I2C master and slave address for all APK43070 are set by connecting an associated resister value on GPIO1 pin, and up to 8 addresses are supported.

Just like the one-port solution, the PD output VBUS MOS switch for each port can be saved by leveraging the MOS switches of the synchronous buck controller. Meanwhile, the APK43070 has built-in source PDO power profiles, and could be selected by connecting a corresponding resistor to a pre-determined pin. If the number of pins is limited, the PDO could be pre-fixed through firmware code assignment.

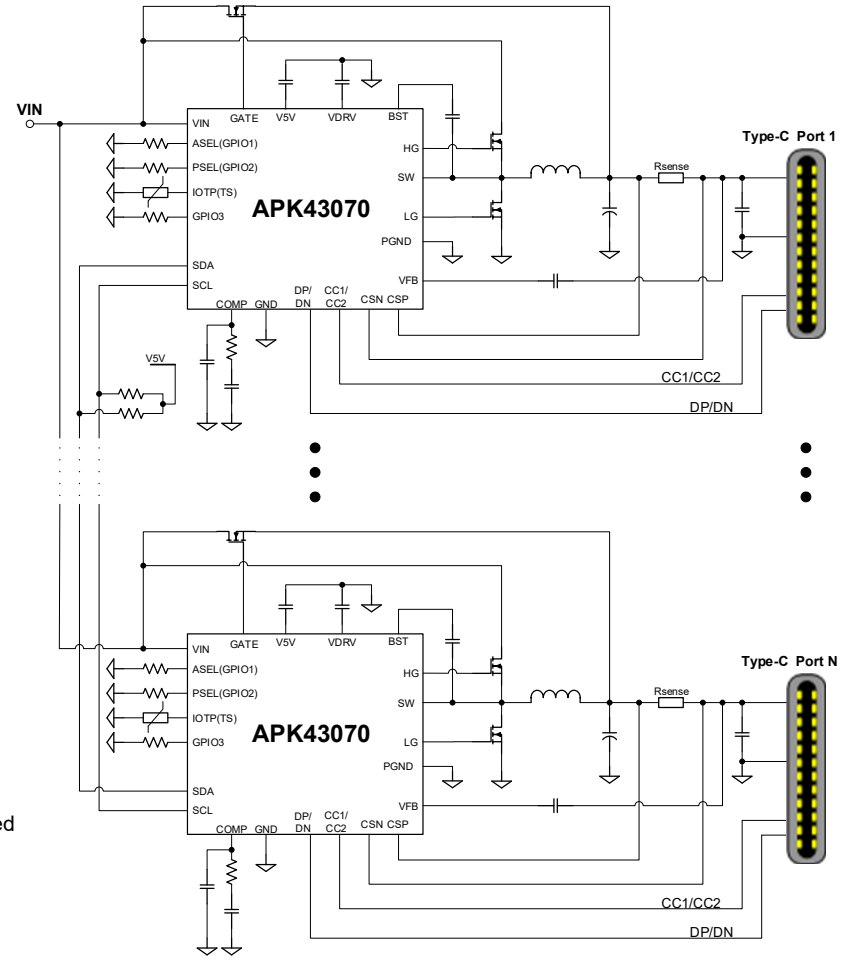



Figure 1. The APK43070 Circuit Topology Used for Multi-Port PD3.1 Charging Application

**APK43070 Multi-Port PD3.1 Solution Key Features:**

1. No additional MCU, and up to 8 ports supported
2. No VBUS switch MOSFET to reduce total BOM
3. I2C address selected by resistor
4. Power sharing controlled through I2C bus
5. PDO power profile selected by resistor or pre-fixed
6. PD3.1 EPR/AVS up to 28V, SPR/PPS up to 21V

## Pin Descriptions

| Pin Number | Pin Name | Function |
|---|---|---|
| 1 | VIN | Power-supply input pin |
| 2 | CC1 | Type-C_CC1 |
| 3 | CC2 | Type-C_CC2 |
| 4 | DN | Type-C_DN |
| 5 | DP | Type-C_DP |
| 6 | TS | Used as temperature sensing by connecting an external NTC resistor. |
| 7 | SDA | I2C interface data pin. Logic-level input/output. |
| 8 | SCL | I2C interface clock pin. Logic-level input/output. |
| 9 | GPIO1 | Current source output to resistor for I2C address selection. |
| 10 | GPIO2 | Current source output to resistor for PDO power profile selection. |
| 11 | GPIO3 | Current source output to resistor for switching frequency selection. |
| 12 | VFB | VOUT feedback input pin. Connecting a capacitor between VFB and VBUS |
| 13 | COMP | Compensation pin. It is used to compensate for the voltage regulation control loop. Connect a series RC network from COMP pin to GND. |
| 14 | PGND | Power ground of the IC. The high-current ground connection to the low-side gate drivers. |
| 15 | LG | Output of the low-side gate driver |
| 16 | SW | Switching node. It is connected to inductor and power MOSFETs. |
| 17 | HG | Output of the high-side gate driver |
| 18 | BST | High-side gate drive boost input. A 100nF or larger capacitor should be connected from BST to SW. |
| 19 | GATE | Gate driver for bypass MOSFET |
| 20 | VDRV | Power supply for drivers |
| 21 | V5V | LDO 5V output |
| 22 | GND | Ground pin |
| 23 | CSN | Negative input of current-sense amplifier |
| 24 | CSP | Positive input of current-sense amplifier |

Table 1. The Mapping Table Between Pin Sequence Number and Pin Name

## Functional Block Diagram

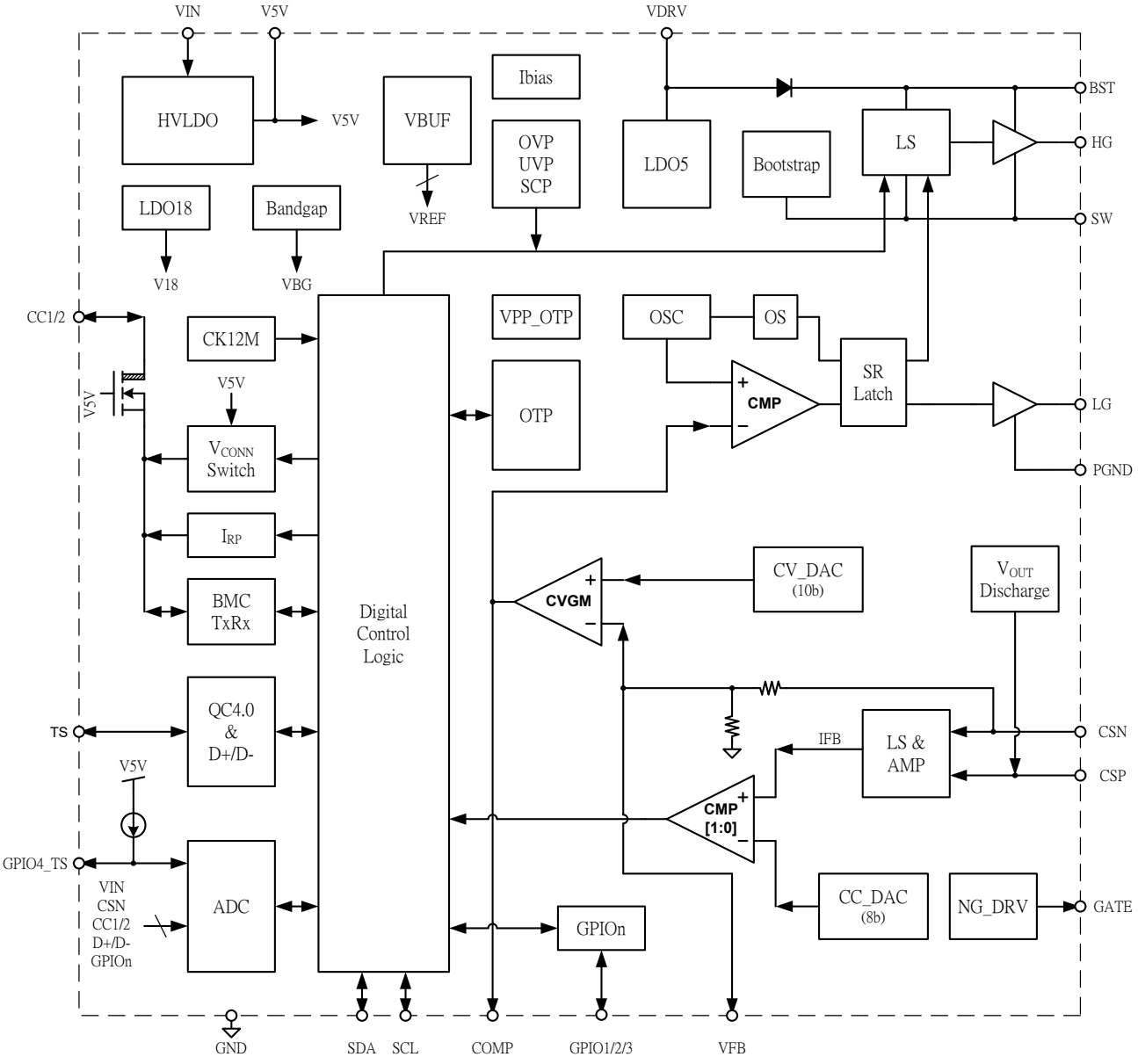



Figure 2. The APK43070 Block Diagram

## Absolute Maximum Ratings (@$T_A$ = +25°C, unless otherwise specified.) (Note 4)

| Symbol | Parameter | Rating | Unit |
|---|---|---|---|
| $V_{VIN}$ | Power-Supply Voltage at VIN Pin | -0.3 to 40 | V |
| $V_{GATE}$ | Voltage at GATE Pin | -0.3 to 40 | V |
| $V_{SW}$, $V_{HG}$ | Voltage at SW, HG Pins | -0.3 to 40 | V |
| $V_{BST}$ | Voltage at BST Input | -0.3 to $V_{SW}$ + 6 | V |
| $V_{CSN}$, $V_{CSP}$ | Voltage at CSN, CSP Pins | -0.3 to 40 | V |
| $V_{CC1}$, $V_{CC2}$ | Voltage at CC1, CC2 Pins | -0.3 to 30 | V |
| $V_{DP}$, $V_{DN}$ | Voltage at DP, DN Pins | -0.3 to 30 | V |
| — | Voltage at Other Pins (Note 5) | -0.3 to 6 | V |
| $T_J$ | Operating Junction Temperature | -40 to +150 | °C |
| $T_{STG}$ | Storage Temperature | -65 to +150 | °C |
| $T_{LEAD}$ | Lead Temperature (Soldering, 10s) | +300 | °C |
| ESD | Human Body Model | 2000 | V |
| ESD | Charged Device Model | 750 | V |

Notes: 4. Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to *Absolute Maximum Ratings* for extended periods can affect device reliability.
5. When GPIO1-3, SDA, SCL, TS pins are pulled high to a voltage source, it is strongly recommended to series a resistor with minimum 10k value.

## Package Thermal Information (Note 6)

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-Ambient Thermal Resistance | 25.5 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-Case (Top) Thermal Resistance | 17.4 | °C/W |
| $R_{\theta JB}$ | Junction-to-Board Thermal Resistance | 6.1 | °C/W |
| $\Psi_{JT}$ | Junction-to-Top Characterization Parameter | 0.2 | °C/W |
| $\Psi_{JB}$ | Junction-to-Board Characterization Parameter | 7.9 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-Case (Bottom) Thermal Resistance | 2.2 | °C/W |

Note: 6. Test condition: device mounted on FR-4 substrate PC board, 2oz copper, with the minimum footprint.

## Recommended Operating Conditions (Note 7)

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| VIN | Supply Voltage | 4.0 | 36 | V |
| VOUT | Output Voltage | 1.0 | 28 | V |
| $T_A$ | Operating Ambient Temperature | -40 | +85 | °C |
| $T_J$ | Operating Junction Temperature | -40 | +125 | °C |

Note: 7. The device function is not guaranteed outside of the recommended operating conditions.

## Electrical Characteristics (@$T_A$ = +25°C, $V_{IN}$ = 12V, unless otherwise specified.)

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **VIN Pin & Internal Bias Section** | | | | | | |
| $V_{VIN\_ON}$ | VIN Turn-On Threshold | — | 3.5 | 4 | 4.3 | V |
| $V_{HYS}$ | VIN Hysteresis | — | — | 0.5 | — | V |
| $I_{PD}$ | Power-Down Mode Current | — | — | 400 | — | μA |
| $I_{OP}$ | Operating Supply Current | — | 1 | 2.3 | 3.5 | mA |
| $I_{DISCHG\_VOUT}$ | Discharge Current for VOUT | $V_{CSP}$ = 5V | 70 | 130 | 170 | mA |
| **V5V & CV Function** | | | | | | |
| V5V | LDO 5V Output | — | 4.75 | 5.0 | 5.25 | V |
| $I_{V5VOCP}$ | V5V Overcurrent Protection | — | 20 | — | 50 | mA |
| $V_{VBUS\_CV5}$ | VBUS Voltage for 5V CV Control | — | 4.85 | 5 | 5.15 | V |
| $V_{VBUS\_CV9}$ | VBUS Voltage for 9V CV Control | — | 8.73 | 9 | 9.27 | V |
| $V_{VBUS\_CV20}$ | VBUS Voltage for 20V CV Control | — | 19.4 | 20 | 20.6 | V |
| $V_{VBUS\_CV28}$ | VBUS Voltage for 28V CV Control | — | 26.6 | 28 | 29.4 | V |
| **Current-Sense Function** | | | | | | |
| $CC_{3A5}$ | Current Sense and CC Loop Correction | $R_{SEN}$ = 5mΩ, $I_L$ = 3A | 13.5 | 15 | 16.5 | mV |
| $OCP_{110}$ | Overcurrent Protection (110%) | — | 3 | 3.3 | 3.6 | A |
| **CC1/CC2 Pin Section** | | | | | | |
| $V_{OH\_CCX}$ | Pull High Voltage of CCx | — | 3.0 | 3.3 | 3.6 | V |
| $I_{rp\_330}$ | Source Current of CCx | $R_D$ = 5.1kΩ | 303.6 | 330 | 356.4 | μA |
| $I_{rp\_180}$ | Source Current of CCx | $R_D$ = 5.1kΩ | 165.6 | 180 | 194.4 | μA |
| $I_{rp\_80}$ | Source Current of CCx | $R_D$ = 5.1kΩ | 73.6 | 80 | 86.4 | μA |
| $V_{SWH\_TxDC}$ | Voltage Swing High of CCx for BMC Tx | (Note 8) | 1.05 | 1.125 | 1.2 | V |
| $V_{SWL\_TxDC}$ | Voltage Swing Low of CCx for BMC Tx | (Note 8) | — | — | 75 | mV |
| $t_{R\_Tx}$ | Rising Time of CCx for BMC Tx | (Note 8) | 300 | — | — | ns |
| $t_{F\_Tx}$ | Falling Time of CCx for BMC Tx | (Note 8) | 300 | — | — | ns |
| $V_{ATH\_C}$ | Attach Sensing Voltage of Type-C | (Note 8) | 0.27 | — | 2.25 | V |
| **DP/DN Pin Section** | | | | | | |
| $V_{DP\_APP}$ | DP Apple Mode Output Voltage | (Note 8) | — | 2.68 | — | V |
| $V_{DN\_APP}$ | DN Apple Mode Output Voltage | (Note 8) | — | 2.68 | — | V |
| $V_{DP\_0P6V}$ | DP 0.6V Output Voltage | Source Current 250μA | — | 0.6 | — | V |
| $V_{DN\_0P6V}$ | DN 0.6V Output Voltage | Source Current 250μA | — | 0.6 | — | V |
| $R_{DP\_DWM20K}$ | DP 20k Pulldown Resistor | — | 16 | 20 | 24 | kΩ |
| $R_{DN\_DWM20K}$ | DN 20k Pulldown Resistor | — | 16 | 20 | 24 | kΩ |
| $R_{DP\_DWM900K}$ | DP 900k Pulldown Resistor | — | 700 | 900 | 1200 | kΩ |
| $R_{DN\_DWM900K}$ | DN 900k Pulldown Resistor | — | 700 | 900 | 1200 | kΩ |
| $R_{DPDN\_short}$ | DPDN Short Resistor | — | 5 | 20 | 40 | Ω |
| $R_{DN\_IMP}$ | Impedance Checks at DN | — | 100 | 275 | 505 | Ω |
| $V_{OH\_DP/DN}$ | Output High Threshold Voltage of DP/DN | Source Current 2mA | 2.9 | 3.1 | 3.3 | V |
| $V_{OL\_DP/DN}$ | Output Low Threshold Voltage of DP/DN | Sink Current 2mA | — | — | 300 | mV |

Note: 8. Guaranteed by design.

## Electrical Characteristics (continued) (@$T_A$ = +25°C, $V_{IN}$ = 12V, unless otherwise specified.)

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Digital I/O Pin Section (GPIO1/2/3)** | | | | | | |
| $V_{IH}$ | Input High Threshold Voltage of GPIOx | — | 1.4 | — | — | V |
| $V_{IL}$ | Input Low Threshold Voltage of GPIOx | — | — | — | 0.8 | V |
| $V_{OH}$ | Output High Level Voltage of GPIOx | Source Current 2mA | 4.3 | — | — | V |
| $V_{OL}$ | Output Low Level Voltage of GPIOx | Sink Current 2mA | — | — | 300 | mV |
| $t_R$ | Rising Time | (Note 8) | — | — | 300 | ns |
| $t_F$ | Falling Time | (Note 8) | — | — | 300 | ns |
| $I_{TS20}$ | TS Source Current for NTC | $V_{TS}$ = 1V | 18 | 20 | 22 | μA |
| $I_{TS100}$ | TS Source Current for NTC | $V_{TS}$ = 1V | 90 | 100 | 110 | μA |
| $I_{GPX}$ | GPIO Source Current | $V_{GPIOX}$ = 1V | 18 | 20 | 22 | μA |
| **Protection** | | | | | | |
| $V_{OVP5}$ | 5V VBUS Overvoltage Protection | — | 5.5 | 6 | 6.5 | V |
| $V_{OVP9}$ | 9V VBUS Overvoltage Protection | (Note 8) | — | 10.8 | — | V |
| $V_{OVP15}$ | 15V VBUS Overvoltage Protection | (Note 8) | — | 18 | — | V |
| $V_{OVP20}$ | 20V VBUS Overvoltage Protection | (Note 8) | — | 24 | — | V |
| $V_{OVP28}$ | 28V VBUS Overvoltage Protection | (Note 8) | 28.6 | 30.8 | 33 | V |
| $V_{UVP5}$ | 5V VBUS Undervoltage Protection | — | 3.5 | 4 | 4.4 | V |
| $V_{UVP9}$ | 9V VBUS Undervoltage Protection | (Note 8) | — | 7.2 | — | V |
| $V_{UVP15}$ | 15V VBUS Undervoltage Protection | (Note 8) | — | 12 | — | V |
| $V_{UVP20}$ | 20V VBUS Undervoltage Protection | (Note 8) | — | 16 | — | V |
| $V_{UVP28}$ | 28V VBUS Undervoltage Protection | (Note 8) | — | 22.4 | — | V |
| TSD | Thermal Shutdown | (Note 8) | — | +145 | — | °C |
| $T_{HYS}$ | Temperature Hysteresis | (Note 8) | — | +30 | — | °C |

Note: 8. Guaranteed by design.

## Electrical Characteristics (continued) (@$T_A$ = +25°C, $V_{IN}$ = 12V, unless otherwise specified.)

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **GATE DRIVER** | | | | | | |
| $V_{HG\_L}$ | Low-State Voltage Drop | $V_{HG}$ – $V_{SW}$, 100mA Sinking | 0.05 | 0.1 | 0.2 | V |
| $V_{HG\_H}$ | High-State Voltage Drop | $V_{BST}$ – $V_{HG}$, 100mA Souring | 0.1 | 0.2 | 0.42 | V |
| $V_{LG\_L}$ | Low-State Voltage Drop | $V_{LG}$, 100mA Sinking | 0.07 | 0.1 | 0.3 | V |
| $V_{LG\_H}$ | High-State Voltage Drop | $V_{VDRV}$ – $V_{LG}$, 100mA Souring | 0.1 | 0.2 | 0.42 | V |
| $V_{GATE}$ | Gate Voltage for Bypass Mode | $C_g$ = 10nF | $V_{VIN}$ + 3 | $V_{VIN}$ + 4 | $V_{VIN}$ + 5 | V |
| **Operation Frequency** | | | | | | |
| $f_{SW1}$ | Switching Frequency 1 | — | 112.5 | 125 | 137.5 | kHz |
| $f_{SW2}$ | Switching Frequency 2 | — | 225 | 250 | 275 | kHz |
| $f_{SW3}$ | Switching Frequency 3 | — | 315 | 350 | 385 | kHz |
| $f_{SW4}$ | Switching Frequency 4 | — | 360 | 400 | 440 | kHz |
| **SPREAD SPECTRUM** | | | | | | |
| $f_{DITH}$ | Frequency Dithering Span | (Note 8) | — | +21 | — | % |
| **VDRV** | | | | | | |
| $V_{VDRV}$ | Internal Driver Regulator Output | $I_{VDRV}$ = 50mA, $V_{VIN}$ = 12V | 5.2 | — | 5.8 | V |
| $V_{VDRV\_DO}$ | VDRV Dropout | $I_{VDRV}$ = 50mA | 80 | — | 350 | mV |
| **ERROR AMPLIFIER** | | | | | | |
| $I_{SINK}$ | COMP Pin Sink Current | $V_{FB}$ = $V_{DAC}$ + 400mV, $V_{COMP}$ = 1.5V | 20 | — | 60 | µA |
| $I_{SOURCE}$ | COMP Pin Source Current | $V_{FB}$ = $V_{DAC}$ – 400mV, $V_{COMP}$ = 1.5V | 20 | — | 60 | µA |
| $G_{EA}$ | Error Amplifier Transconductance | $V_{FB}$ = $V_{DAC}$ – 100mV, $V_{COMP}$ = 1.5V | 170 | — | 370 | µA/V |
| | | $V_{FB}$ = $V_{DAC}$ + 100mV, $V_{COMP}$ = 1.5V | 170 | — | 370 | µA/V |

Note: 8. Guaranteed by design.

## Application Information

### Function Description

The APK43070 integrates a synchronous buck controller with USB Type-C PD3.1 source controller. It supports SPR/PPS up to 100W, and EPR/AVS up to 140W. The APK43070 is targeted for high-power-density charging products with high power efficiency and extremely low standby power and addressing to multiple-port charging application up to 8 ports without the need of external MCU.

### Synchronous Buck Controller in APK43070

The compact buck controller in APK43070 is a constant frequency synchronous step-down controller. It integrates drivers for external N-MOSFETs, and is shooting for higher power efficiency through high driving capability, optimized dead time, and high driving gate voltage to cover middle- and high-power charging.

### Switching Frequency Setting (Dedicated Function in APK43070DKZ-13-FA01)

The APK43070 provides four options for switching frequency options: 125kHz, 250kHz, 350kHz, and 400kHz. The switching frequency is configured by placing a 1% precision resister between PIN11 (GPIO3) and ground. The higher the frequency, the smaller the size of the inductor, but the lower efficiency it is. If it is necessary to pass the CISPR 25 EMI criteria for automotive applications, the 400kHz switching frequency is recommended. The mapping table is illustrated in Table 2.

| Switching Frequency | Resistance |
|---|---|
| 125kHz | 100kΩ/Floating |
| 250kHz | 66kΩ |
| 350kHz | 39kΩ |
| 400kHZ | 5.1kΩ |

Table 2. Switching Frequency Setting

### Switching Frequency Dithering

To reduce the EMI emission, the APK43070 supports PWM frequency dithering with a triangle pattern, as shown in Figure 3. The modulation amplitude of dithering is a +21% frequency boost (Fsw0 to Fsw+21%) with a modulation frequency of 4kHz typically.

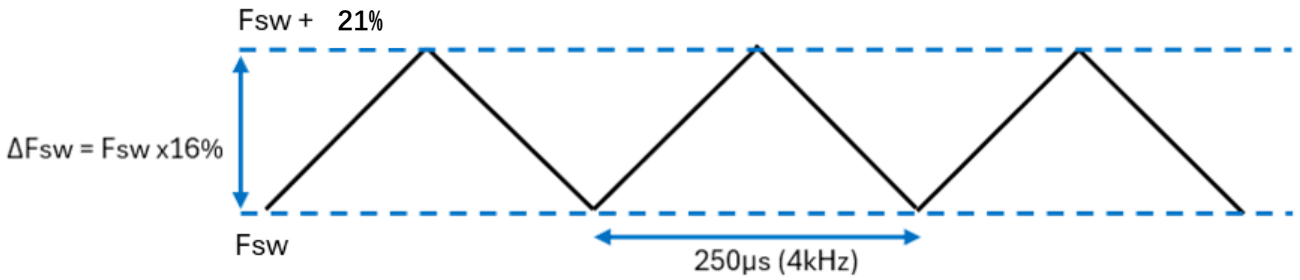



Figure 3. The PWM Frequency Dithering Used in APK43070

### Inductor Selection

For most of the system designs, the following equation can be used to calculate the inductor value:

$$L = \frac{VOUT \cdot (VIN - VOUT)}{VIN \cdot \Delta I_L \cdot f_{SW}}$$

Where:

- $\Delta I_L$ is the inductor current ripple.
- $f_{SW}$ is the buck converter switching frequency.

For APK43070 application, we can assume $\Delta I_L$ as 30% to 40% of the maximum output current of 3A.

$$I_{PEAK} = I_{LOAD} + \frac{\Delta I_L}{2}$$

The peak current determines the required saturation current rating, which affects the size of the inductor. The inductor saturation will reduce converter efficiency while increasing the temperature of the inductor and power MOSFETs. Therefore, it is important to select an inductor with an appropriate saturation current rating. For most applications, it is recommended to select an inductor of approximately 3.3μH to 22μH with a DC current rating that is at least 35% higher than the maximum load current. For maximum efficiency, the DC resistance of the inductor should be as small as possible.

## Application Information (continued)

**Input Capacitor Selection**

The input capacitor reduces both the surge current drawn from the input supply as well as the switching noise from the device. The input capacitor must sustain the ripple current produced during the on-time of the main switch. It must have a low ESR to minimize power dissipation from the RMS input current. The RMS current rating of the input capacitor is a critical parameter and must be higher than the RMS input current. As a rule of thumb, select an input capacitor with an RMS current rating greater than half of the maximum load current. The chart in Figure 4 shows the ratio of RMS current to load current vs. duty cycle.

Due to large di/dt through the input capacitor, it is better to use electrolytic or ceramic capacitors with low ESR. If the tantalum capacitor is used, surging protection should be provided, otherwise capacitor failure could occur.

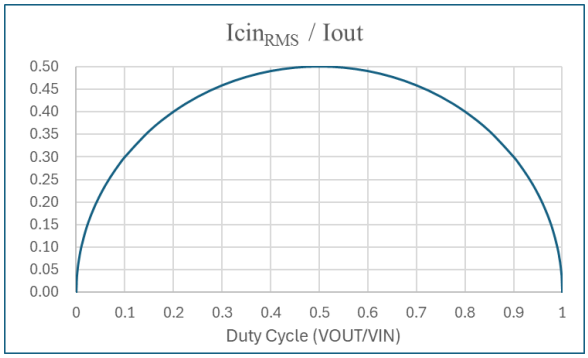



Figure 4. The Chart Shows the Ratio of RMS Current to Load Current vs. Duty Cycle

**Output Capacitor Selection**

The output capacitor keeps the output voltage ripple small, ensures feedback loop stability, and reduces both the overshoots and undershoots of the output voltage during load transients. During the first few microseconds of an increasing load transient, the converter recognizes the change from steady state and enters 100% duty cycle to supply more current to the load. However, the inductor limits the change to increasing current depending on its inductance. Therefore, the output capacitor supplies the difference in current to the load during this time. Likewise, during the first few microseconds of a decreasing load transient, the converter recognizes the change from steady state and sets the on-time to minimum to reduce the current supplied to the load. However, the inductor limits the change in decreasing current as well. Therefore, the output capacitor absorbs the current ripples due to the inductor during this time.

The effective requested output capacitance, COUT, can be calculated from the equations below, where the ESR of the output capacitor dominates the output voltage ripple:

$$VOUT_{Ripple} = \Delta I_L \cdot \left( ESR + \frac{1}{8 \cdot f_{SW} \cdot COUT} \right)$$

The output capacitors with large capacitance and low ESR are the best option. For APK43070, a polymer capacitor of 100μF is recommended. To meet the load transient requirements, the calculated COUT should satisfy the following inequality:

$$COUT > max\left( \frac{L \cdot I_{Trans}^2}{\Delta V_{Overshoot} \cdot VOUT}, \frac{L \cdot I_{Trans}^2}{\Delta V_{Undershoot} \cdot (VIN - VOUT)} \right)$$

Where:

- $I_{Trans}$ is the load transient.
- $\Delta V_{Overshoot}$ is the maximum output overshoot voltage.
- $\Delta V_{Udershoot}$ is the maximum output undershoot voltage.

## Application Information (continued)

### Soft-Start

The soft-start circuitry controls the output voltage slope to prevent excessive inrush current, maintain a controlled output voltage, and avoid unwanted voltage overshoots and drops during the startup of power management IC. The APK43070 ramps up its output voltage to 5V at 30ms at a controlled slew rate.

### Compensator

The APK43070 has an OTA error amplifier to perform output regulation. The COMP pin is the output of the error amplifier where a type-III compensator network is suggested as shown in Figure 5. The type-III compensator produces two zeros and poles that can be calculated with the equations below.

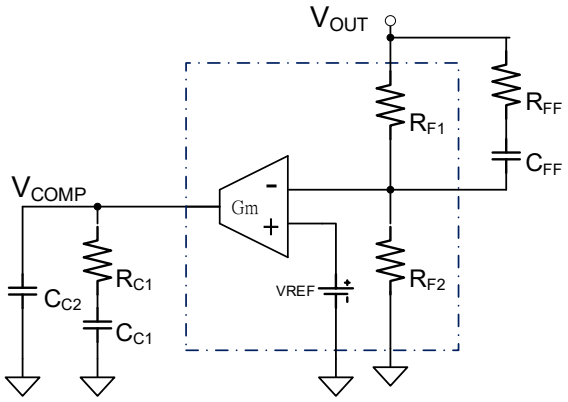



Figure 5. Type-III Compensator Network is Suggested to Connect at COMP Pin and FB Pin

$$f_{Z1} = \frac{1}{2\pi R_1 C_1} \qquad f_{Z2} = \frac{1}{2\pi (R_{F1} + R_{FF}) C_{FF}}$$

$$f_{P1} = \frac{1}{2\pi \left(\frac{R_{F1} R_{F2}}{R_{F1} + R_{F2}} + R_{FF}\right) C_{FF}} \qquad f_{P2} = \frac{(C_{C1} + C_{C2})}{2\pi R_{C1} C_{C1} C_{C2}}$$

The type-III compensator as below is recommended:

$$C_{C1} = 4.7nF \quad R_{C1} = 47k\Omega \quad C_{C2} = 22pF \quad C_{FF} = 470pF \quad R_{FF} = 0$$

$$f_{Z1} = 720 \quad f_{Z2} = 3.76k \quad f_{P1} = 37.6k \quad f_{P2} = 154k$$

### Output Active Discharge

The APK43070 has built-in output discharge in CSP pin. When the output voltage transits from a high level to a low level, the CSP pin sinks a current of 130mA to discharge the output capacitor.

### PCB Layout Guide

PCB layout is critical to achieve stable operation. It is highly recommended to duplicate the EVB layout for optimum performance.

If changes are necessary, please follow these guidelines:

i. Keep the path of switching current short and minimize the loop area formed by the input cap, high-side MOSFET and low-side MOSFET.
ii. $V_{CC}$ bypass ceramic capacitors are suggested to be put close to the $V_{CC}$ pin.
iii. It recommends using a four-layer PCB and pouring ground in mid-layer to shield radiated noises.
iv. Adding the snubber circuit across the high side MOSFET (Drain - Source) is suggested to reduce the SW spike.
v. Rout the CSN and CSP traces to the current sensing resistor close together as a differential pair, using a Kelvin connection to reduce the line drop error.

## Application Information (continued)

**PD3.1 Controller in APK43070**

The PD3.1 EPR decoder in APK43070 combines internal MCU-based flexibility and hardware off-load speed to support multiple-port charging up to 8 ports without the external MCU. Not only PD3.1 SPR/PPS, EPR/AVS protocols are supported, but also BC1.2, and QC3.0/4/4+/5.0 could be included. Besides, the APK43070 provides comprehensive safety protection.

**I2C Interface and Address Setting**

The APK43070 supports I2C communication between master to each port through SDA, SCL pins. To support extremely low standby power, and smart power sharing for up to 8-ports applications, the APK43070 implements a wake-up and interrupt mechanism to improve the I2C communication efficiency as shown in Figure 6. To support master/slave addressing scheme up to 8 ports, the addresses can be set by connecting an associated 1% precision resistor between GPIO1 and ground. The mapping table is illustrated in Table 3.

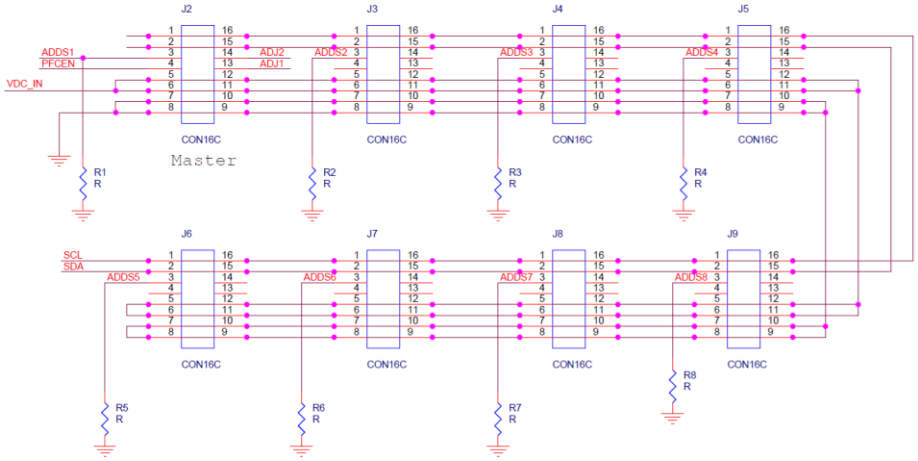



Figure 6. The APK43070-Based Multi-Port Charger Application Can Support Up to 8 Ports Without External MCU

| Master/Slave | Resistance(Ω) | I2C Address | Port Number |
|---|---|---|---|
| Master | 100k/Floating | — | 0 |
| Slave #1 | 82k | 0x51 | 1 |
| Slave #2 | 66k | 0x52 | 2 |
| Slave #3 | 52k | 0x53 | 3 |
| Slave #4 | 39k | 0x54 | 4 |
| Slave #5 | 26k | 0x55 | 5 |
| Slave #6 | 15k | 0x56 | 6 |
| Slave #7 | 5.1k | 0x57 | 7 |

Table 3. The Mapping Table Between I2C Master/Slave Address and Its Corresponding Resistor Value

**Power Sharing (Dedicated Configuration in APK43070DKZ-13-FA01)**

The APK43070DKZ-13-FA01 has built-in power sharing function. The power sharing principles are as bellows. In multiple ports application, customers need to set up each APK43070's PDO the same as the maximum total power of the whole system. If only one device is attached, this device will get the maximum total power of the whole system no matter which port is attached. If more than one device is attached, master port will get the power sharing priority than slave port. Among slave ports, the port with front numbering will get the power sharing priority. For standard firmware in APK43070DKZ-13-FA01, the port numbers are limited in "0,1,2,3" in Table 3.

| Maximum Total Power = 140W (28V, 5A) | | | | |
|---|---|---|---|---|
| Attach Port(s) | PortX | PortX | PortX | PortX |
| *1 | 140W | | | |
| *2 | 65W | 65W | | |
| *3 | 65W | 45W | 30W | |
| *4 | 65W | 30W | 20W | 20W |

| Maximum Total Power = 100W (20V, 5A) | | | |
|---|---|---|---|
| Attach Port(s) | PortX | PortX | PortX |
| *1 | 100W | | |
| *2 | 65W | 30W | |
| *3 | 45W | 30W | 20W |

| Maximum Total Power = 65W (20V, 3.25A) | | | |
|---|---|---|---|
| Attach Port(s) | PortX | PortX | PortX |
| *1 | 65W | | |
| *2 | 45W | 20W | |
| *3 | 30W | 15W | 15W |

Table 4. Power Sharing Principle of APK43070DKZ-13-FA01

## Application Information (continued)

**PDO Power Profile Selection (Dedicated Configuration in APK43070DKZ-13-FA01)**

The APK43070 has built-in source PDO power profiles and could be selected by connecting a corresponding 1% precision resistor to the pre-determined GPIO2 pin. If the number of pins is limited, the PDO table could be pre-fixed through firmware code assignment. There is a total of 8 PDO power profiles in the OTP memory of the APK43070, as shown in Table 5.

| Power Profile No | Resistance | PDO | Power Data | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | SPR Fixed PDO | | | | SPR AVS | | SPR PPS | | EPR Fixed PDO | EPR AVS PDO |
| 1 | 5.1 KΩ | 15W | 5V / 3A | 9V / 1.66A | | | | | | | | |
| 2 | 15 KΩ | 20W | 5V / 3A | 9V / 2.22A | | | | | 5V~11V / 2.2A | | | |
| 3 | 26 KΩ | 30W | 5V / 3A | 9V / 3A | 15V / 2A | | 9V~15V / 2A | | 5V~11V / 3A | 5V~16V / 2A | | |
| 4 | 39 KΩ | 45W | 5V / 3A | 9V / 3A | 15V / 3A | 20V / 2.25A | 9V~15V / 3A | 15V~20V / 2.25A | 5V~16V / 3A | 5V~21V / 2.25A | | |
| 5 | 52 KΩ | 60W | 5V / 3A | 9V / 3A | 15V / 3A | 20V / 3A | 9V~15V / 3A | 15V~20V / 3A | 5V~16V / 4A | 5V~21V / 3A | | |
| 6 | 66 KΩ | 65W | 5V / 3A | 9V / 3A | 15V / 3A | 20V / 3.25A | 9V~15V / 3A | 15V~20V / 3.25A | 5V~16V / 4A | 5V~21V / 3.25A | | |
| 7 | 82 KΩ | 100W | 5V / 3A | 9V / 3A | 15V / 3A | 20V / 5A | 9V~15V / 3A | 15V~20V / 5A | 5V~21V / 5A | | 28V / 3.5A | 15~28V / 100W |
| 8 | 100KΩ/Floating | 140W | 5V / 3A | 9V / 3A | 15V / 3A | 20V / 5A | 9V~15V / 3A | 15V~20V / 5A | 5V~21V / 5A | | 28V / 5A | 15~28V / 140W |

Table 5. The PDO Data in APK43070 Supports PD3.1 SPR/PPS and EPR/AVS Up to 140W

**Safety Protections**

Based on high-voltage process, the APK43070 offers VBUS short protection on CC1/CC2 pins up to 30V. In addition, the APK43070 provides comprehensive safety protection, including OVP, UVP, OCP, and OTP. The connector moisture detection between DP and DN pins can also be supported. When the safety protection is triggered on, the VBUS is disconnected from VIN or ground by turning off the high/low NMOS switches of the buck controller, and provides a path for VBUS to discharge to ground. Besides, the system will recover automatically after the shutdown.

**OCP**

The APK43070 supports OCP to control the output load condition by monitoring the output current through detection of IR drop on the 5mΩ current-sense resistor. Once the load draws more current than the OCP threshold level for a duration longer than the debounce time, the APK43070 triggers the UVP protection by immediately issuing a Hard_Reset command, then turning off VBUS and providing a discharge path.

**OVP and UVP**

The OVP threshold is set at 120% of the PDO voltage and can be adjusted slightly. When the VBUS voltage is higher than OVP threshold and lasts longer than the debounce time, the APK43070 triggers the OVP protection by turning off VBUS and provides a discharge path for VBUS. Furthermore, a fast OVP is embedded by monitoring the voltage on VFB, the VOUT feedback input pin. If the voltage stays below a pre-determined threshold for a duration, VBUS overvoltage protection will be triggered immediately.

The UVP is provided when the VBUS voltage remains lower than 80% of pre-determined PDO voltage and lasts longer than the debounce time. The APK43070 triggers the UVP protection by turning off VBUS and provides a discharge path.

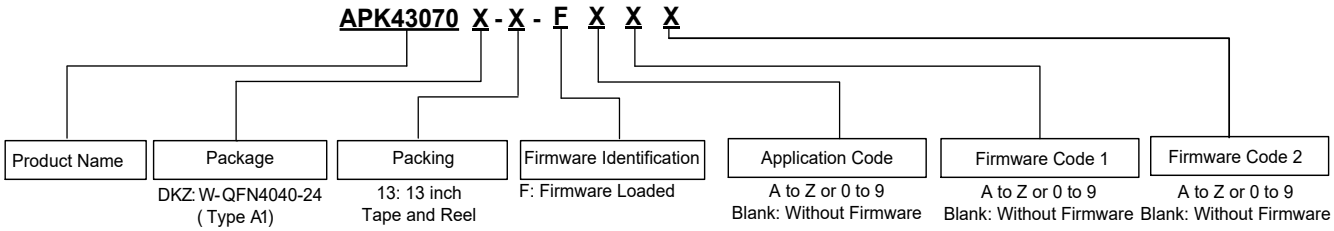
**Internal OTP**

The OTP is supported via IC internal junction temperature detection with the +145°C threshold and +30°C hysteresis by default. When the temperature goes beyond the internal OTP threshold, the APK43070 triggers the OTP protection by turning off VBUS and provides a discharge path for VBUS. When the chip temperature cools down 30°C below the threshold, the VOUT is recovered automatically.

**External OTP (Dedicated Configuration in APK43070DKZ-13-FA01)**

The external OTP could be supported with an NTC thermistor connected between TS pin and ground near the potential hot spot. There is a 100μA current source from TS pin. External OTP threshold is set to 100mV. OTP function will be triggered when the voltage on TS pin is lower than 100mV and the OTP function is cleared when the voltage raises over 130mV.

## Ordering Information (Note 9)



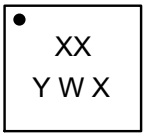

| Orderable Part Number | Package | Identification Code | Firmware Inside | Packing | |
|---|---|---|---|---|---|
| | | | | Qty. | Carrier |
| APK43070DKZ-13-FA01 | W-QFN4040-24 (Type A1) | K3 | Standard Firmware (Function as Described in Datasheet) | 3,000 | 13” Tape & Reel |
| APK43070DKZ-13-FXXX | | | Customized Firmware | | |

Note: 9. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

## Marking Information

**W-QFN4040-24 (Type A1)**

**(Top View)**

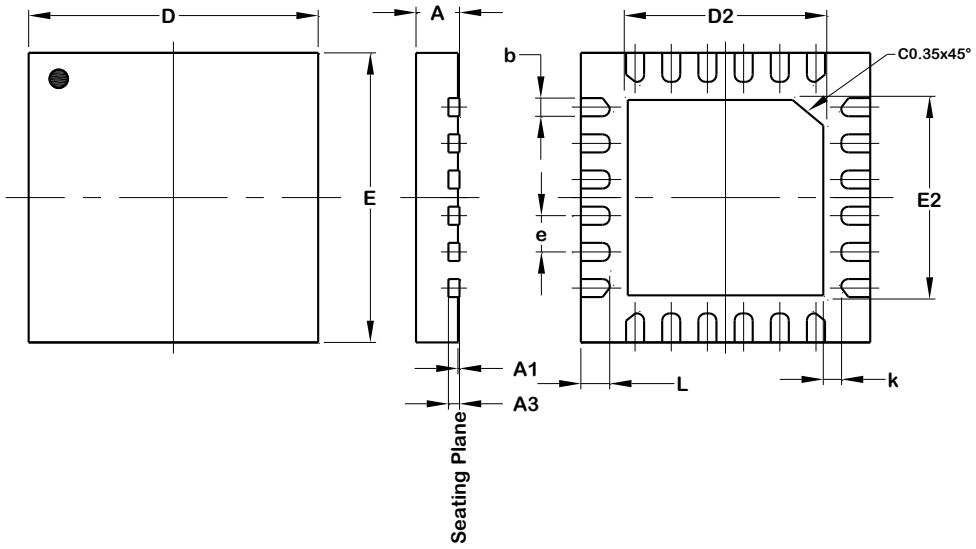



XX : Identification Code
Y : Year : 0~9
W : Week : A~Z : week 1~26; a~z : week 27~52; z represents week 52 and 53
X : Internal Code

## Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

**W-QFN4040-24 (Type A1)**

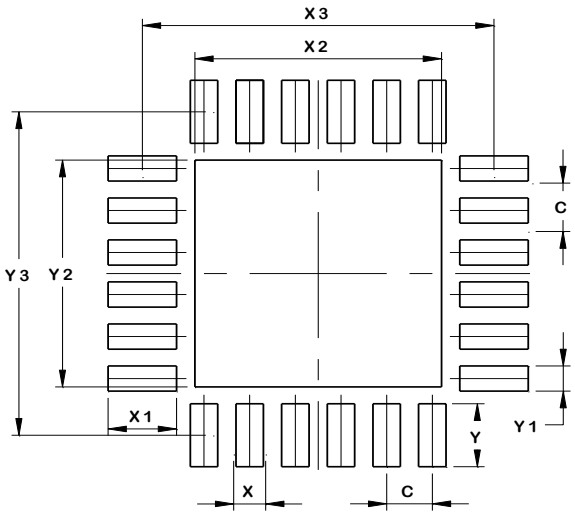



| W-QFN4040-24 (Type A1) | | | |
|---|---|---|---|
| **Dim** | **Min** | **Max** | **Typ** |
| **A** | 0.70 | 0.80 | 0.75 |
| **A1** | 0.00 | 0.05 | 0.02 |
| **A3** | 0.203 REF | | |
| **b** | 0.18 | 0.30 | 0.25 |
| **D** | 4.00 BSC | | |
| **D2** | 2.65 | 2.75 | 2.70 |
| **E** | 4.00 BSC | | |
| **E2** | 2.65 | 2.75 | 2.70 |
| **e** | 0.50 BSC | | |
| **k** | 0.20 | -- | -- |
| **L** | 0.35 | 0.45 | 0.40 |
| **All Dimensions in mm** | | | |

## Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

**W-QFN4040-24 (Type A1)**




| Dimensions | Value (in mm) |
|---|---|
| **C** | 0.500 |
| **X** | 0.300 |
| **X1** | 0.750 |
| **X2** | 2.700 |
| **X3** | 3.850 |
| **Y** | 0.750 |
| **Y1** | 0.300 |
| **Y2** | 2.700 |
| **Y3** | 3.850 |

## Mechanical Data

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – Matte Tin-Plated Leads, Solderable per J-STD-202 e3
- Weight: 0.041 grams (Approximate)

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