2.3V TO 5.5V INPUT, 4A AUTOMOTIVE-COMPLIANT SYNCHRONOUS BUCK CONVERTER WITH I2C

Description

The AP61406Q is a selectable up to 4A, synchronous buck converter with an input voltage range of 2.3V to 5.5V and fully integrates a 75mΩ high-side power MOSFET and a 33mΩ low-side power MOSFET to provide high-efficiency step-down DC/DC conversion.

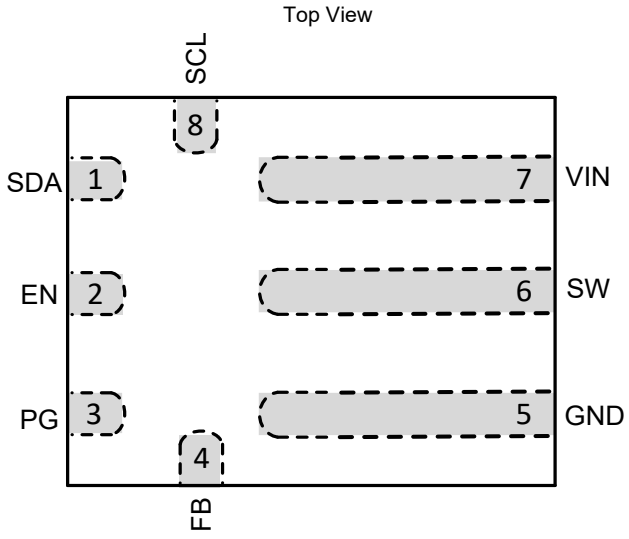
The AP61406Q is easily used by minimizing the external component count due to its adoption of constant on-time (COT) control to achieve fast transient responses, ease loop stabilization, and low output voltage ripple.

The AP61406Q has optimized designs for small form factor. The series offers various fixed output voltage and an adjustable output voltage version. It also has a proprietary gate driver scheme to resist switching node ringing without sacrificing MOSFET turn-on and turn-off times, which reduces high-frequency radiated EMI noise caused by MOSFET switching.

The AP61406Q features I2C compatible, 2-wires serial interface consisting of a bi-directional serial-data line, SDA, and a serial-clock line, SCL. It supports SCL clock rates up to 3.4MHz.

The device is available in a W-QFN1520-8/SWP (Type UX) package.

Pin Assignments



W-QFN1520-8/SWP (Type UX)

Features

- AEC-Q100 Qualified with the Following Results
  - Device Temperature Grade 1: -40°C to +125°C T_A
  - Device HBM ESD Classification Level H1C
  - Device CDM ESD Classification Level C3B
- Functional Safety-Capable – Documentation Available to Aid Functional Safety System Design
- Wettable Flange
- VIN 2.3V to 5.5V
- Wide Output Voltage Range: 0.300V to 3.600V
- 0.5V ± 2% Reference Voltage (Default Setting)
- 20μA Ultra-Low Quiescent Current (Pulse-Frequency Modulation)
- I2C Interface up to 3.4MHz SCL Clock Rates
  - Programmable Mode – PFM/PWM
  - Programmable Frequency – 1MHz, 1.5MHz, 2MHz, 2.5MHz
  - Programmable IOUT – 1A/2A/3A/4A
  - 20mV Increment VOUT Adjust
- Power-Good Indicator
- Protection Circuitry
  - Undervoltage Lockout (UVLO)
  - VIN Overvoltage Protection (OVP)
  - Peak and Valley Current Limit
  - Thermal Shutdown
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **The AP61406Q is suitable for automotive applications requiring specific change control; this part is AEC-Q100 qualified, PPAP capable, and manufactured in IATF 16949 certified facilities.**
  https://www.diodes.com/quality/product-definitions/

Applications

- Automotive power systems
- Automotive infotainment
- Automotive instrument clusters
- Automotive telematics
- Advanced driver assistance systems

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Typical Applications Circuit

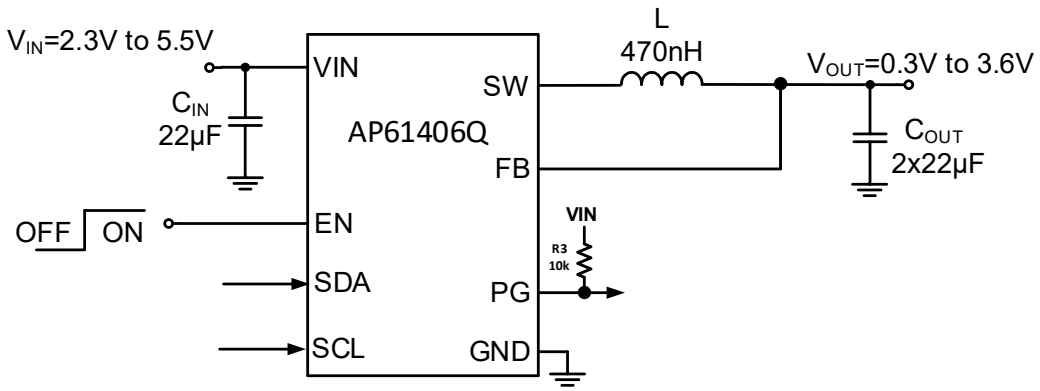


Figure 1. Typical Application Circuit

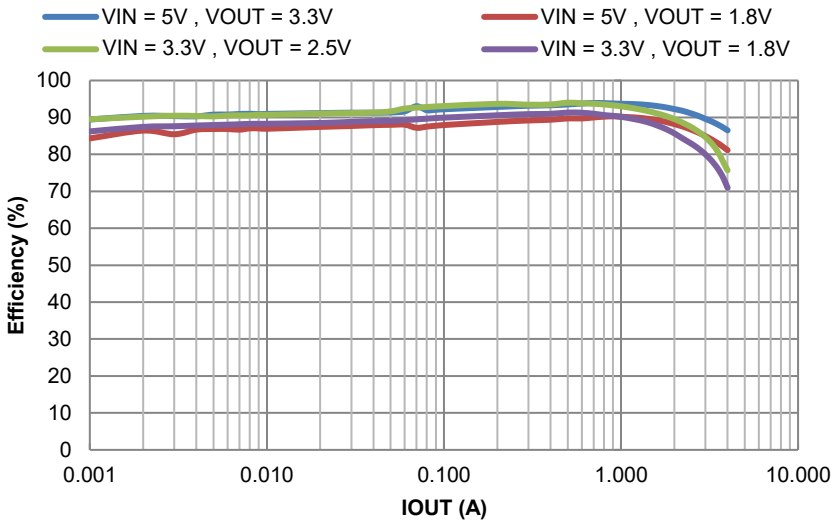


Figure 2. PFM Efficiency vs. Output Current, L = 0.47µH

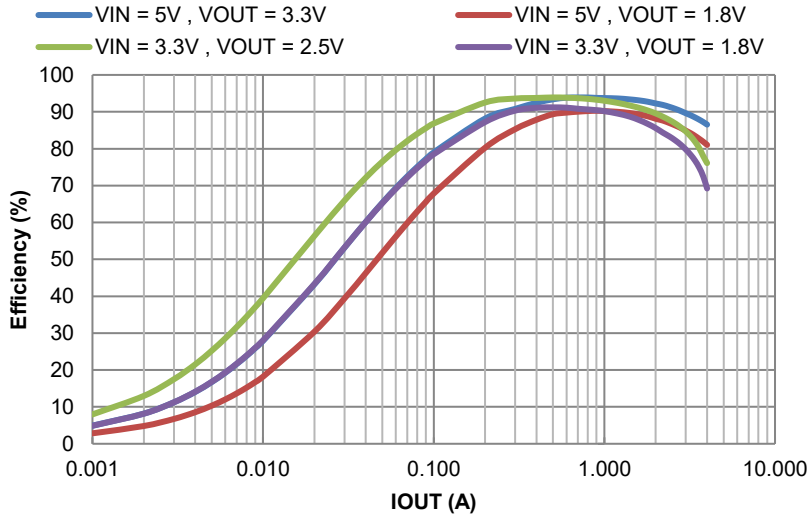


Figure 3. FPWM Efficiency vs. Output Current, L = 0.47µH

Pin Descriptions

Pin Number	Pin Name	Function
1	SDA	I2C Data I/O.
2	EN	Enable Input. EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator and low to turn it off. EN is used to program the Modulation Mode (PFM or PWM). See *Enable* section for more details.
3	PG	Power-Good Pin. Open-drain power-good output that is pulled to GND when the output voltage is out of its regulation limits or during soft-start. There is an internal 5MΩ pullup resistor.
4	FB	Feedback Sensing Terminal for the Output Voltage.
5	GND	Power Ground.
6	SW	Power Switching Output. SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load.
7	VIN	Power Input. VIN supplies the power to the IC, as well as the step-down converter switches. Drive VIN with a 2.3V to 5.5V power source. Bypass VIN to GND with a suitably large capacitor to eliminate noise due to the switching of the IC. See *Input Capacitor* section for more details.
8	SCL	I2C Clock Input.

Functional Block Diagram

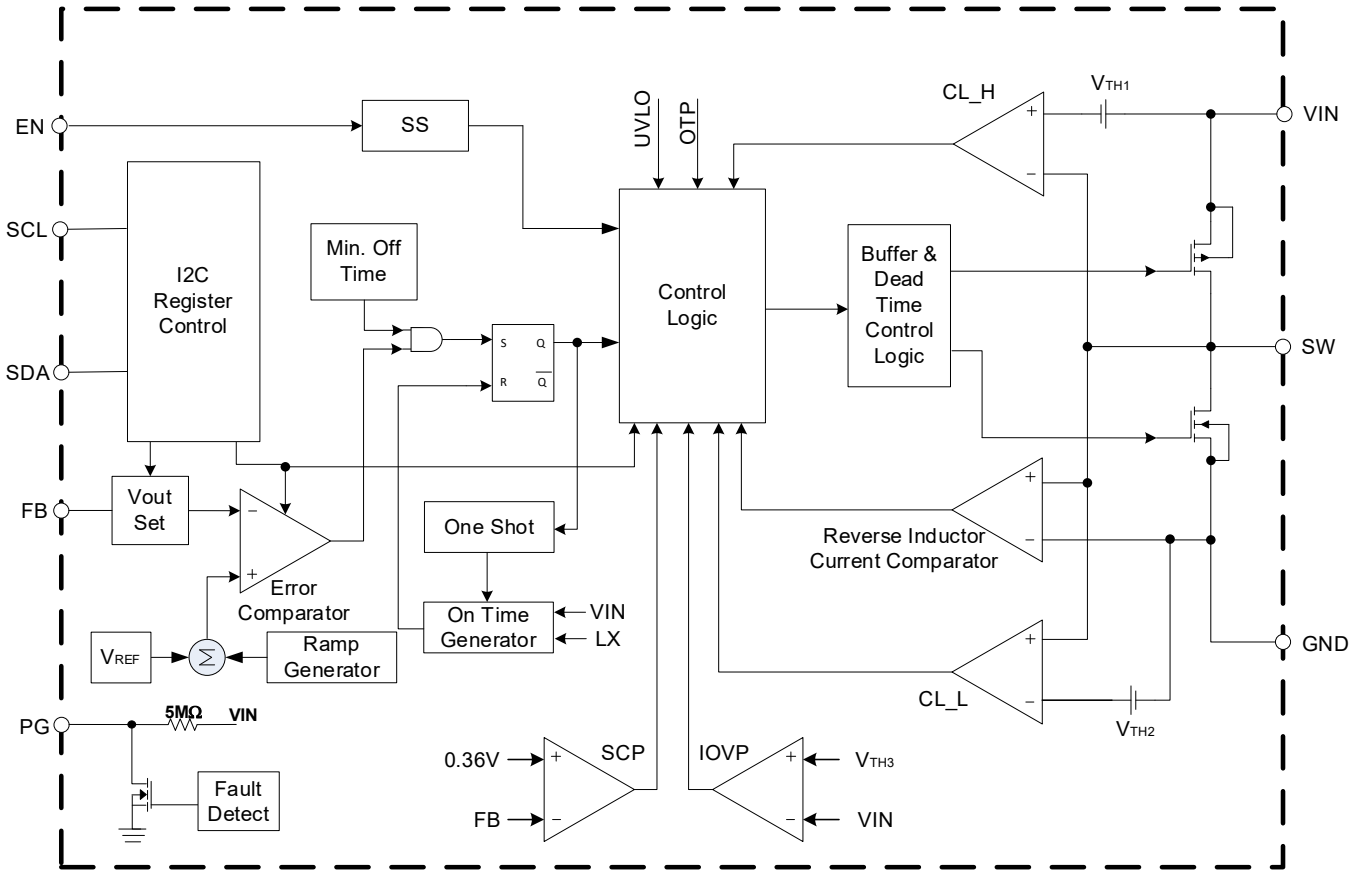


Figure 4. AP61406Q Functional Block Diagram

Absolute Maximum Ratings (@T_A = +25°C, unless otherwise specified.) (Note 4)

Parameter	Rating	Unit
Supply Voltage	-0.3 to +6.0 (DC)	V
	-0.3 to 6.5 (400ms)	
Switch Node Voltage	-1.0 to VIN + 0.3 (DC)	V
	-0.3 to VIN + 2.0 (20ns)	
Feedback Voltage	-0.3 to VIN + 0.3	V
All Other Pins	-0.3 to VIN + 0.3	V
Storage Temperature	-65 to +150	°C
Junction Temperature	+160	°C
ESD Susceptibility (Note 5)		
Human Body Model	±2000	V
Charged Device Model	±1000	V

Notes: 4. Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to *Absolute Maximum Ratings* for extended periods can affect device reliability.
5. Semiconductor devices are ESD sensitive and may be damaged by exposure to ESD events. Suitable ESD precautions should be taken when handling and transporting these devices.

Package Thermal Information

Symbol	Parameter	Rating, JEDEC (Note 6)	AP61406Q EVM (Note 7)	Unit
θ_{JA}	Junction to Ambient	91	71	°C/W
$\theta_{JC(TOP)}$	Junction to Case (Top)	58	N/A	°C/W
θ_{JB}	Junction to Board (Bottom)	9.8	N/A	°C/W
ψ_{JT}	Junction to Top Characterization Parameter	2.6	2.6	°C/W
ψ_{JB}	Junction to Board Characterization Parameter	9.4	9	°C/W
$\theta_{JC(BOT)}$	Junction to Case (Bottom)	9.6	9	°C/W

Notes: 6. Device mounted on FR-4 substrate, JEDEC 4-layer 50mm x 50mm PCB board (2oz copper), with minimum recommended pad layout.
7. Device mounted on Diodes Incorporated's evaluation board. See user guide for more details.

Recommended Operating Conditions (@T_A = +25°C, unless otherwise specified.) (Note 8)

Symbol	Parameter	Min	Max	Unit
V_{IN}	Supply Voltage	2.3	5.5	V
I_{OUT}	Output Current	—	4	A
T_J	Operating Junction Temperature Range	-40	+150	°C

Note: 8. The device function is not guaranteed outside of the recommended operating conditions.

Electrical Characteristics (T_A = +25°C, VIN = 5V, unless otherwise specified. Min/Max limits apply across the recommended junction temperature range, -40°C to +150°C, and input voltage range, 2.3V to 5.5V.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{SHDN}	Shutdown Supply Current	V_{EN} = 0	—	0.02	—	μA
I_Q	Supply Current (Quiescent)	V_{FB} = 0.65V	—	20	—	μA
UVLO	V_{IN} Undervoltage Threshold (Rising)	—	—	2.15	2.3	V
	V_{IN} Undervoltage Threshold Hysteresis	—	—	150	—	mV
$R_{DS(ON)1}$	High-Side Switch On-Resistance (Note 9)	I_{SW} = 100mA High Side	—	75	—	mΩ
$R_{DS(ON)2}$	Low-Side Switch On-Resistance (Note 9)	I_{SW} = 100mA Low Side	—	33	—	mΩ
R_{DISCH}	Output Discharge Switch On Resistor	—	—	100	—	Ω
I_{PEAK_LIMIT}	HS Peak Current Limit (Note 9)	—	5.0	6.5	8.5	A
I_{VALLEY_LIMIT}	LS Valley Current Limit (Note 9)	—	4.7	5.7	8.0	A
f_{SW}	Switching Frequency	—	—	2	—	MHz
t_{OFF_MIN}	Minimum Off-Time	—	—	110	—	ns
PG Detection	UVP PG Threshold Reference to FB	UVP FB Rising Edge	—	95	—	%
	UVP Hysteresis	UVP FB Falling Edge	—	10	—	
PG Pullup	PG Pullup resistor	—	—	5	—	MΩ
PG Low	PG Low Voltage	Rp = 10kΩ	—	—	0.4	V
PG Delay	PG Delay	—	—	40	—	μs
V_{FB}	Feedback Voltage	Default Setting	490	500	510	mV
V_{EN_H}	EN Logic High	—	—	—	1.2	V
V_{EN_L}	EN Logic Low	—	0.6	—	—	V
I_{EN}	EN Input Current	VIN = V_{EN} = 5V	—	2	—	μA
t_{SS}	Soft-Start Period	—	0.3	0.5	0.7	ms
T_{SD}	Thermal Shutdown (Note 9)	—	—	+160	—	°C
T_{HYS}	Thermal Hysteresis (Note 9)	—	—	+30	—	°C
V_{IOVP}	VIN Overvoltage Protection (Note 9)	—	—	6.3	—	V
V_{IHYS}	VIN Overvoltage Protection Hysteresis (Note 9)	—	—	0.3	—	V
I2C Electrical Characteristics						
SCL, SDA	SCL, SDA Input High Voltage Threshold	—	0.7 x VCC	—	—	V
	SCL, SDA Input Low Voltage Threshold	—	—	—	0.3 x VCC	V
	Hysteresis	—	—	0.05 x VCC	—	V
	Input Current	—	-10	—	10	μA
	Input Capacitance	—	—	10	—	pF
SDA	Output Low Voltage	I_{SINK} = 20mA	—	—	0.4	V
t_{OF}	Output Fall Time from VCC to 0.3 x VCC	—	—	—	120	ns

Note: 9. Compliance with the datasheet limits is assured by one or more methods: production test, characterization, and/or design.

Electrical Characteristics (T_A = +25°C, VIN = 5V, unless otherwise specified. Min/Max limits apply across the recommended junction temperature range, -40°C to +150°C, and input voltage range, 2.3V to 5.5V.) (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I2C – Compatible Interface Timing (Standard, Fast, and Fast Mode Plus) (Note 9)						
f_{SCL}	Clock Frequency	—	—	—	1	MHz
$t_{SU;STA}$	Setup Time (Repeated) Start Condition	SCL rising edge to SDA falling edge; Both crossing High threshold	0.26	—	—	µs
$t_{HD;STA}$	Hold Time (Repeated) Start Condition	From SDA falling edge crossing Low threshold to SCL falling edge crossing High threshold	0.26	—	—	µs
t_{LOW}	SCL Low Period	Time measured during the Low voltage threshold	0.5	—	—	µs
t_{HIGH}	SCL High Period	Time measured during the High voltage threshold	0.26	—	—	µs
$t_{HD;DAT}$	Input Data Hold Time	From SCL falling edge crossing Low threshold to SDA entering the Low-High window	0	—	—	µs
$t_{SU;DAT}$	Input Data Setup Time	From SDA exiting the Low-High window to SCL rising edge crossing Low threshold	50	—	—	ns
$t_{SU;STO}$	Setup Time for Stop Condition	From SCL rising edge crossing High threshold to SDA rising edge crossing Low threshold	0.26	—	—	µs
t_{BUF}	Bus-Free Time Between Stop and Start	From SDA crossing High threshold during STOP condition to SDA crossing High threshold for the following START condition	0.5	—	—	µs
t_{SP}	Maximum Pulse Width of Spike That Must be Suppressed by the Input Filter	Any pulse width narrower than the maximum specification is suppressed	—	50	—	ns
C_B	Capacitive Load for Each Bus Line	Total on-chip and off-chip capacitance	—	—	550	pF

Note: 9. Compliance with the datasheet limits is assured by one or more methods: production test, characterization, and/or design.

Electrical Characteristics (T_A = +25°C, VIN = 5V, unless otherwise specified. Min/Max limits apply across the recommended junction temperature range, -40°C to +150°C, and input voltage range, 2.3V to 5.5V.) (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I2C – Compatible Interface Timing (High-Speed Mode, C_B = 100pF) (Note 9)						
f_{SCL}	Clock Frequency	—	—	—	3.4	MHz
$t_{SU;STA}$	Setup Time (Repeated) Start Condition	SCL rising edge to SDA falling edge; Both crossing High threshold	160	—	—	ns
$t_{HD;STA}$	Hold Time (Repeated) Start Condition	From SDA falling edge crossing Low threshold to SCL falling edge crossing High threshold	160	—	—	ns
t_{LOW}	SCL Low Period	Time measured during the Low voltage threshold	160	—	—	ns
t_{HIGH}	SCL High Period	Time measured during the High voltage threshold	60	—	—	ns
$t_{HD;DAT}$	Input Data Hold Time	From SCL falling edge crossing Low threshold to SDA entering the Low-High window	—	35	—	ns
$t_{SU;DAT}$	Input Data Setup Time	From SDA exiting the Low-High window to SCL rising edge crossing Low threshold	10	—	—	ns
$t_{SU;STO}$	Setup Time for Stop Condition	From SCL rising edge crossing High threshold to SDA rising edge crossing Low threshold	160	—	—	ns
t_{RCL}	SCL Rise Time	—	10	—	40	ns
t_{RCL1}	Rise time of SCL signal after REPEATED START condition and after Acknowledge bit	—	10	—	80	ns
t_{FCL}	SCL Fall Time	—	10	—	40	ns
t_{RDA}	SDA Rise Time	—	—	—	80	ns
t_{FDA}	SDA Fall Time	—	—	—	80	ns
t_{BUF}	Bus-Free Time Between Stop and Start	From SDA crossing High threshold during STOP condition to SDA crossing High threshold for the following START condition	—	10	—	ns
t_{SP}	Maximum Pulse Width of Spike That Must be Suppressed by the Input Filter	Any pulse width narrower than the maximum specification is suppressed	—	10	—	ns
C_B	Capacitive Load for Each Bus Line	Total on-chip and off-chip capacitance	—	—	100	pF

Note: 9. Compliance with the datasheet limits is assured by one or more methods: production test, characterization, and/or design.

Typical Performance Characteristics (AP61406Q at T_A = +25°C, VIN = 3.3V, VOUT = 1.8V, L = 0.47µH, PFM unless otherwise specified.)

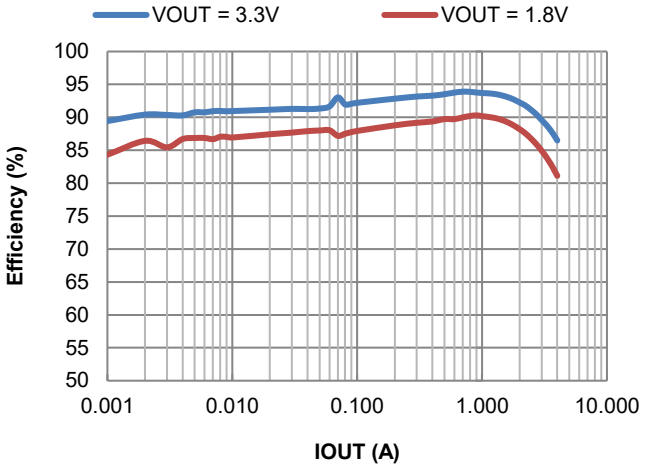


Figure 5. Efficiency vs. Output Current

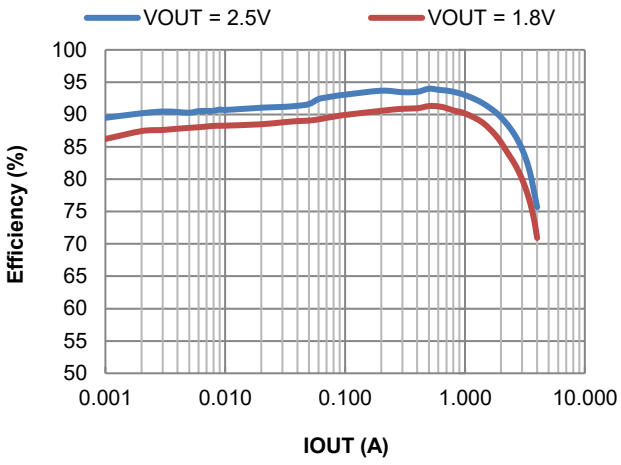


Figure 6. Efficiency vs. Output Current

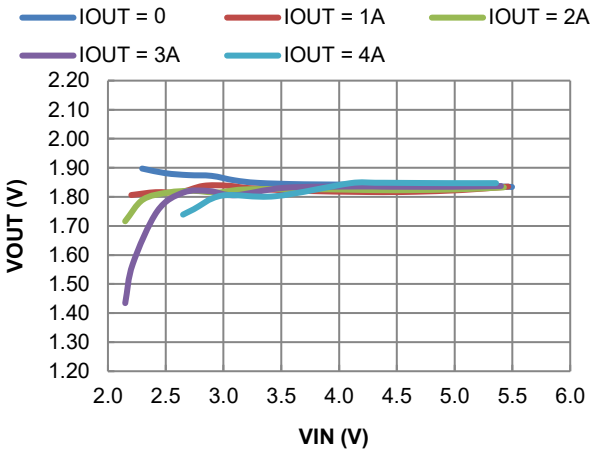


Figure 7. Line Regulation

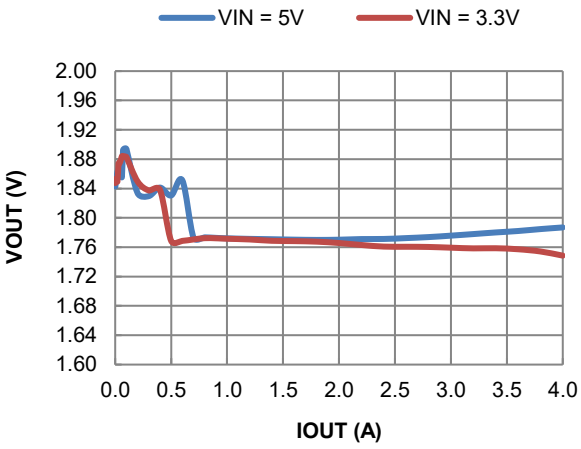


Figure 8. Load Regulation

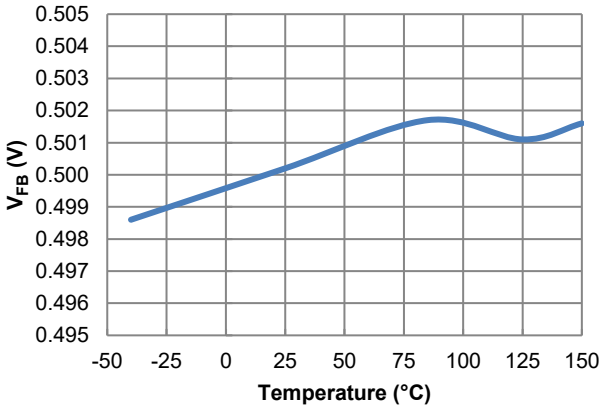


Figure 9. Feedback Voltage vs. Temperature

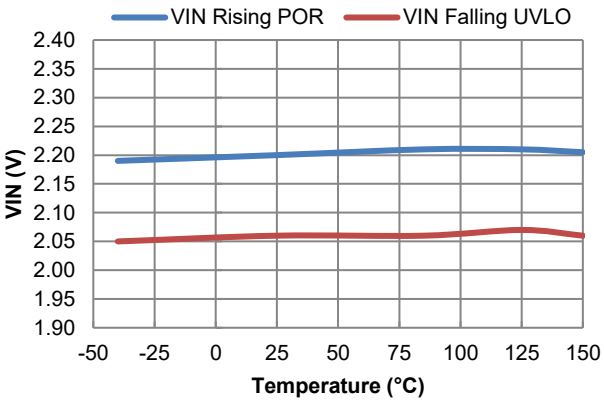


Figure 10. VIN Power-On Reset and UVLO vs. Temperature

Typical Performance Characteristics (AP61406Q at T_A = +25°C, VIN = 3.3V, VOUT = 1.8V, L = 0.47µH, PFM unless otherwise specified.) (continued)

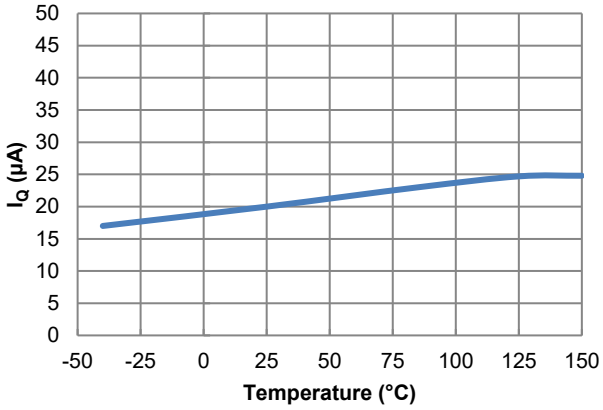


Figure 11. I_Q vs. Temperature

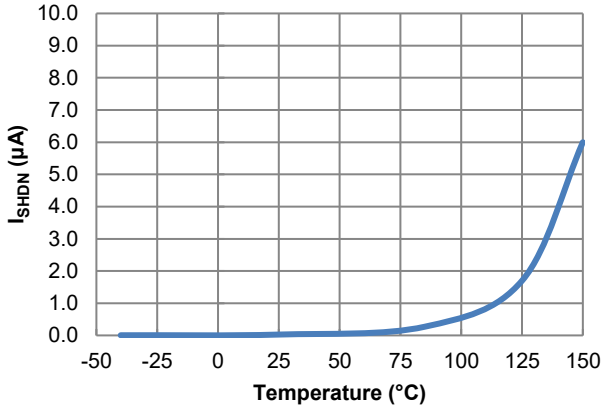


Figure 12. I_{SHDN} vs. Temperature

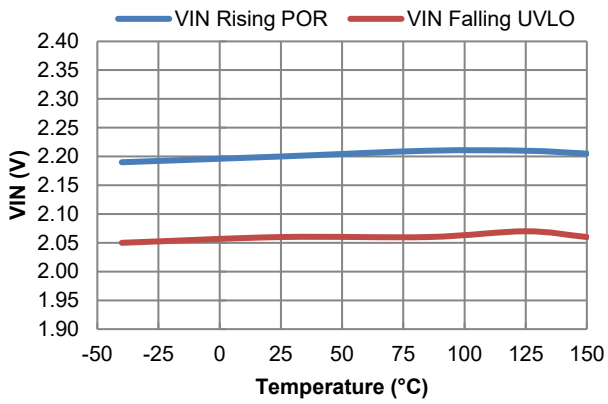


Figure 13. VIN Power-On Reset and UVLO vs. Temperature

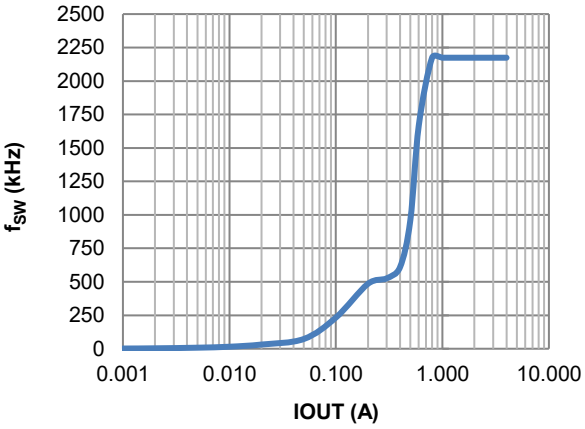


Figure 14. f_{SW} vs. Load

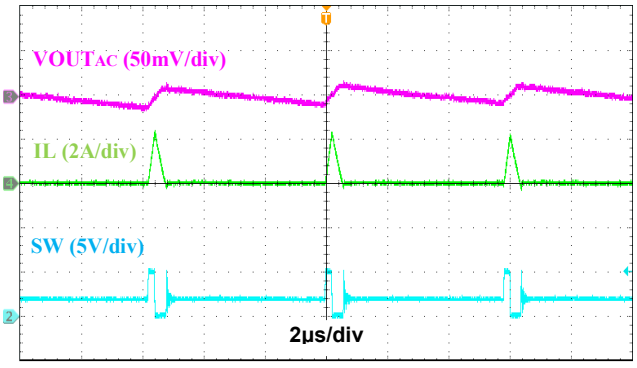


Figure 15. Output Voltage Ripple, IOUT = 100mA

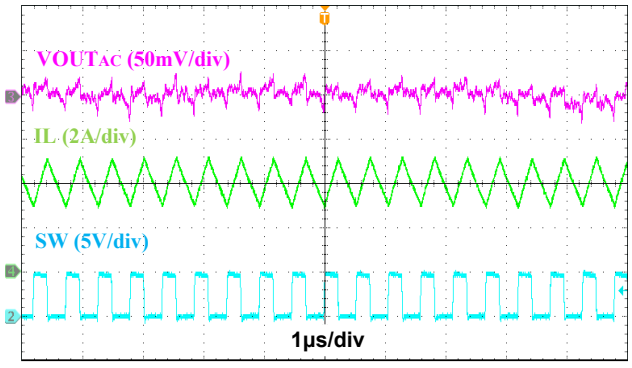


Figure 16. Output Voltage Ripple, IOUT = 4A

Typical Performance Characteristics (AP61406Q at T_A = +25°C, VIN = 3.3V, VOUT = 1.8V, L = 0.47µH, PFM unless otherwise specified.) (continued)

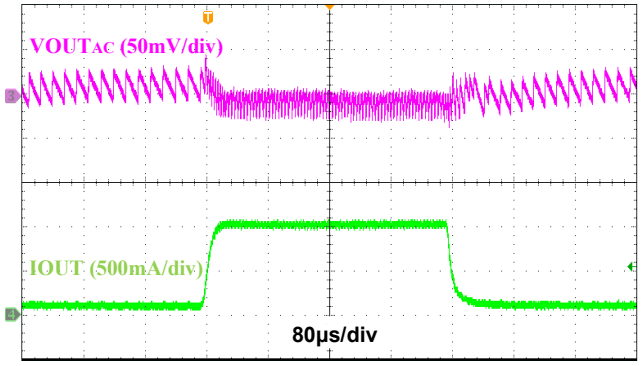


Figure 17. Load Transient, IOUT = 50mA to 1A to 50mA

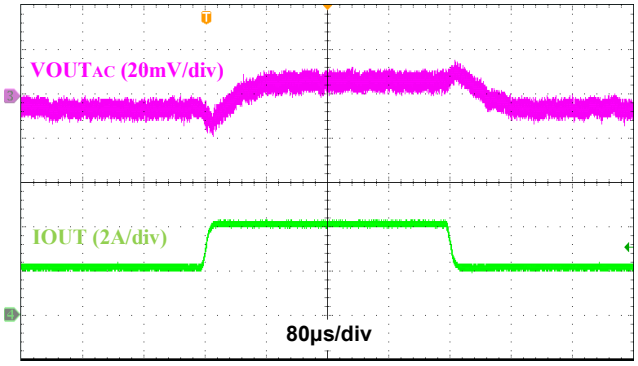


Figure 18. Load Transient, IOUT = 2A to 4A to 2A

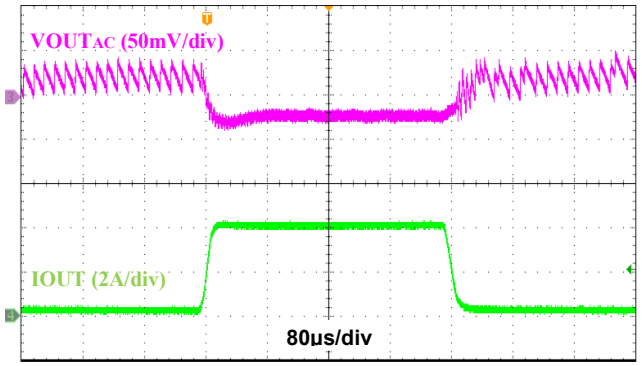


Figure 19. Load Transient, IOUT = 50mA to 4A to 50mA

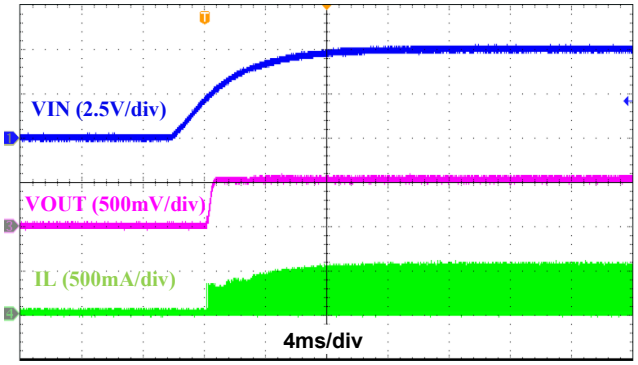


Figure 20. Startup Using VIN, IOUT = 0.1A

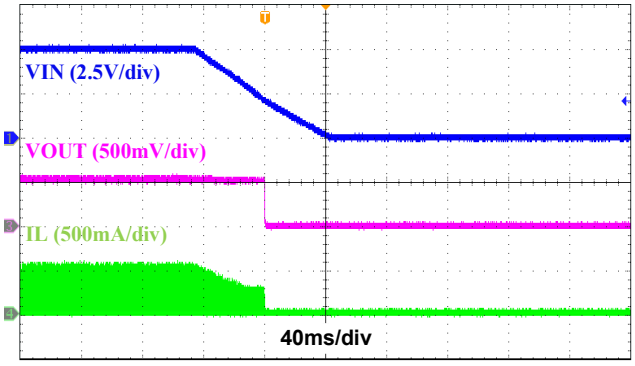


Figure 21. Shutdown Using EN, IOUT = 0.1A

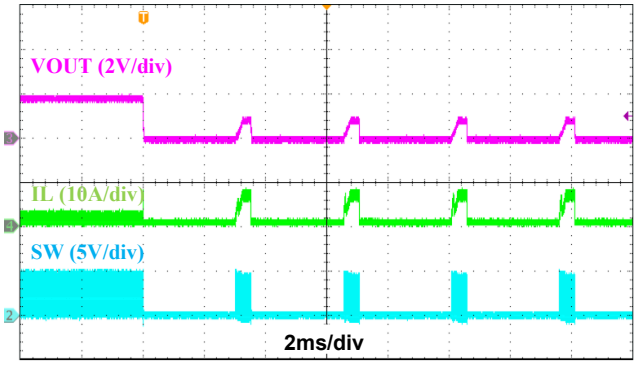


Figure 22. Output Short Protection, IOUT = 0.05A

Typical Performance Characteristics (AP61406Q at T_A = +25°C, VIN = 3.3V, VOUT = 1.8V, L = 0.47µH, PFM unless otherwise specified.) (continued)

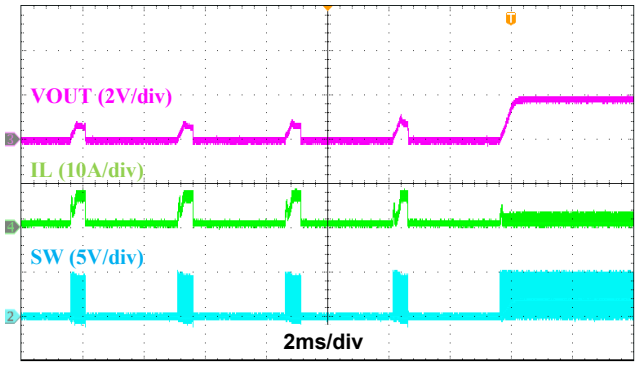


Figure 23. Output Short Recovery, IOUT = 0.05A

Typical Performance Characteristics (AP61406Q at T_A = +25°C, VIN = 3.3V, VOUT = 1.8V, L = 0.47µH, PWM unless otherwise specified.) (continued)

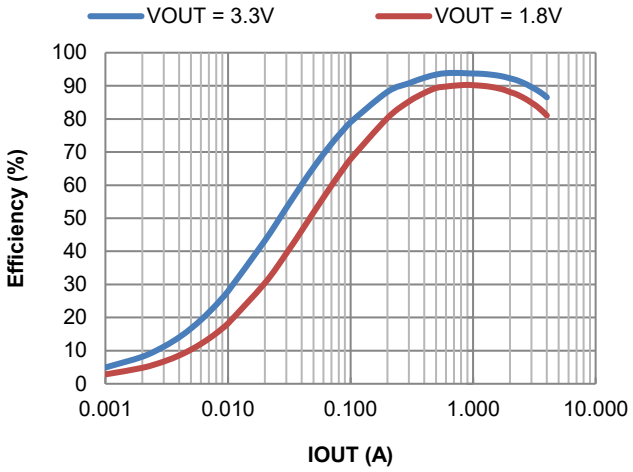


Figure 24. Efficiency vs. Output Current

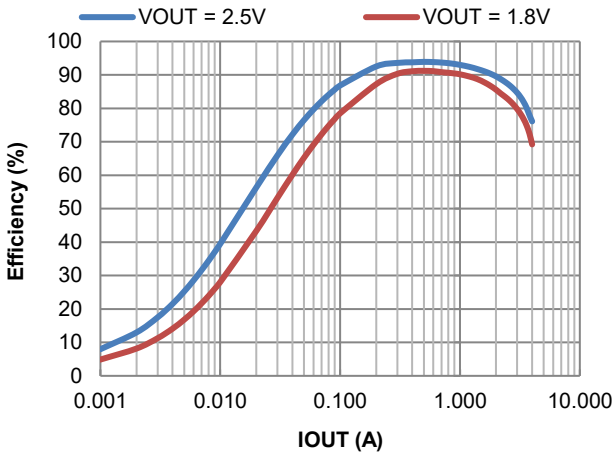


Figure 25. Efficiency vs. Output Current

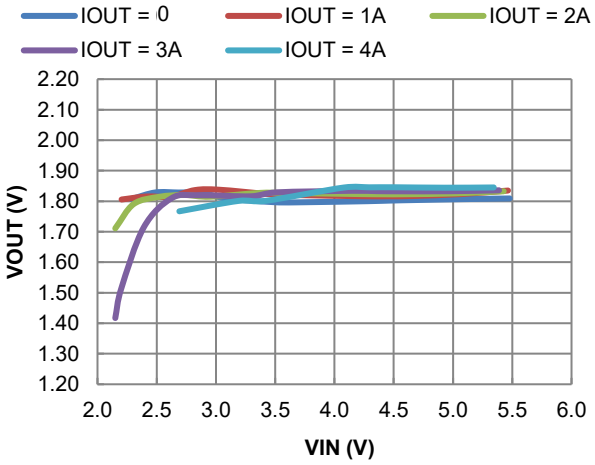


Figure 26. Line Regulation

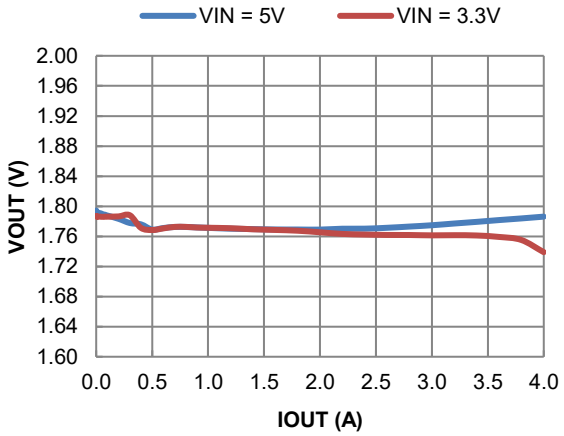


Figure 27. Load Regulation

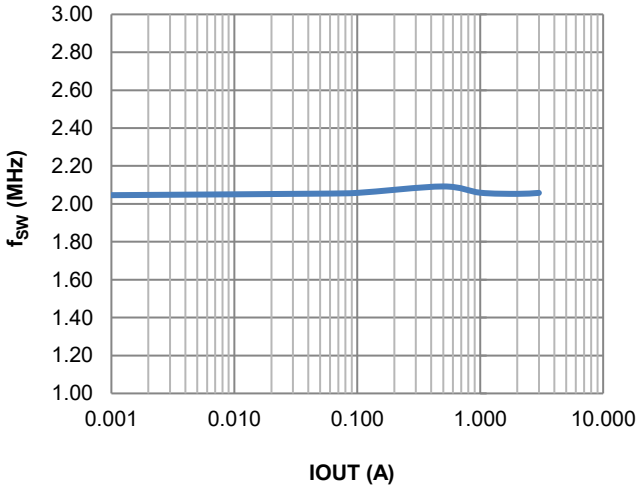


Figure 28. f_{SW} vs. Load

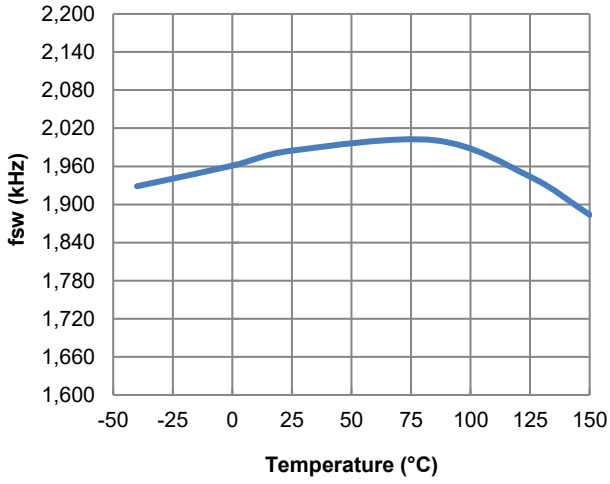


Figure 29. f_{SW} vs. Temperature

Typical Performance Characteristics (AP61406Q at T_A = +25°C, VIN = 3.3V, VOUT = 1.8V, L = 0.47µH, FPWM unless otherwise specified.) (continued)

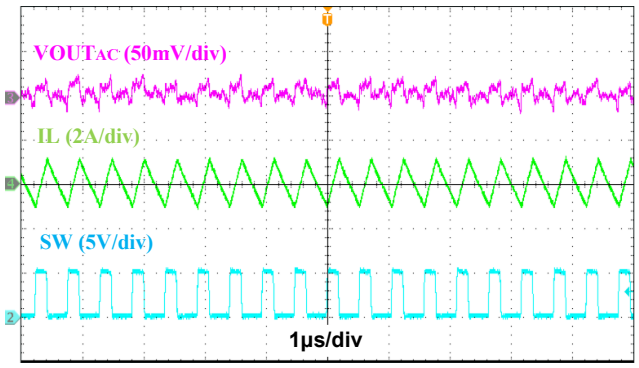


Figure 30. Output Short Recovery, IOUT = 0.05A

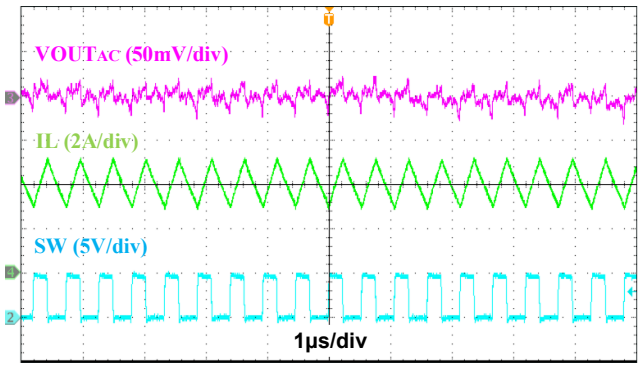


Figure 31. Output Short Recovery, IOUT = 4A

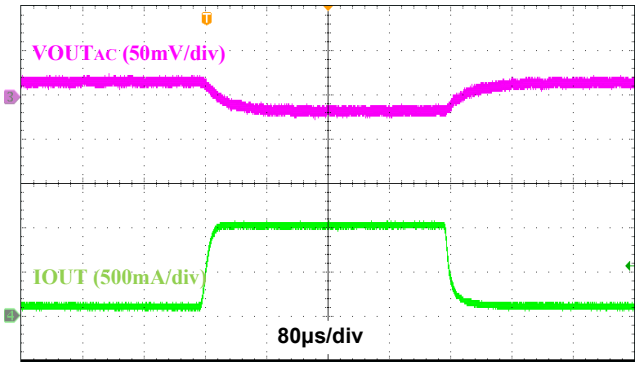


Figure 32. Load Transient, IOUT = 50mA to 1A to 50mA

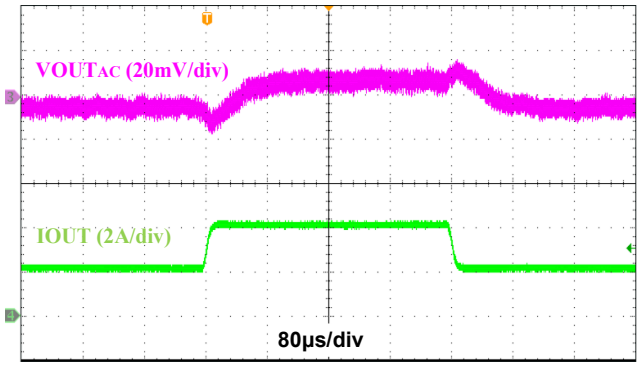


Figure 33. Load Transient, IOUT = 2A to 4A to 2A

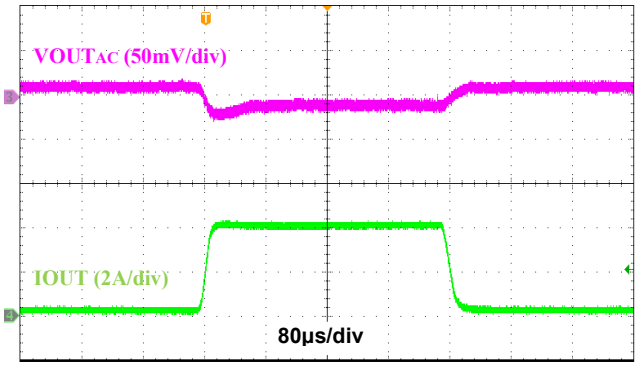


Figure 34. Load Transient, IOUT = 50mA to 4A to 50mA

Application Information

Constant-On-Time Control

The Constant-On-Time control architecture allows for fast transient response and requires no loop compensation, which reduces external component count and reduces design complexity.

The COT control relies on a fixed switch on-time to regulate the output. The on-time of the high-side switch can be estimated as:

$$t_{ON} = 500ns*(V_{OUT}/V_{IN}) \quad \text{(Default Frequency)} \qquad \textbf{Eq. 1}$$

The AP61406Q has a fixed minimum off-time of 110ns, which can prevent the inductor current runaway during load transient.

Undervoltage Lockout (UVLO) Circuit

When the V_{IN} drops lower than the UVLO detector threshold (2V typ), the UVLO circuit starts to operate, V_{REF} stops, and with the high-side and low-side switch turned "OFF". As a result, V_{OUT} drops according to the COUT capacitance value and the load. When the V_{IN} rises higher than UVLO released voltage (2.15V typ), the IC will restart the operation.

Current Limit Protection

The AP61406Q typically has a 6A high-side switch current limit. When the current flows into high side switch reaches the current limit threshold, the AP61406Q will enter cycle by cycle current limit mode until the current drops. Also, a cycle-by-cycle valley current detect circuit is implemented for current limit. The switch current is monitored during the low-side switch on state, if the monitored current is above the current threshold, the converter maintains low-side switch on until the current level becomes threshold level or lower.

Short-Circuit Protection and Recovery

When the AP61406Q output node is shorted to GND that V_{FB} drops under 0.36V, it will enter hiccup mode to lower power loss. If a short circuit is removed, and V_{FB} rises over 0.36V, the AP61406Q recovers to normal operation again.

Overtemperature Protection

The internal thermal temperature protection circuitry is provided to protect the integrated circuit if the maximum junction temperature is exceeded. When the junction temperature exceeds +160°C, it shuts down the internal control circuit and switches. The AP61406Q will restart automatically under the control of soft-start circuit when the junction temperature decreases to +130°C.

Enable

When disabled, the device shutdown supply current is only 0.1μA. When applying a voltage greater than the EN logic-high threshold (typical 0.91V, rising), the AP61406Q enables all functions, and the device initiates the soft-start phase. The AP61406Q has a built-in 0.5ms soft-start time to prevent output voltage overshoot and inrush current. When the EN voltage falls below its logic-low threshold (typical 0.83V, falling), the internal SS voltage discharges to ground and device operation is disabled.

Input Capacitor

The input capacitor reduces both the surge current drawn from the input supply as well as the switching noise from the device. The input capacitor must sustain the ripple current produced during the on-time of Q1. It must have a low ESR to minimize power dissipation due to the RMS input current.

The RMS current rating of the input capacitor is a critical parameter and must be higher than the RMS input current. As a rule of thumb, select an input capacitor with an RMS current rating greater than half of the maximum load current.

Due to large di/dt through the input capacitor, electrolytic or ceramic capacitors with low ESR should be used. If using a tantalum capacitor, it must be protected, or failure could occur. Using a ceramic capacitor of 22μF or greater is sufficient for most applications.

Output Capacitor

The output capacitor keeps the output voltage ripple small, ensures feedback loop stability, and reduces both the overshoots and undershoots of the output voltage during load transients. During the first few microseconds of an increasing load transient, the converter recognizes the change from steady state and sets the off-time to minimum to supply more current to the load. However, the inductor limits the change in increasing current depending on its inductance. Therefore, the output capacitor supplies the difference in current to the load during this time. Likewise, during the first few microseconds of a decreasing load transient, the converter recognizes the change from steady state and increases the off-time to reduce the current supplied to the load. However, the inductor limits the change in decreasing current as well. Therefore, the output capacitor absorbs the excess current from the inductor during this time.

Application Information (continued)

The effective output capacitance, COUT, requirements can be calculated from the equations below.

The ESR of the output capacitor dominates the output voltage ripple. The amount of ripples can be calculated by:

$$\mathbf{VOUT_{Ripple}} = \Delta \mathbf{I_L} \cdot \left(\mathbf{ESR} + \frac{\mathbf{1}}{\mathbf{8} \cdot \mathbf{f_{sw}} \cdot \mathbf{COUT}} \right) \quad \textbf{Eq. 2}$$

An output capacitor with large capacitance and low ESR is the best option. For most applications, a 10μF to 22μF ceramic capacitor is sufficient. To meet the load transient requirements, the calculated COUT should satisfy the following inequality:

$$\mathbf{COUT} > \mathbf{max}\left(\frac{\mathbf{L} \cdot \mathbf{I_{Trans}^2}}{\Delta \mathbf{V_{Overshoot}} \cdot \mathbf{VOUT}}, \frac{\mathbf{L} \cdot \mathbf{I_{Trans}^2}}{\Delta \mathbf{V_{Undershoot}} \cdot (\mathbf{VIN} - \mathbf{VOUT})} \right) \quad \textbf{Eq. 3}$$

Where:

- I_{Trans} is the load transient.
- $\Delta V_{Overshoot}$ is the maximum output overshoot voltage.
- $\Delta V_{Undershoot}$ is the maximum output undershoot voltage.

Serial Interface

The I2C compatible 2-wire serial interface is used for regulator on/off control, setting output voltages, and other functions. See the *Register Map* section for details. The I2C interface is an open-drain serial bus that consists of a bi-directional serial data line (SDA) and a serial clock line (SCL). Pullup resistors of 500Ω each or greater must be added from VIN to SDA and VIN to SCL. Optional 24Ω resistors in series with SDA and SCL help to protect the device inputs from high voltage spikes on the bus lines. Series resistors also minimize crosstalk and undershoot on bus lines.

System Configuration

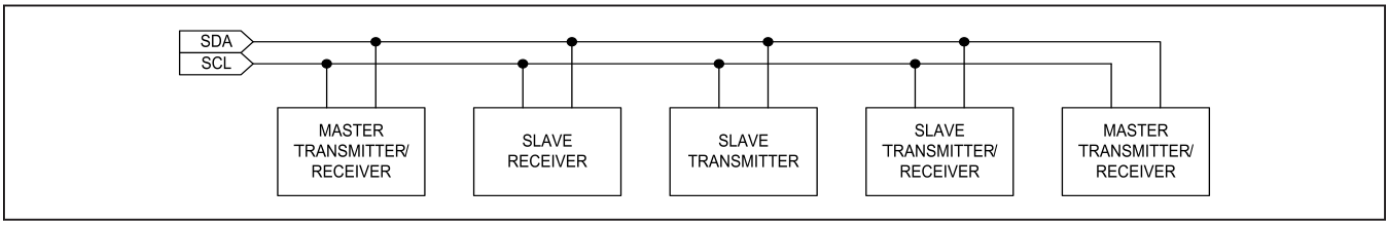


Figure 35. Functional Logic Diagram for Communications Controller

The I2C bus is a multi-master bus. The maximum number of devices that can attach to the bus is limited by bus capacitance. The figure above shows an example of a typical I2C system. A device on the I2C bus that sends data to the bus is called a transmitter. A device that receives data from the bus is called a receiver. The device that initiates a data transfer and generates the SCL clock signal to control the data transfer is the master. Any device on the bus that can be addressed by the master is considered a slave. When the AP61406Q I2C compatible interface is operating, it is a slave on I2C bus.

Bit Transfer

One data bit is transferred for each SCL clock cycle. The data on SDA must remain stable during the high portion of SCL clock pulse. Changes in SDA while SCL are high are control signals (START and STOP conditions).

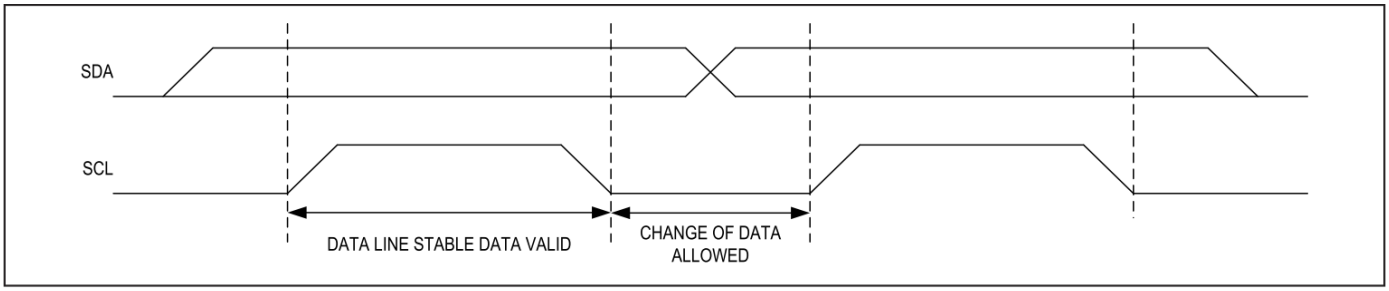


Figure 36. I2C Bit Transfer

Application Information (continued)

START and STOP Conditions

When the I2C serial interface is inactive, SDA and SCL are pulled high. A master device initiates communication by issuing a START (S) condition. A START condition is a high-to-low transition on SDA while SCL is high. A STOP (P) condition is a low-to-high transition on SDA while SCL is high. A START condition from the master signals the AP61406Q that a transmission is about to begin. The master terminates transmission and frees the bus by issuing a STOP condition. To issue a series of commands to the slave, the master may issue REPEATED START (Sr) conditions instead of a STOP condition to maintain control of the bus. In general, a REPEATED START condition is functionally equivalent to a regular START condition. AP61406Q will listen to its address after a START condition is detected. If its address is not detected, it will stay idle until the next START condition is detected.

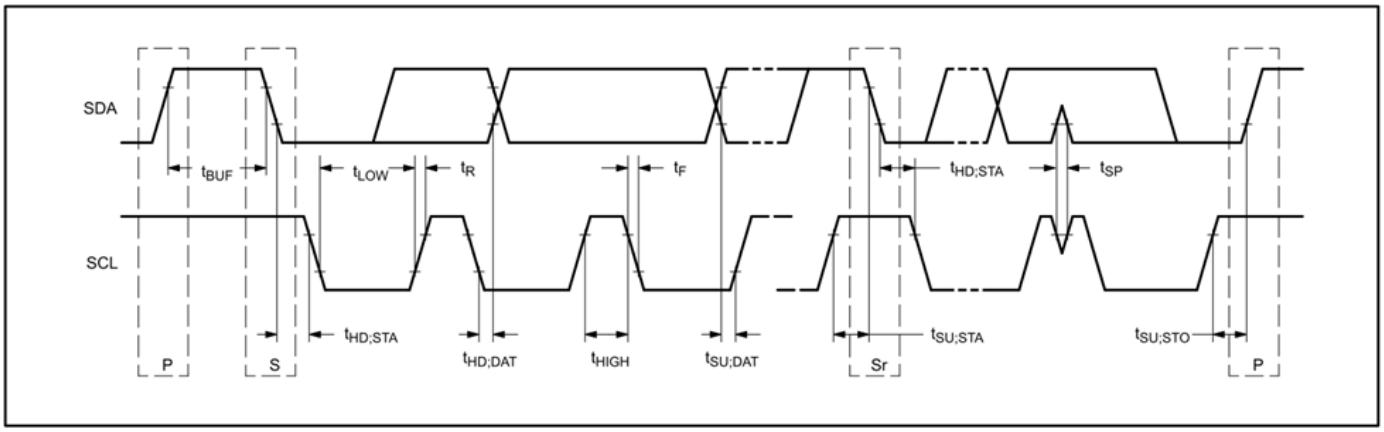


Figure 37. Start and Stop Conditions

Acknowledge

Both I2C bus master and AP61406Q (slave) generate ACKNOWLEDGE (ACK) bits when receiving data. The ACK bit is the last bit of each nine bit data packet. To generate an ACK bit, the receiving device must pull SDA low before the rising edge of the ACK-related clock pulse (ninth SCL pulse) and keep it low during the high period of the clock pulse. To generate a NOT ACKNOWLEDGE (nACK), the receiving device allows SDA to be pulled high before the rising edge of the ACK-related clock pulse and leaves it high during the high period of the clock pulse. Monitoring the ACK bits allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master should reattempt communication later.

Slave Address

The I2C slave address of AP61406Q is shown in table below:

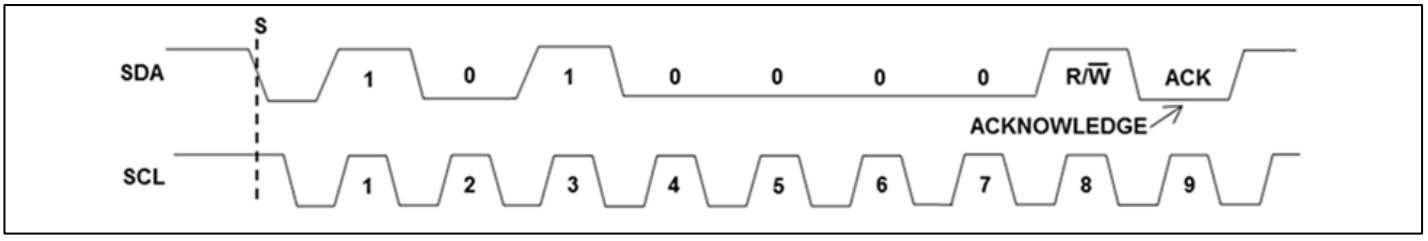


Figure 38. Slave Address Byte Example for AP61406Q

Clock Stretching

In general, the clock signal generation for the I2C bus is the responsibility of the master device. I2C specification allows slow slave devices to alter the clock signal by holding down the clock line. The process in which a slave device holds down the clock line is typically called clock stretching. The AP61406Q does not use any form of clock stretching to hold down the clock line.

General Call Address

The AP61406Q does not implement the I2C specification called general call address. If the AP61406Q sees a general call address (00000000b), it does not issue an ACKNOWLEDGE.

Application Information (continued)

Communication Speed

The AP61406Q provides I2C 3.0-compatible serial interface.

- I2C revision 3-compatible serial communications channel
  - 0 to 100kHz (Standard-mode)
  - 0 to 400kHz (Fast-mode)
  - 0 to 1MHz (Fast-mode Plus)
  - 0 to 3.4MHz (High-Speed mode)
  - Does not utilize I2C clock stretching

Operating in Standard-mode, Fast-mode, or Fast-mode Plus does not require any special protocols. The main consideration when changing the bus speed through this range is the combination of the bus capacitance and pullup resistors. Higher time constants created by the bus capacitance and pullup resistance (C x R) slow the bus operation. Therefore, when increasing bus speeds, the pullup resistance must be decreased to maintain a reasonable time constant. Refer to the Pullup Resistor Sizing section of I2C revision 3.0 specification for detailed guidance on the pullup resistor selection. In general, for bus capacitances of 200pF, a 100kHz bus needs pullup resistor of 5.6kΩ, a 400kHz bus needs about a 1.5kΩ pullup resistors, and a 1MHz bus needs 680Ω pullup resistors. Note that the pullup resistor is dissipating power when the open-drain bus is low. Lower values of the pullup resistors result in higher power dissipation (V^2/R).

Operating in High-Speed (HS) mode requires some special considerations. For the full list of considerations, refer to the I2C 3.0 specification. The major considerations with respect to AP61406Q are:

- The I2C bus master uses current source pullups to shorten the signal rise times.
- The I2C slave must use a different set of input filters on its SDA and SCL lines to accommodate for the higher bus speed.
- The communication protocols need to utilize the High-Speed master code.

At power-up or after each STOP condition, the AP61406Q inputs filters are set for Standard-mode, Fast-mode, or Fast-mode Plus (i.e. 0 to 1MHz). Use the High-Speed master code protocols that are described in *Communication Protocols* section to switch the input filters for High-Speed mode.

Communication Protocols

The AP61406Q supports both writing and reading from its registers. The following sections show the I2C communication protocols.

Application Information (continued)

Writing to a Single Register

Figure 39 below shows the protocol for I2C master device to write one byte of data to the AP61406Q the write byte protocol is as follows:

1. The master sends a START condition.
2. The master sends the 7-bit slave address followed by a write bit (R/nW = 0).
3. The addressed slave sends an ACK bit by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a data byte.
7. The slave acknowledges the data byte.
8. The next falling edge of SCL loads the data byte into its target register and the data becomes active.
9. The master sends a STOP condition or a REPEATED START condition.

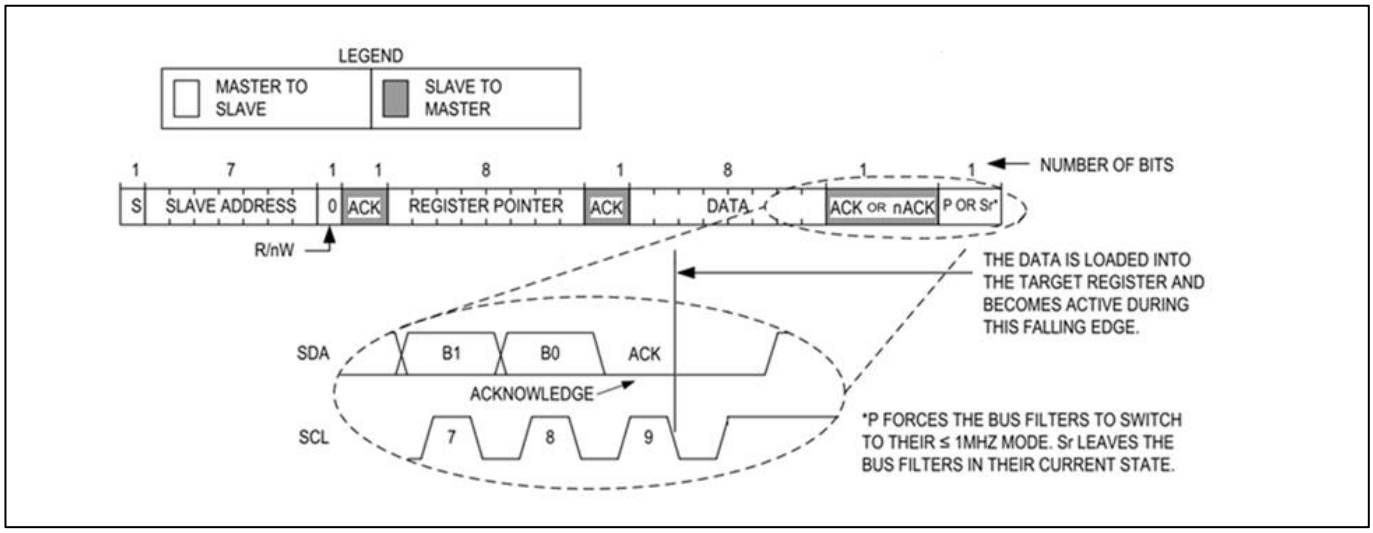


Figure 39. Writing to a Single Register with Write Byte Protocol

Application Information (continued)

Writing to a Sequential Register

Figure 40 below shows the protocol for writing to sequential registers. This protocol is similar to the write byte protocol, except the master continues to write additional data after it receives an ACK from the slave that it successfully received the previous data byte. The slave's register pointer will auto-increment by one after each byte received. When the master is done writing, it issues a STOP or REPEATED START. The writing to sequential registers protocol is as follows:

1. The master sends a START condition.
2. The master sends the 7-bit slave address followed by a write bit (R/nW = 0).
3. The addressed slave sends an ACK bit by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a data byte.
7. The slave acknowledges the data byte.
8. The next falling edge on SCL loads the data byte into its target register and the data becomes active.
9. Steps 6 to 8 are repeated as many times as the master requires.
10. The master sends a STOP condition or a REPEATED START condition.

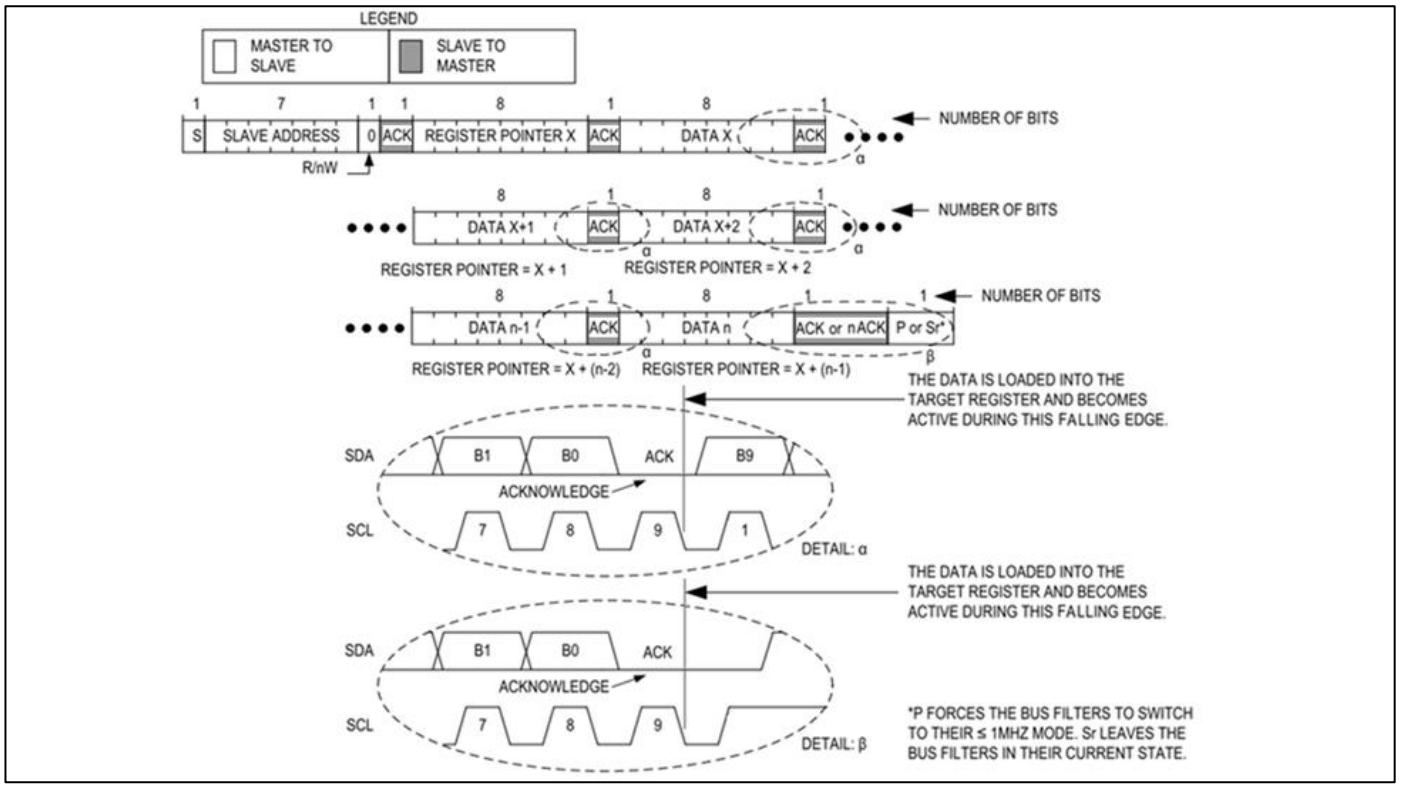


Figure 40. Writing to Sequential Registers X to N

Application Information (continued)

Reading from a Single Register

The I2C master device reads one byte of data from AP61406Q. The read byte protocol is as follows:

1. The master sends a START condition.
2. The master sends the 7-bit slave address followed by a write bit (R/nW = 0).
3. The addressed slave sends an ACK bit by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a REPEATED START condition.
7. The master sends the 7-bit slave address followed by a read bit (R/nW = 1).
8. The addressed slave sends an ACK bit by pulling SDA low.
9. The addressed slave places 8 bits of data on the bus from the register specified by the register pointer.
10. The master issues a nACK.
11. The master sends a STOP condition or a REPEATED START condition.

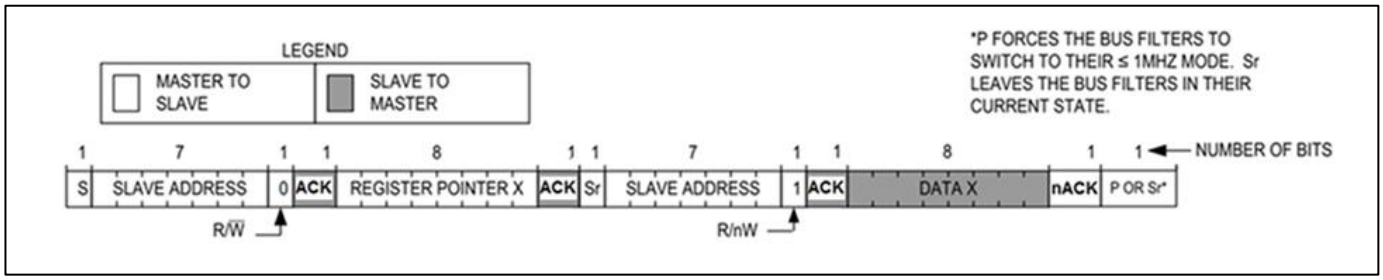


Figure 41. Reading from a Single Register X

Application Information (continued)

Reading from a Sequential Register

Figure 42 below shows the protocol for reading from sequential registers. This protocol is like the read byte protocol except the master issues an ACK to signal the slave that it wants more data. The slave's register pointer will auto-increment by one after each byte sent. When the master has all the data it requires, it issues a nACK and a STOP to end the transmission. The continuous read from sequential registers protocol is as follows:

1. The master sends a START condition.
2. The master sends the 7-bit slave address followed by a write bit (R/nW = 0).
3. The addressed slave sends an ACK bit pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a REPEATED START condition.
7. The master sends the 7-bit slave address followed by a read bit (R/nW = 1).
8. The addressed slave sends an ACK bit by pulling SDA low.
9. The addressed slave places 8-bits of data on the bus from the register specified by the register pointer.
10. The master issues an ACK signaling the slave that it wishes to receive more data.
11. Steps 9 to 10 are repeated as many times as the master requires.
12. Following the last byte of data, the master must issue a nACK to signal that it wishes to stop receiving data.
13. The master sends a STOP condition or a REPEATED START condition.

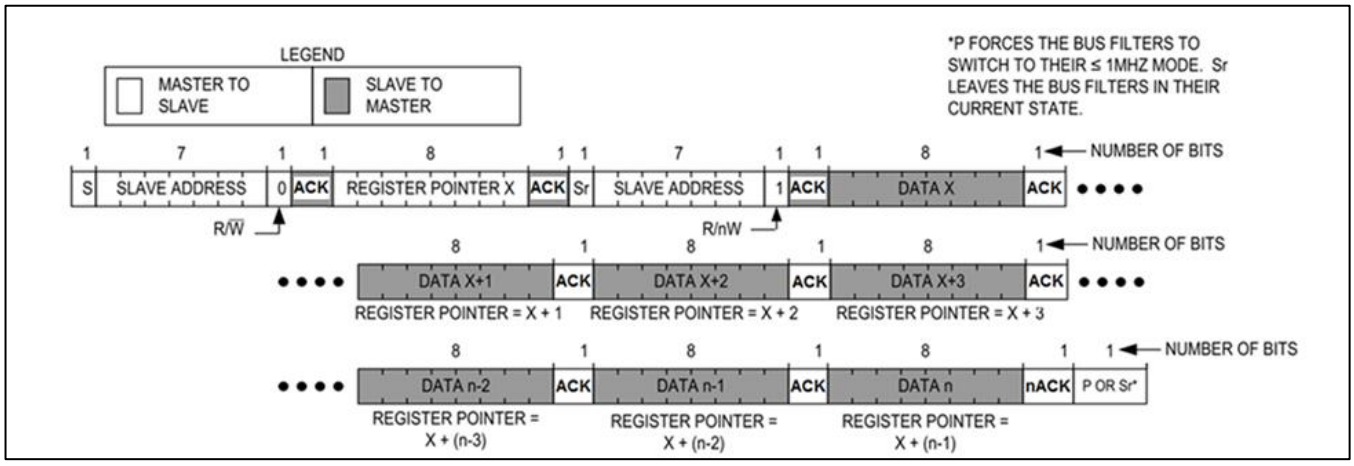


Figure 42. Reading Continuously from Sequential Registers X to N

Application Information (continued)

Engaging HS Mode for Operation up to 3.4MHz

Figure 43 below shows the protocol for engaging HS mode operation. HS mode operation allows for a bus operating speed of up to 3.4MHz. The protocol to engage HS mode is as follows:

1. Begin the protocol while operating at a bus speed of 1MHz or lower.
2. The master sends a START condition.
3. The master sends the 8-bit master code of 00001xxxb where xxxb are don't care bits.
4. The master code is not acknowledged.
5. The master switches to High-Speed communication and can now increase its bus speed up to 3.4MHz.
6. The master sends a REPEATED START condition.
7. The master issues any read/write operation in the known manner.

The master may continue to issue High-Speed read/write operations until a STOP is issued. Issuing a STOP ensures that the bus input filters are set for 1MHz or slower operation. Repeat steps 1 to 7 in the above algorithm to re-enter HS mode after a STOP has been issued.

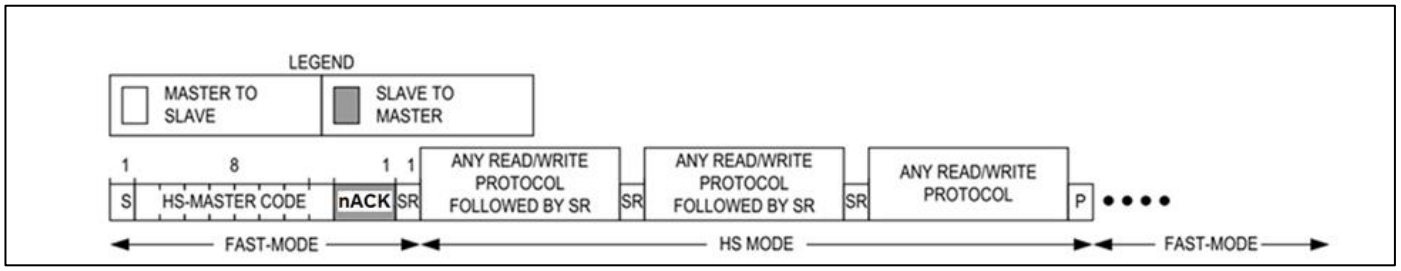


Figure 43. Engaging HS Mode

Application Information (continued)

Registers

Register reset conditions – Registers are reset when VIN = low, EN pin = low.

Register Map - I2C Slave Address (W/R): 50

ADDRESS	REGISTER NAME	RESET TYPE	R/W	BIT 7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	RESET VALUE
0x00	DEVICE_ID	TYPE_O	R	RESERVED	VERSION [3:0]				CHIP_REV [2:0]			-
0x01	STATUS	TYPE_O	R	RESERVED	RESERVED	RESERVED	RESERVED	TSHDN_S	VI_OVP_S	VO_OVP_S	OCP_S	-
0x02	CONFIG	TYPE_O	R/W	EN	AD	FS [1:0]		OCP [1:0]		RESERVED	PWM	0xEC
0x03	VOUT	TYPE_O	R/W	VOUT[7:0]								0x0A

Device ID Register

ADDRESS	ID		TYPE: O	RESET VALUE: N/A
0x00	R			
BIT	NAME	POR	DESCRIPTION	
7	RESERVE	0		
6:3	VERSION [3:0]	-	Version 0000b: A 0001b: B 0010b: C 0011b: D 0100b: E 0101b: F 0110b: G 0111b: H 1000b: I 1001b: J 1010b: K 1011b: L 1100b: M 1101b: N 1110b: O 1111b: P	
2:0	CHIP_REV [2:0]	-	Chip Revision History 000b: Pass1 001b: Pass2 010b: Pass3 011b: Pass4 100b: Pass5 101b: Pass6 110b: Pass7 111b: Pass8	

Application Information (continued)

Status Register

ADDRESS	STATUS		TYPE: O	RESET VALUE: N/A
0x01	R			
BIT	NAME	POR	DESCRIPTION	
7:4	RESERVE	-		
3	TSHDN_S	-	0: Junction Temperature ≤ 150°C 1: Junction Temperature ≥ 150°C	
2	VI_OVP_S	-	0: Input Voltage ≤ 6.5V 1: Input Voltage ≥ 6.5V	
1	VO OVP_S	-	0: Output Voltage ≤ 110% of VOUT set 1: Input Voltage ≥ 110% of VOUT set	
0	OCP_S	-	0: Not in OCP State 1: In OCP State	

Configuration Register

ADDRESS	CONFIG		TYPE: O	RESET VALUE: 0xEC
0x02	R/W			
BIT	NAME	POR	DESCRIPTION	
7	EN	1	Enable/Disable Control 0: Buck Disable 1: Buck Enable	
6	AD	1	Output Active Discharge 0: Disable Acive Discharge 1: Enable Active Discharge	
5:4	FS	10	Frequency Adjust 00b: 1MHz 01b: 1.5MHz 10b: 2MHz 11b: 2.5MHz	
3:2	OCP [1:0]	11	Output Current 00b: 1A 01b: 2A 10b: 3A 11b: 4A	
1	RESERVE	0		
0	PWM	0	PWM Enable 0: PFM 1: PWM	

Application Information (continued)

Output Voltage Setting Registers

ADDRESS	VOUT		TYPE: O	RESET VALUE: 0x0A
0x03	R/W			
BIT	NAME	POR	DESCRIPTION	
7	RESERVE	0		
7:0	VOUT [7:0]	0000 1010	0x00 = 0.300V	
			0x01 = 0.320V	
			0x02 = 0.340V	
			0x03 = 0.360V	
			0x04 = 0.380V	
			0x05 = 0.400V	
			0x06 = 0.420V	
			0x07 = 0.440V	
			0x08 = 0.460V	
			0x09 = 0.480V	
			0x0A = 0.500V	
			0x0B = 0.520V	
			0x0C = 0.540V	
			**	
			**	
			**	
			**	
			0xA0 = 3.500V	
			0xA1 = 3.520V	
			0xA2 = 3.5400V	
			0xA3 = 3.560V	
			0xA4 = 3.580V	
			0xA5 = 3.600V	

Note: 10. Address 0x03 must be written before VOUT change can initiate.

Application Information (continued)

PCB Layout

1. The AP61406Q device works at 4A current load, so heat dissipation is a major concern in the layout of the PCB. 2oz copper for both the top and bottom layers is recommended.
2. Provide sufficient vias for the input and output capacitors' GND side to dissipate heat to the bottom layer.
3. Make the bottom layer under the device as the GND layer for heat dissipation. The GND layer should be as large as possible to provide better effects.
4. Place the VIN capacitors as close to the device as possible.
5. Place the feedback components as close to FB as possible.
6. See Figure 44 for reference.

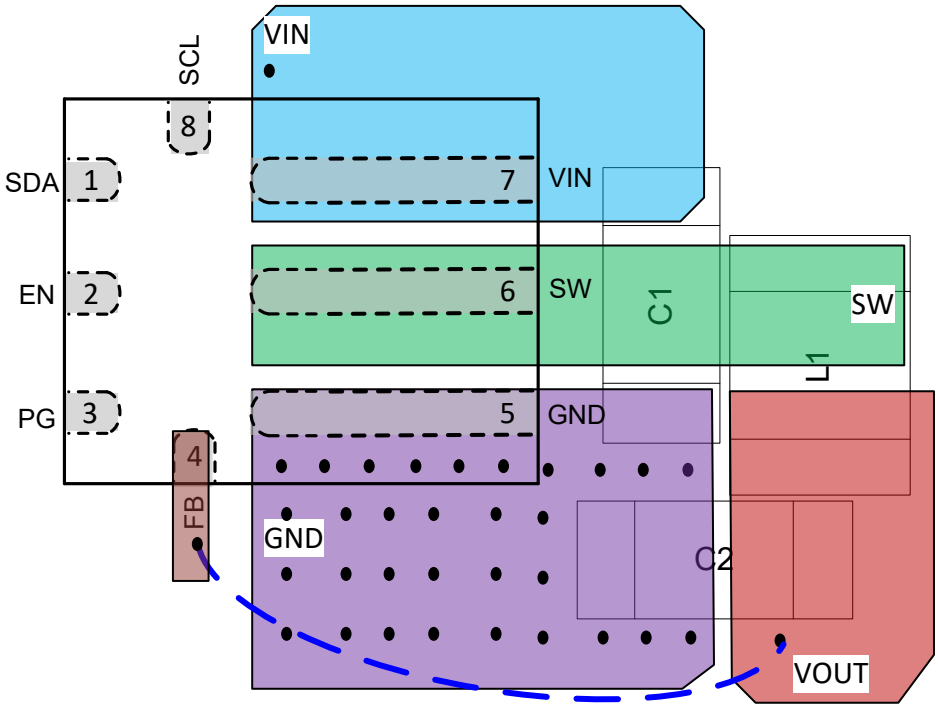
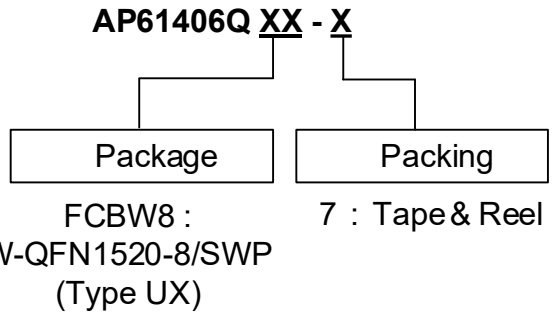


Figure 44. Recommended Layout

Ordering Information (Note 11)



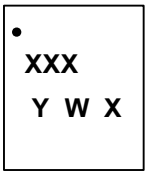
Orderable Part Number	Package	Package Code	Packing	
			Qty.	Carrier
AP61406QFCBW8-7	W-QFN1520-8/SWP (Type UX)	FCBW8	3000	Tape & Reel

Note: 11. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information

W-QFN1520-8/SWP (Type UX)

(Top View)



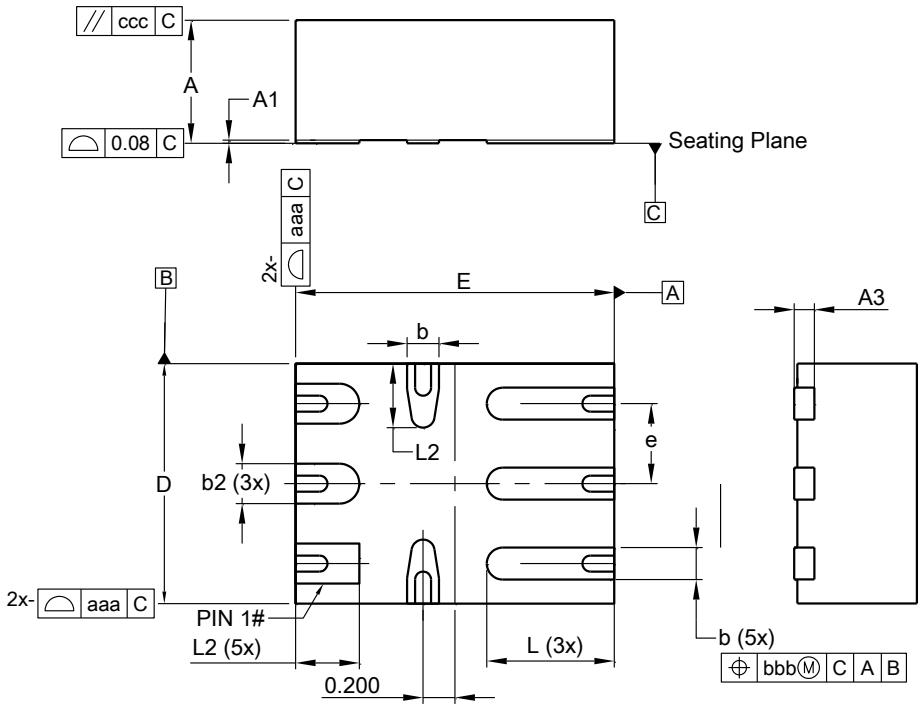
XXX : Identification Code
Y : Year 0 to 9 (ex: 5 = 2025)
W : Week: A to Z: week 1 to 26
a to z: week 27 to 52; z represents
week 52 and 53
X : Internal Code

Orderable Part Number	Package	Identification Code
AP61406QFCBW8-7	W-QFN1520-8/SWP (Type UX)	H3Q

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

W-QFN1520-8/SWP (Type UX)

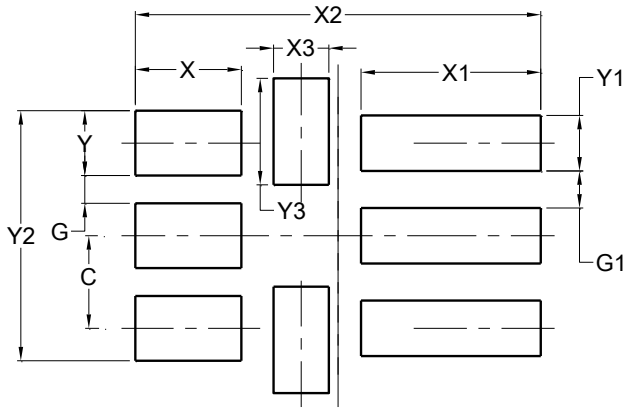


W-QFN1520-8/SWP (Type UX)			
Dim	**Min**	**Max**	**Typ**
A	0.70	0.80	0.75
A1	0.00	0.05	0.03
A3	--	--	0.127
b	0.150	0.250	0.200
b2	0.200	0.300	0.250
D	1.45	1.55	1.50
E	1.95	2.05	2.00
e	--	--	0.500
L	0.700	0.900	0.800
L2	0.300	0.500	0.400
aaa	0.15		
bbb	0.05		
ccc	0.05		
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

W-QFN1520-8/SWP (Type UX)



Dimensions	Value (in mm)
C	0.500
G	0.175
G1	0.275
X	0.575
X1	0.975
X2	1.700
X3	0.350
Y	0.350
Y1	0.300
Y2	1.350
Y3	0.575

Mechanical Data

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads, Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.008 grams (Approximate)

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