Description

The AP61402 is a selectable up to 4A, synchronous buck converter with an input voltage range of 2.3V to 5.5V and fully integrates a 75mΩ high-side power MOSFET and a 33mΩ low-side power MOSFET to provide high-efficiency step-down DC/DC conversion.

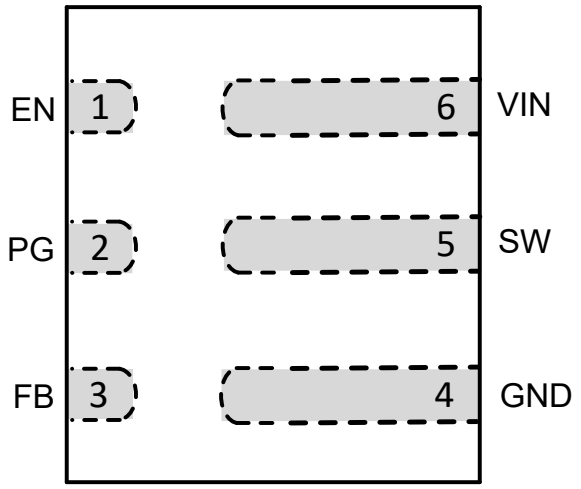
The AP61402 is easily used by minimizing the external component count due to its adoption of constant on-time (COT) control to achieve fast transient responses, easy loop stabilization, and low output voltage ripple.

The AP61402 has optimized designs for small form factor. The series offers various fixed output voltage and an adjustable output voltage version. It also has a proprietary gate driver scheme to resist switching node ringing without sacrificing MOSFET turn-on and turn-off times, which reduces high frequency radiated EMI noise caused by MOSFET switching.

The device is available in a V-DFN1515-6/SWP (Type UX) package.

Pin Assignments

Top View



V-DFN1515-6/SWP (Type UX)

Features

- VIN 2.3V to 5.5V
- Wide Output Voltage Range: 0.5V to 5.5V
- 4A Continuous Output Current
- 0.5V ±2% Reference Voltage
- 20μA Ultra-Low Quiescent Current (Pulse-Frequency Modulation)
- 2MHz Switching Frequency
- Programmable Modulation Mode Through EN
  - Pulse-Frequency Modulation
  - Pulse-Width Modulation Regardless of Output Load
- Proprietary Gate Driver Design for Best EMI Reduction
- ±5% Window Power-Good Indicator and OCP Selector
- Protection Circuitry
  - Undervoltage Lockout (UVLO)
  - VIN Overvoltage Protection (OVP)
  - Peak and Valley Current Limit
  - Thermal Shutdown
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **An automotive-compliant part is available under a separate datasheet (AP61402Q)**

Applications

- General-purpose POL supplies
- Network video cameras
- Wireless routers
- Hard disk drivers

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Typical Applications Circuit

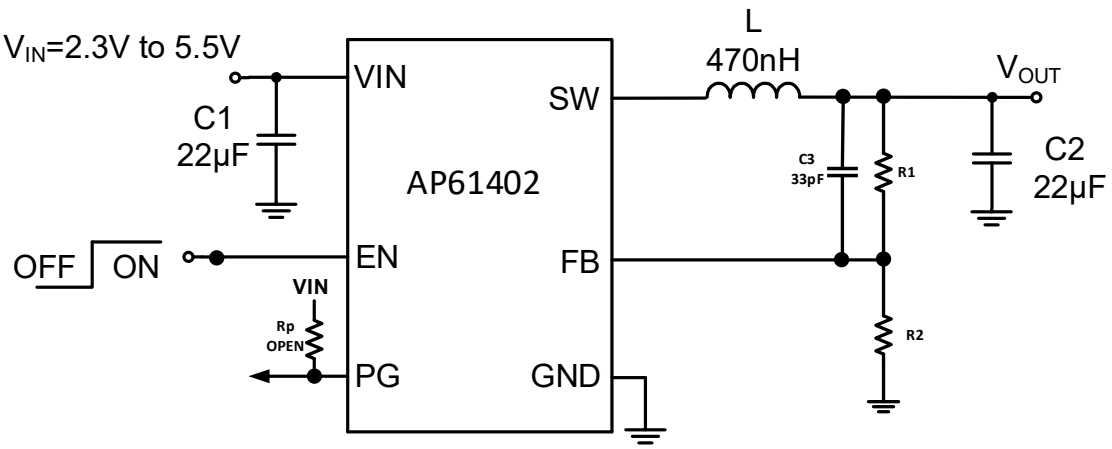


Figure 1. Typical Application Circuit

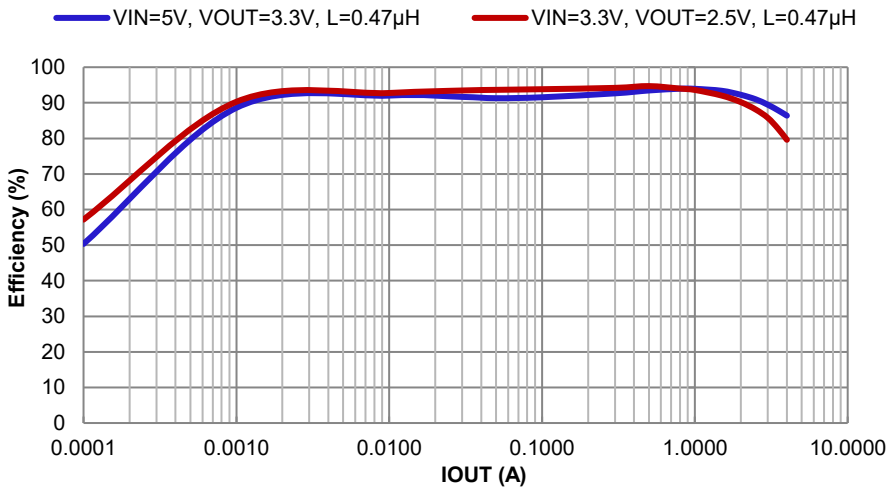


Figure 2. PFM Efficiency vs. Output Current

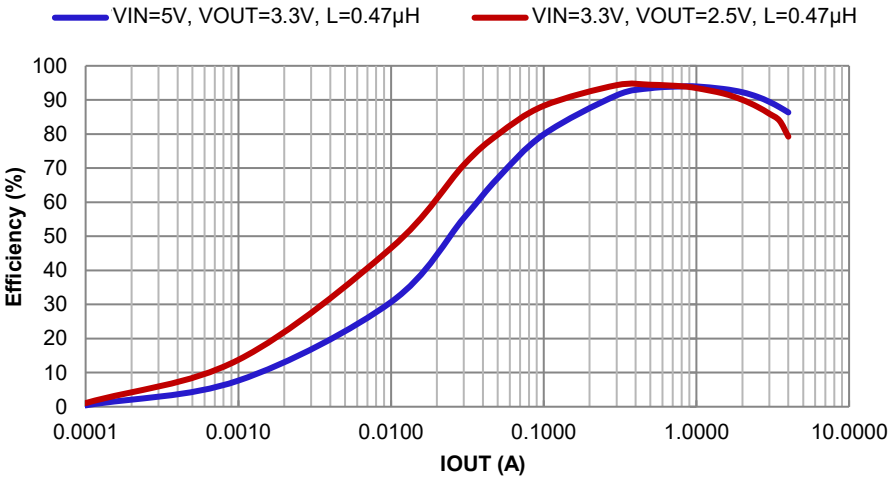


Figure 3. PWM Efficiency vs. Output Current

Pin Descriptions

Pin Number	Pin Name	Function
1	EN	Enable Input. EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator and low to turn it off. EN is used to program the Modulation Mode (PFM or PWM). See *Enable* section for more details.
2	PG	Power-Good Pin. Open-drain power-good output that is pulled to GND when the output voltage is out of its regulation limits or during soft-start. There is an internal 5MΩ pullup resistor.
3	FB	Feedback sensing terminal for the output voltage. Connect this pin to the resistive divider of the output. See *Setting the Output Voltage* section for more details.
4	GND	Power Ground.
5	SW	Power Switching Output. SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load.
6	VIN	Power Input. VIN supplies the power to the IC, as well as the step-down converter switches. Drive VIN with a 2.3V to 5.5V power source. Bypass VIN to GND with a suitably large capacitor to eliminate noise due to the switching of the IC. See *Input Capacitor* section for more details.

Functional Block Diagram

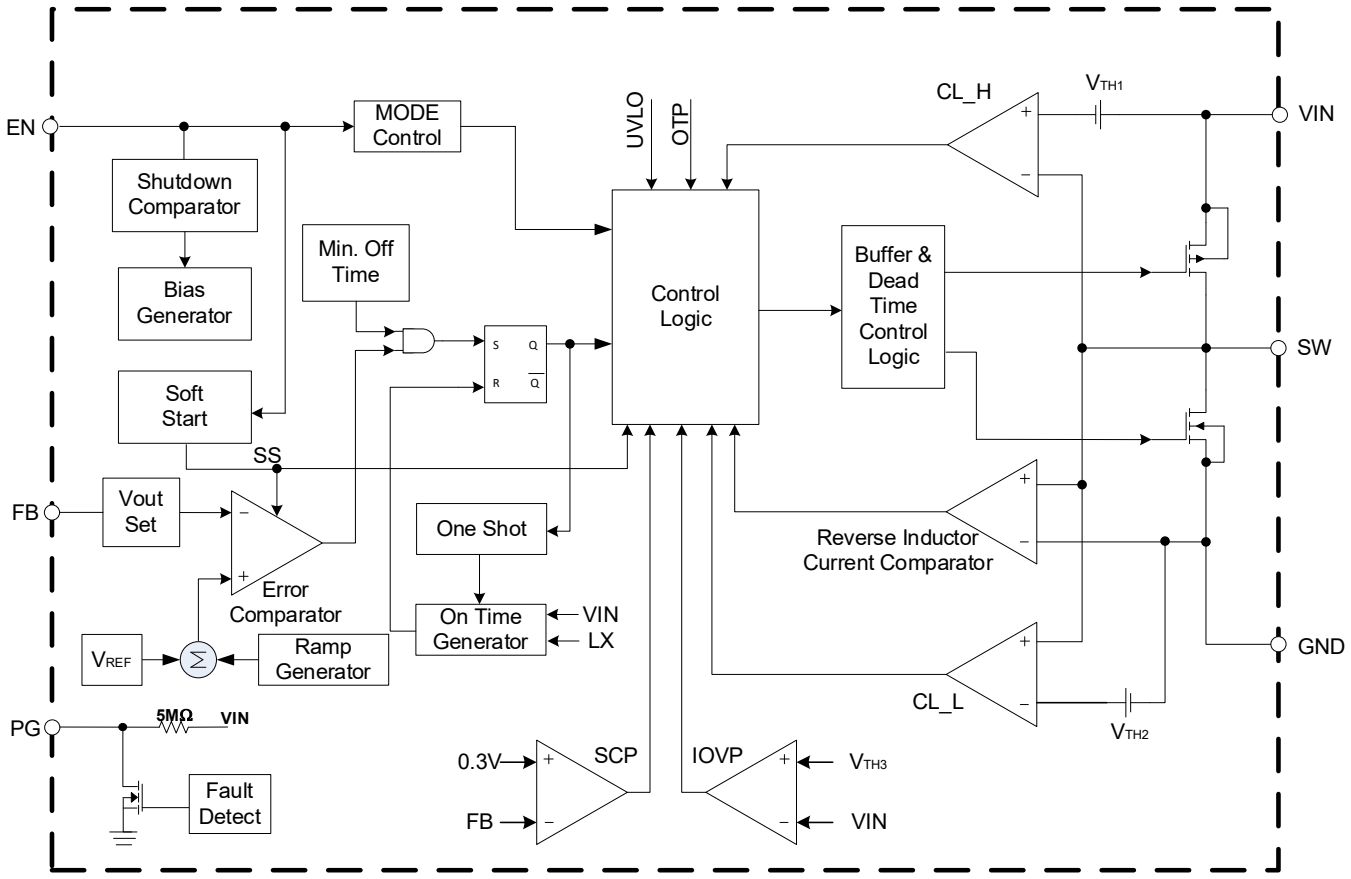


Figure 4. AP61402 Functional Block Diagram

Absolute Maximum Ratings (@T_A = +25°C, unless otherwise specified.) (Note 4)

Parameter	Rating	Unit
Supply Voltage	-0.3 to +6.0 (DC)	V
	-0.3 to 6.5 (400ms)	
Switch Node Voltage	-1.0 to VIN + 0.3 (DC)	V
	-0.3 to VIN + 2.0 (20ns)	
Feedback Voltage	-0.3 to VIN + 0.3	V
All Other Pins	-0.3 to VIN + 0.3	V
Storage Temperature	-65 to +150	°C
Junction Temperature	+160	°C
ESD Susceptibility (Note 5)		
Human Body Model	±2000	V
Charged Device Model	±1000	V

Notes: 4. Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to *Absolute Maximum Ratings* for extended periods can affect device reliability.
5. Semiconductor devices are ESD sensitive and may be damaged by exposure to ESD events. Suitable ESD precautions should be taken when handling and transporting these devices.

Package Thermal Data (Note 6)

Symbol	Parameter	Rating, JEDEC (Note 6)	AP61402 EVM (Note 7)	Unit
θ_{JA}	Junction to Ambient	91	71	°C/W
$\theta_{JC(TOP)}$	Junction to Case (Top)	58	N/A	°C/W
θ_{JB}	Junction to Board (Bottom)	9.8	N/A	°C/W
ψ_{JT}	Junction to Top Characterization Parameter	2.6	2.6	°C/W
ψ_{JB}	Junction to Board Characterization Parameter	9.4	9	°C/W
$\theta_{JC(BOT)}$	Junction to Case (Bottom)	9.6	9	°C/W

Notes: 6. Device mounted on FR-4 substrate, JEDEC 4 layer 50mm x 50mm PCB board (2oz copper), with minimum recommended pad layout.
7. Device mounted on Diodes Incorporated's evaluation board. See user guide for more details.

Recommended Operating Conditions (@T_A = +25°C, unless otherwise specified.) (Note 8)

Symbol	Parameter	Min	Max	Unit
V_{IN}	Supply Voltage	2.3	5.5	V
I_{OUT}	Output Current	—	4	A
T_J	Operating Junction Temperature Range	-40	+125	°C

Note: 8. The device function is not guaranteed outside of the recommended operating conditions.

Electrical Characteristics (T_A = +25°C, VIN = 5V, unless otherwise specified. Min/Max limits apply across the recommended junction temperature range, -40°C to +125°C, and input voltage range, 2.3V to 5.5V.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{SHDN}	Shutdown Supply Current	V_{EN} = 0	—	0.03	—	μA
I_Q	Supply Current (Quiescent)	V_{FB} = 0.65V	—	20	—	μA
UVLO	V_{IN} Undervoltage Threshold (Rising)	—	—	2.15	2.30	V
	V_{IN} Undervoltage Threshold Hysteresis	—	—	150	—	mV
$R_{DS(ON)1}$	High-Side Switch On-Resistance (Note 9)	I_{SW} = 100mA High Side	—	75	—	mΩ
$R_{DS(ON)2}$	Low-Side Switch On-Resistance (Note 9)	I_{SW} = 100mA Low Side	—	33	—	mΩ
R_{DISCH}	Output Discharge Switch On Resistor	—	—	100	—	Ω
I_{PEAK_LIMIT}	HS Peak Current Limit (Note 9)	—	5.0	6.5	8.5	A
I_{VALLEY_LIMIT}	LS Valley Current Limit (Note 9)	—	4.7	5.7	8.0	A
f_{SW}	Switching Frequency	VOUT = 1.8V, CCM	—	2	—	MHz
t_{OFF_MIN}	Minimum Off-Time	—	—	110	—	ns
PG Detection	OVP PG Threshold Reference to FB	OVP FB Rising Edge	—	110	—	%
	OVP Hysteresis	OVP FB Falling Edge	—	5	—	
	UVP PG Threshold Reference to FB	UVP FB Rising Edge	—	95	—	
	UVP Hysteresis	UVP FB Falling Edge	—	5	—	
PG Pullup	PG Pullup Resistor	—	—	5	—	MΩ
PG Low	PG Low Voltage	Rp = 10kΩ	—	—	0.4	V
PG Delay	PG Delay	—	—	40	—	μs
V_{FB}	Feedback Voltage	CCM	490	500	510	mV
V_{EN_H}	EN Logic High	—	—	—	1.2	V
V_{EN_L}	EN Logic Low	—	0.6	—	—	V
I_{EN}	EN Input Current	VIN = V_{EN} = 5V	—	2	—	μA
t_{SS}	Soft-Start Period	—	0.3	0.5	0.7	ms
T_{SD}	Thermal Shutdown (Note 9)	—	—	+160	—	°C
T_{HYS}	Thermal Hysteresis (Note 9)	—	—	+30	—	°C
V_{IOVP}	VIN Overvoltage Protection (Note 9)	—	—	6.3	—	V
V_{IHYS}	VIN Overvoltage Protection Hysteresis (Note 9)	—	—	0.3	—	V

Note: 9. Compliance with the datasheet limits is assured by one or more methods: production test, characterization, and/or design.

Typical Performance Characteristics (AP61402 @ T_A = +25°C, VIN = 5V, VOUT = 1.8V, BOM = Table 1, unless otherwise specified.)

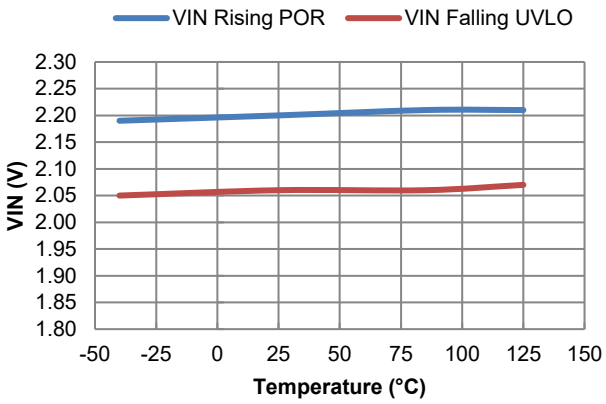


Figure 5. Power MOSFET $R_{DS(ON)}$ vs. Temperature

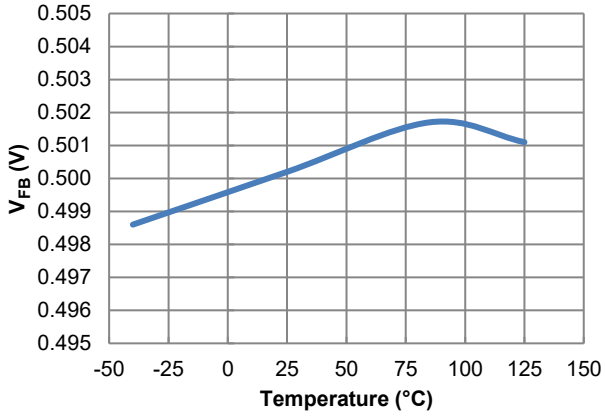


Figure 6. V_{FB} vs. Temperature

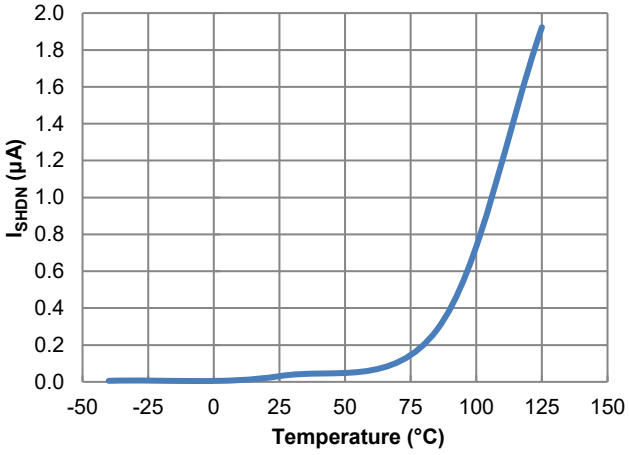


Figure 7. I_{SHDN} vs. Temperature

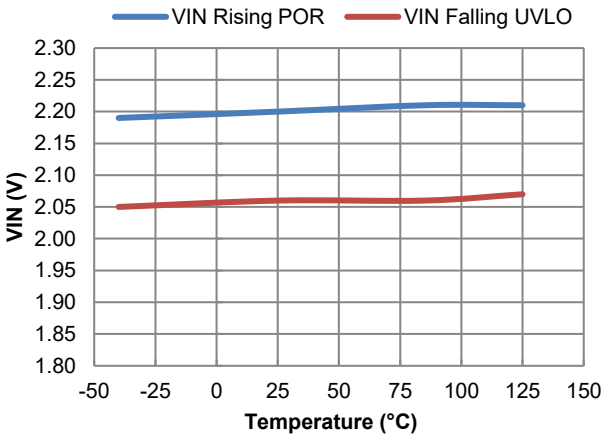


Figure 8. VIN Power-On Reset and UVLO vs. Temperature

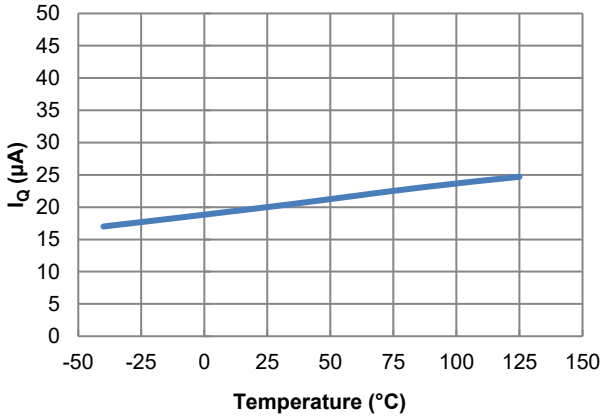


Figure 9. I_Q vs. Temperature

Typical Performance Characteristics (AP61402 @ T_A = +25°C, VIN = 5V, VOUT = 1.8V, BOM = Table 1, **PFM**, unless otherwise specified.)

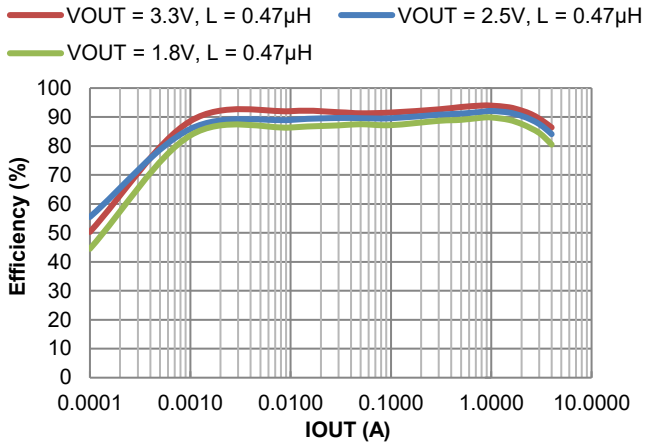


Figure 10. Efficiency vs. Output Current, VIN = 5V

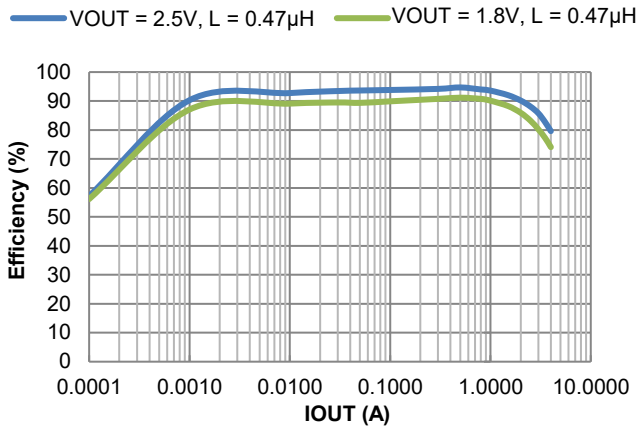


Figure 11. Efficiency vs. Output Current, VIN = 3.3V

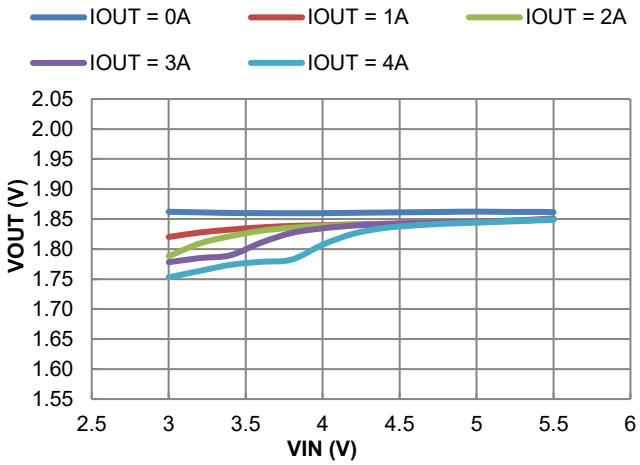


Figure 12. Line Regulation

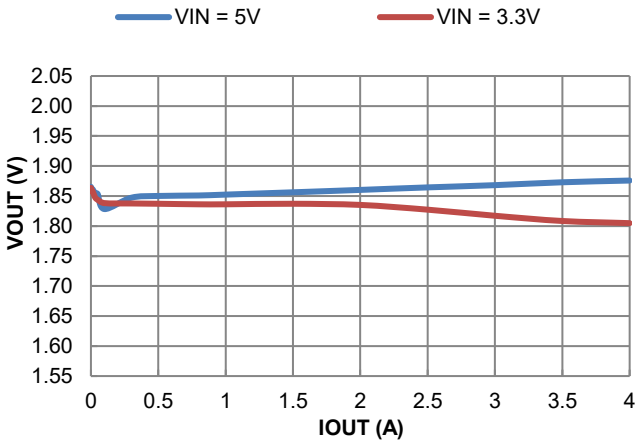


Figure 13. Load Regulation

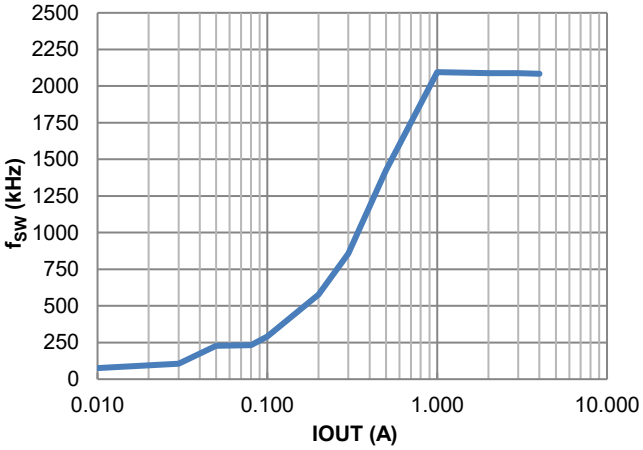


Figure 14. f_{SW} vs. Load

Typical Performance Characteristics (AP61402 @ T_A = +25°C, VIN = 5V, VOUT = 1.8V, BOM = Table 1, **PFM**, unless otherwise specified.) (continued)

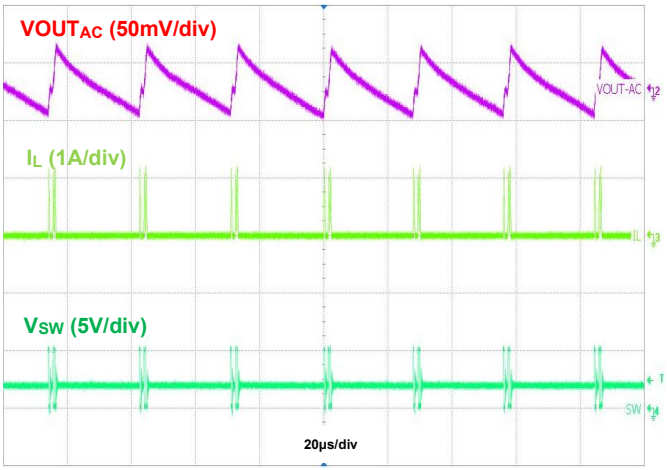


Figure 15. Output Voltage Ripple, IOUT = 50mA

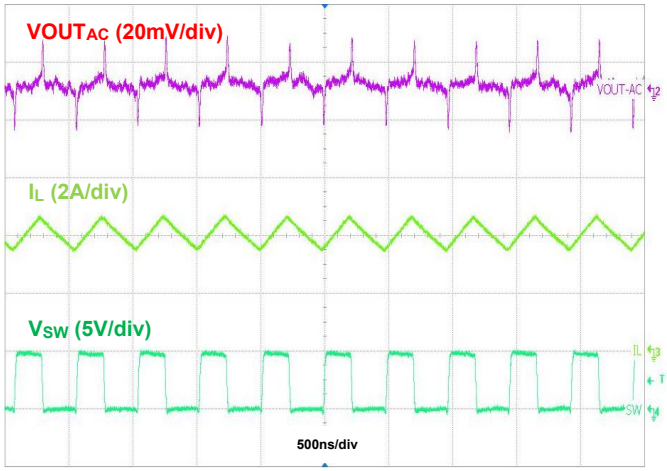


Figure 16. Output Voltage Ripple, IOUT = 4A

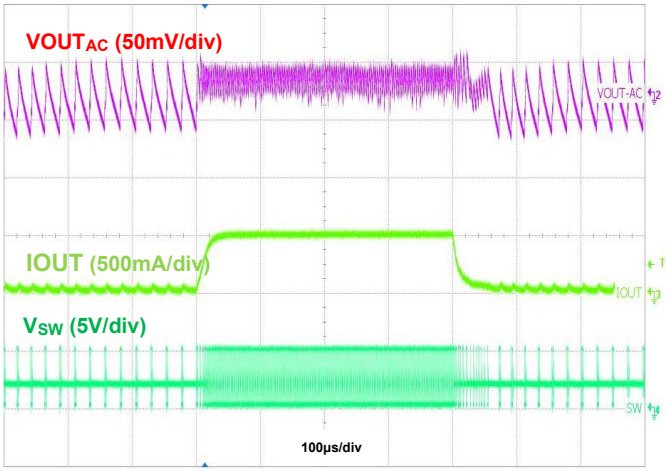


Figure 17. Load Transient, IOUT = 50mA to 500mA to 50mA

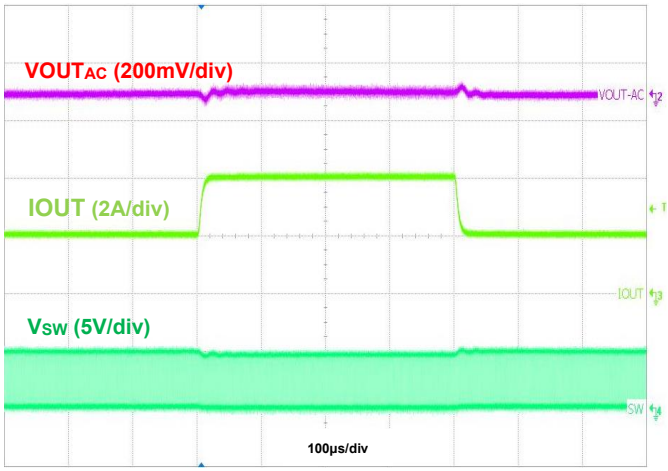


Figure 18. Load Transient, IOUT = 2A to 4A to 4A

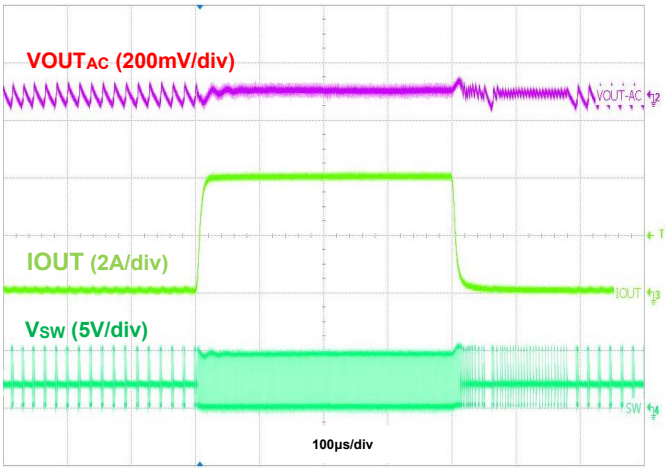


Figure 19. Load Transient, IOUT = 50mA to 4A to 50mA

Typical Performance Characteristics (AP61402 @ T_A = +25°C, VIN = 5V, VOUT = 1.8V, BOM = Table 1, **PWM**, unless otherwise specified.)

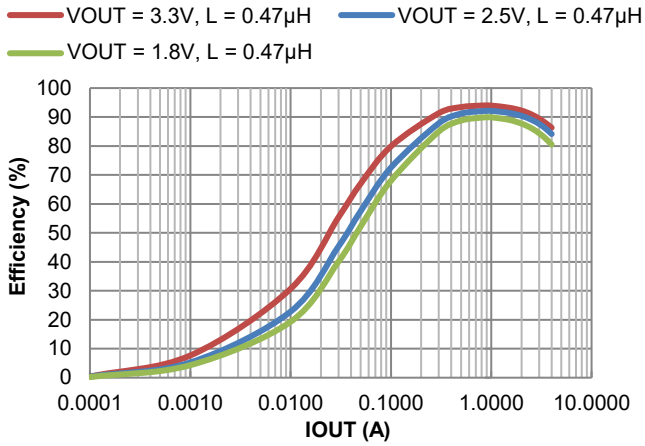


Figure 20. Efficiency vs. Output Current, VIN = 5V

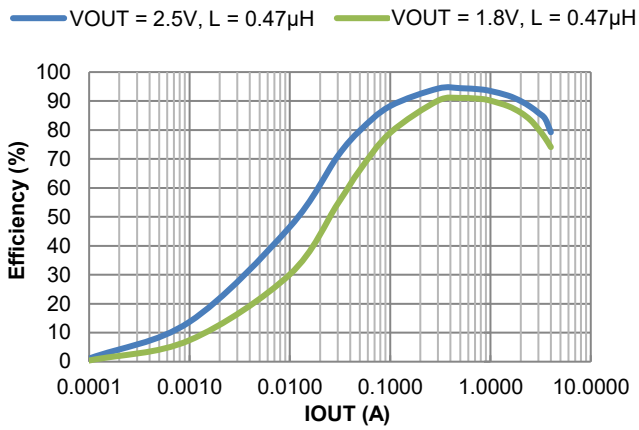


Figure 21. Efficiency vs. Output Current, VIN = 3.3V

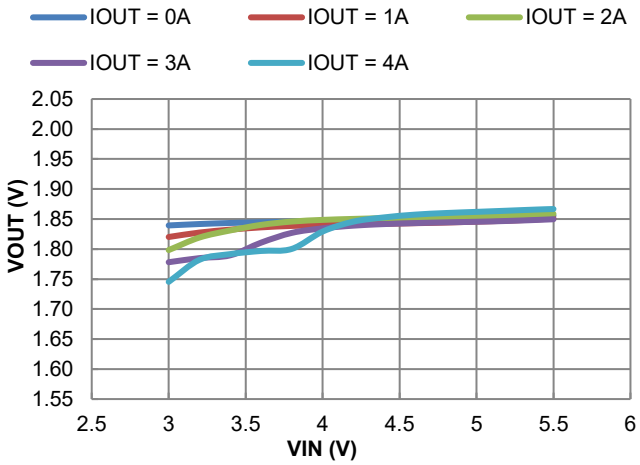


Figure 22. Line Regulation

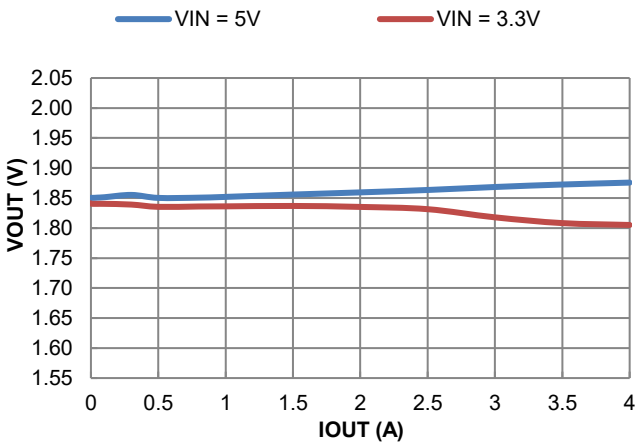


Figure 23. Load Regulation

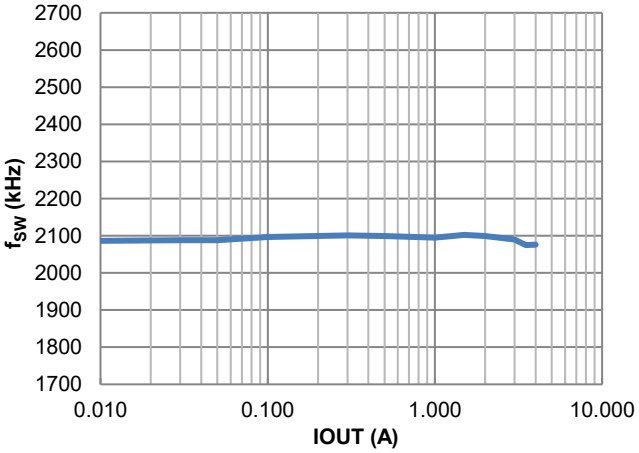


Figure 24. f_{SW} vs. Temperature

Typical Performance Characteristics (AP61402 @ T_A = +25°C, VIN = 5V, VOUT = 1.8V, BOM = Table 1, **PWM**, unless otherwise specified.) (continued)

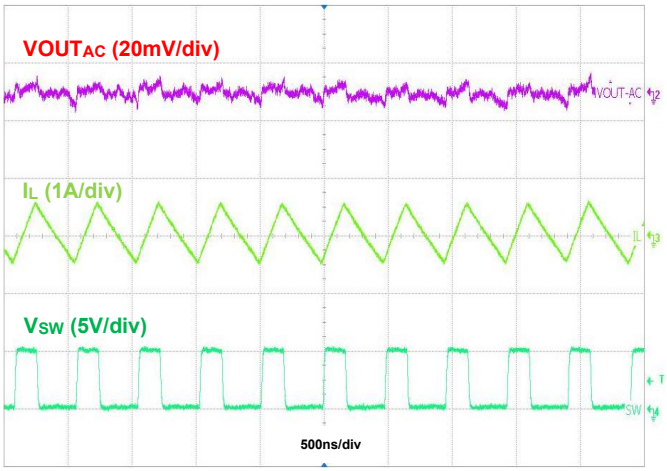


Figure 25. Output Voltage Ripple, IOUT = 50mA

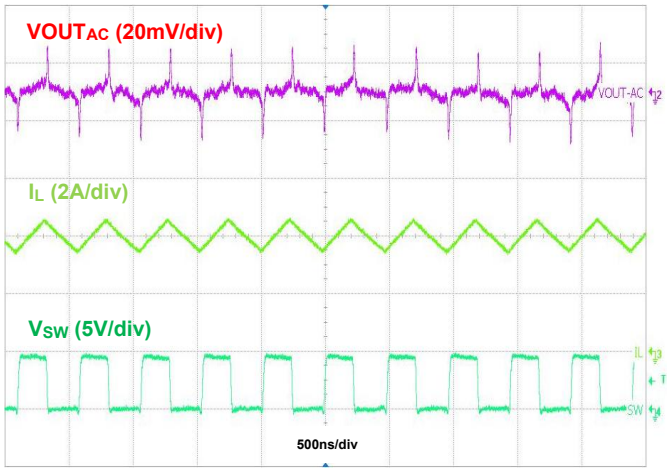


Figure 26. Output Voltage Ripple, IOUT = 4A

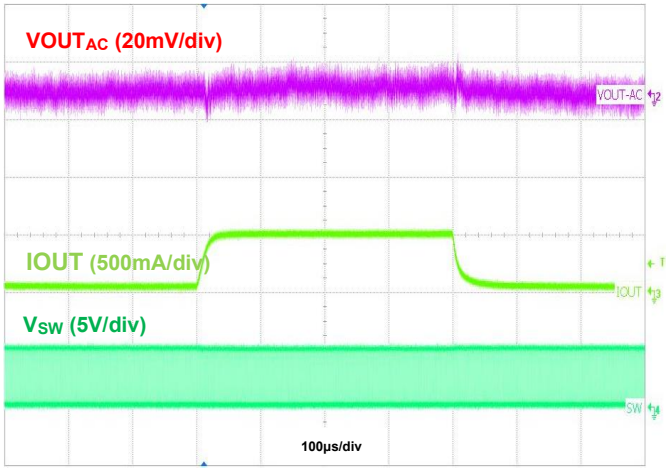


Figure 27. Load Transient, IOUT = 50mA to 500mA to 50mA

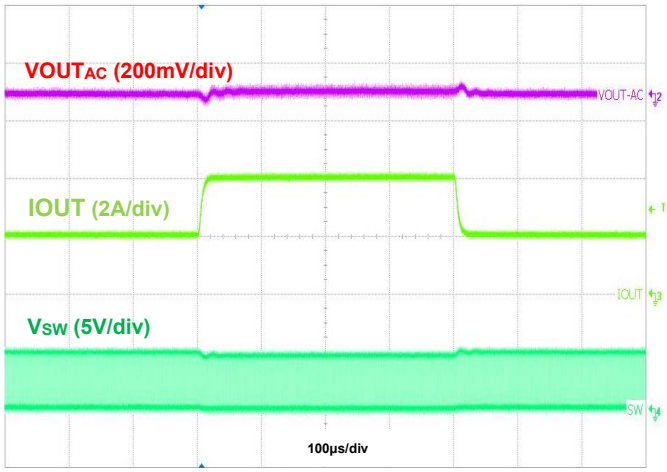


Figure 28. Load Transient, IOUT = 2A to 4A to 4A

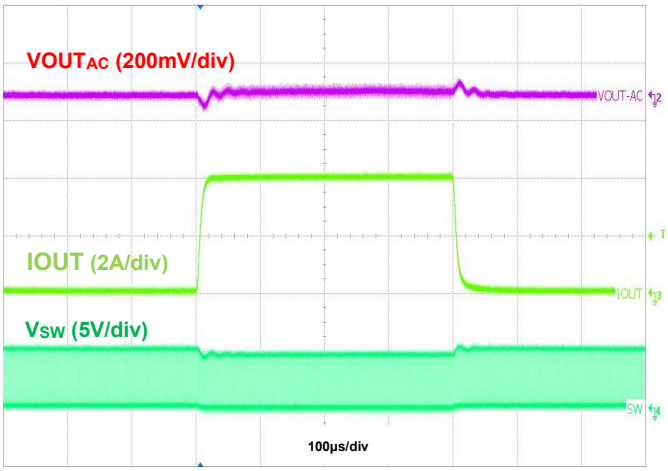


Figure 29. Load Transient, IOUT = 50mA to 4A to 50mA

Typical Performance Characteristics (AP61402 @ T_A = +25°C, VIN = 5V, VOUT = 1.8V, BOM = Table 1, unless otherwise specified.)

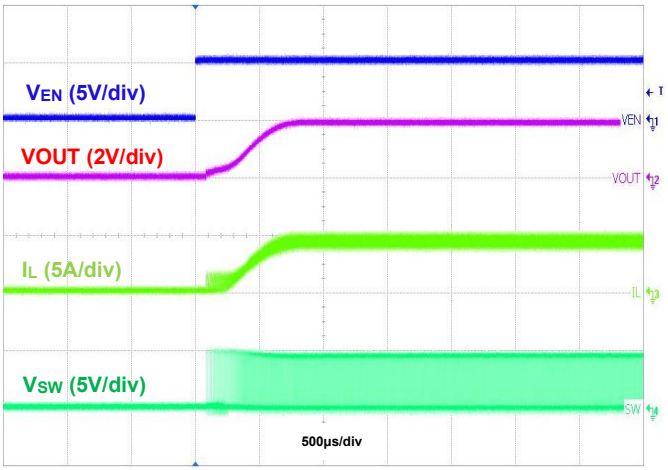


Figure 30. Startup Using EN, IOUT = 4A

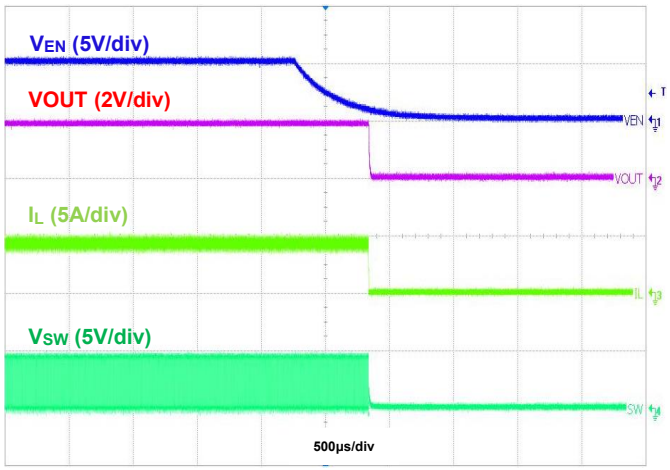


Figure 31. Shutdown Using EN, IOUT = 4A

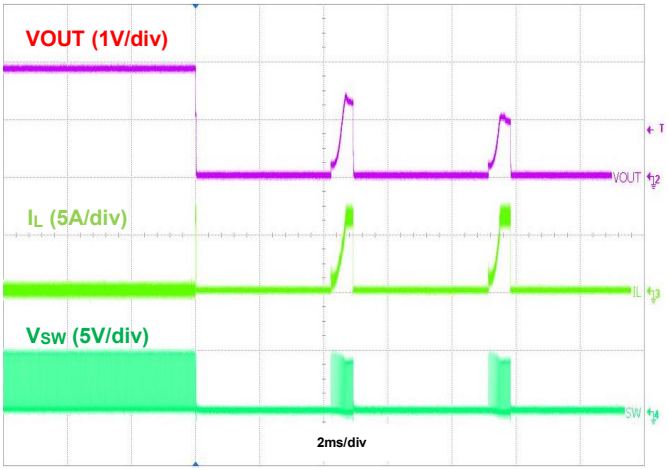


Figure 32. Output Short Protection, IOUT = 0

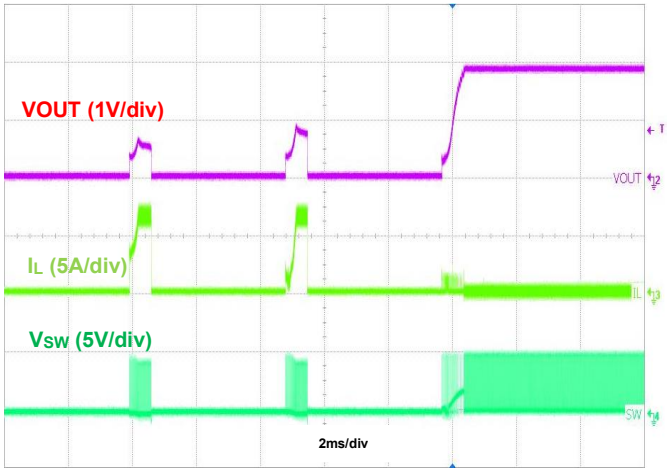


Figure 33. Output Short Recovery, IOUT = 0

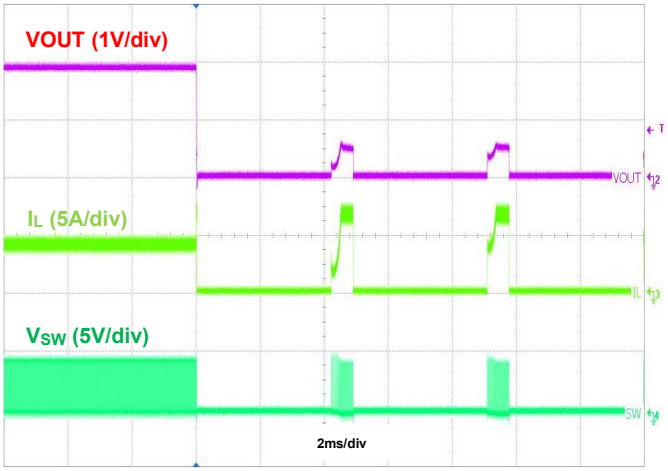


Figure 34. Output Short Protection, IOUT = 4A

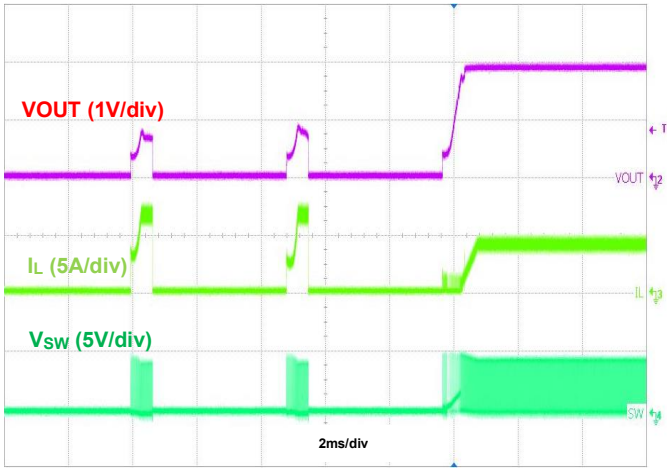


Figure 35. Output Short Recovery, IOUT = 4A

Typical Performance Characteristics (AP61402 @ T_A = +25°C, VIN = 5V, VOUT = 1.8V, BOM = Table 1, unless otherwise specified.) (continued)

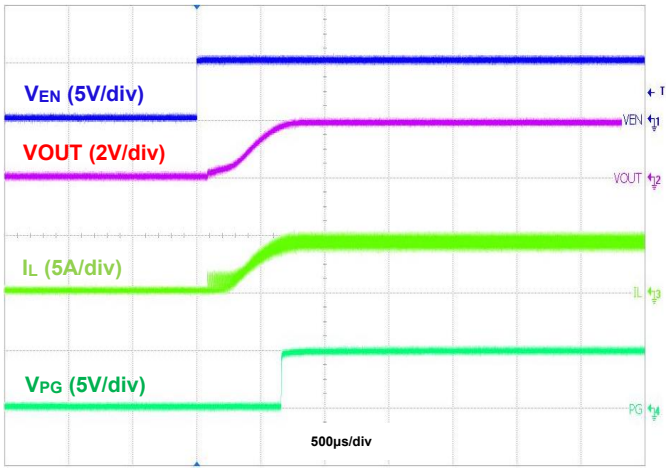


Figure 36. Startup Using EN with VPG, IOUT = 4A

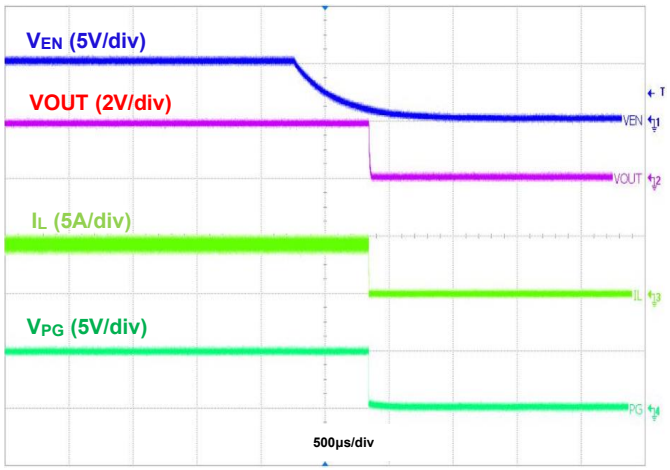


Figure 37. Shutdown Using EN with VPG, IOUT = 4A

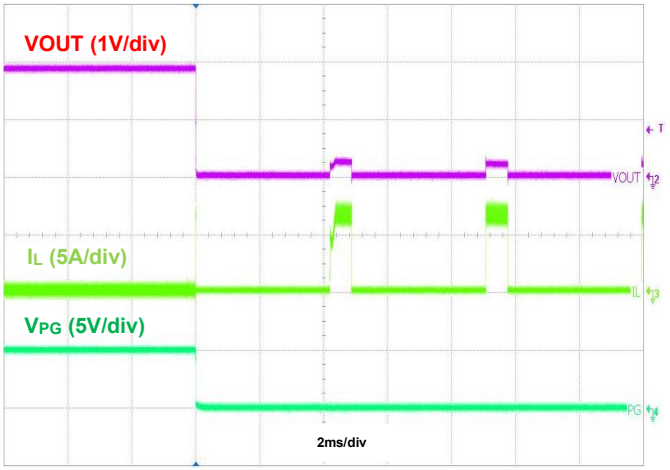


Figure 38. Output Short Protection with VPG, IOUT = 0

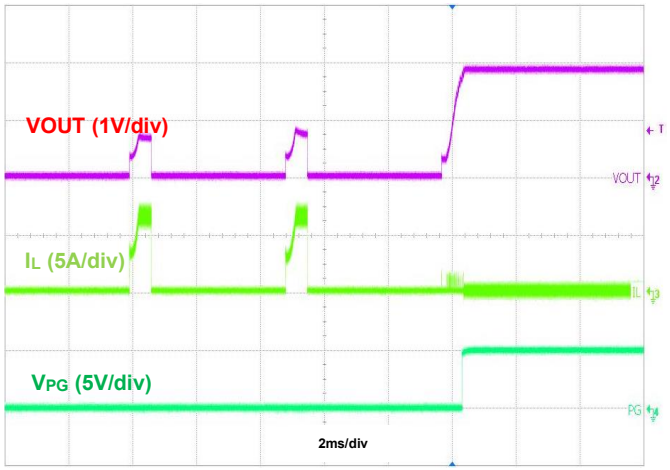


Figure 39. Output Short Recovery with VPG, IOUT = 0

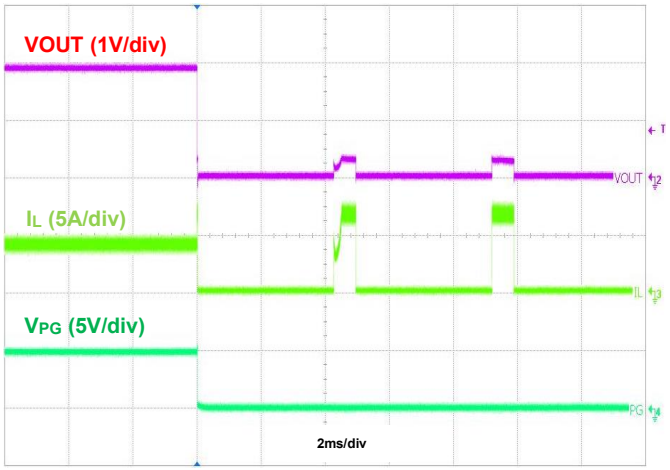


Figure 40. Output Short Protection with VPG, IOUT = 4A

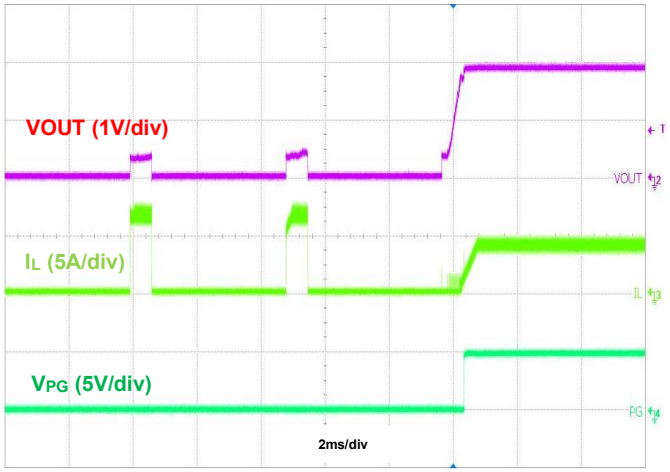


Figure 41. Output Short Recovery with VPG, IOUT = 4A

Application Information

Constant-On-Time Control

The Constant-On-Time control architecture allows for fast transient response and requires no loop compensation, which reduces external component count and reduces design complexity.

The COT control relies on a fixed switch on time to regulate the output. The on-time of the high-side switch can be estimated as:

$$t_{ON} = 500ns \times (V_{OUT}/V_{IN})$$

The AP61402 has a fixed minimum off-time of 60ns, which can prevent the inductor current runaway during load transient.

Undervoltage Lockout (UVLO) Circuit

When the V_{IN} drops lower than the UVLO detector threshold (2V typ), the UVLO circuit starts to operate, V_{REF} stops, and with the high-side and low-side switch turned "OFF". As a result, V_{OUT} drops according to the COUT capacitance value and the load. When the V_{IN} is rising higher than UVLO released voltage (2.15V typ), the IC will restart the operation.

Current Limit Protection

The AP61402 typically has a 4A high-side switch current limit to 6A. When the current flowing into high-side switch reaches the current limit threshold, the AP61402 will enter cycle by cycle current limit mode until the current drops. Also, a cycle-by-cycle valley current detect circuit is implemented for current limit. The switch current is monitored during the low-side switch on state; if the monitored current is above the current threshold, the converter maintains low-side switch on until the current level becomes threshold level or lower.

Short-Circuit Protection and Recovery

When the AP61402 output node is shorted to GND and V_{FB} drops under 0.36V, it will enter hiccup mode to lower power loss. If the short circuit is removed, and V_{FB} rises over 0.36V, the AP61402 recovers to normal operation again.

Overtemperature Protection

The internal thermal temperature protection circuitry is provided to protect the integrated circuit if the maximum junction temperature is exceeded. When the junction temperature exceeds +160°C, it shuts down the internal control circuit and switches. The AP61402 will restart automatically under the control of soft-start circuit when the junction temperature decreases to +130°C.

Enable

When disabled, the device shutdown supply current is only 0.1μA. When applying a voltage greater than the EN logic-high threshold (typical 0.91V, rising), the AP61402 enables all functions, and the device initiates the soft-start phase. The AP61402 has a built-in 0.5ms soft-start time to prevent output voltage overshot and inrush current. When the EN voltage falls below its logic-low threshold (typical 0.83V, falling), the internal SS voltage discharges to ground and device operation is disabled.

PWM, Continuous Conduction Mode Operation

The device operates in PFM when a logic-high voltage is applied to the EN pin greater than VIN – 200mV. The device operates in PWM regardless of output load when a logic-high voltage is applied to the EN pin less than VIN – 200mV. Connect a resistive divider 100kΩ/200kΩ from EN to GND, and the device enters PWM and operates with a constant switching frequency over the entire load range, even at very light loads. This allows predictable operational frequency across loading and avoids potential interference to other sensitive circuitries.

Application Information (continued)

Setting the Output Voltage

There are fixed output voltage options to support most applications. The output voltage can also be adjusted from 1V to 5V using an external resistor divider with an adjustable version. Table 1 shows a list of resistor selections for common output voltages. Resistor R1 is selected based on a design tradeoff between efficiency and output voltage accuracy. For the high values of R1 there is less current consumption in the feedback network. However, the tradeoff is output voltage accuracy due to the bias current in the error amplifier. R1 can be determined by the following equation:

$$\mathbf{R1 = R2 \cdot \left(\frac{VOUT}{0.5V} - 1\right)} \quad \textbf{Eq. 1}$$

Table 1

AP61402						
Output Voltage (V)	**R1 (kΩ)**	**R2 (kΩ)**	**L (μH)**	**C1 (μF)**	**C2 (μF)**	**C3 (CFF) (pF)**
1.2	14	10	0.47	22	22	33
1.5	20	10	0.47	22	22	33
1.8	26	10	0.47	22	22	33
2.5	40	10	0.47	22	22	33
3.3	56	10	0.47	22	22	33

Input Capacitor

The input capacitor reduces both the surge current drawn from the input supply as well as the switching noise from the device. The input capacitor must sustain the ripple current produced during the on-time of Q1. It must have a low ESR to minimize power dissipation due to the RMS input current.

The RMS current rating of the input capacitor is a critical parameter and must be higher than the RMS input current. As a rule of thumb, select an input capacitor with an RMS current rating greater than half of the maximum load current.

Due to large di/dt through the input capacitor, electrolytic or ceramic capacitors with low ESR should be used. If using a tantalum capacitor, it must be surge protected or else capacitor failure could occur. Using a ceramic capacitor of 22μF or greater is sufficient for most applications.

Output Capacitor

The output capacitor keeps the output voltage ripple small, ensures feedback loop stability, and reduces both the overshoots and undershoots of the output voltage during load transients. During the first few microseconds of an increasing load transient, the converter recognizes the change from steady state and sets the off-time to minimum to supply more current to the load. However, the inductor limits the change in increasing current depending on its inductance. Therefore, the output capacitor supplies the difference in current to the load during this time. Likewise, during the first few microseconds of a decreasing load transient, the converter recognizes the change from steady state and increases the off-time to reduce the current supplied to the load. However, the inductor limits the change in decreasing current as well. Therefore, the output capacitor absorbs the excess current from the inductor during this time.

The effective output capacitance, COUT, requirements can be calculated from the equations below.

The ESR of the output capacitor dominates the output voltage ripple. The amount of ripples can be calculated by:

$$\mathbf{VOUT_{Ripple} = \Delta I_L \cdot \left(ESR + \frac{1}{8 \cdot f_{sw} \cdot COUT}\right)} \quad \textbf{Eq. 2}$$

An output capacitor with large capacitance and low ESR is the best option. For most applications, a 10μF to 22μF ceramic capacitor is sufficient. To meet the load transient requirements, the calculated COUT should satisfy the following inequality:

$$\mathbf{COUT > max\left(\frac{L \cdot I_{Trans}^2}{\Delta V_{Overshoot} \cdot VOUT}, \frac{L \cdot I_{Trans}^2}{\Delta V_{Undershoot} \cdot (VIN - VOUT)}\right)} \quad \textbf{Eq. 3}$$

Where:

- I_{Trans} is the load transient.
- $\Delta V_{Overshoot}$ is the maximum output overshoot voltage.
- $\Delta V_{Undershoot}$ is the maximum output undershoot voltage.

Application Information (continued)

PCB Layout

1. The AP61402 device works at 4A current load, so heat dissipation is a major concern in the layout of the PCB. 2oz copper for both the top and bottom layers is recommended.
2. Provide sufficient vias for the input and output capacitors' GND side to dissipate heat to the bottom layer.
3. Make the bottom layer under the device as the GND layer for heat dissipation. The GND layer should be as large as possible to provide better thermal effects.
4. Place the VIN capacitors as close to the device as possible.
5. Place the feedback components as close to FB as possible.
6. See Figure 42 for reference.

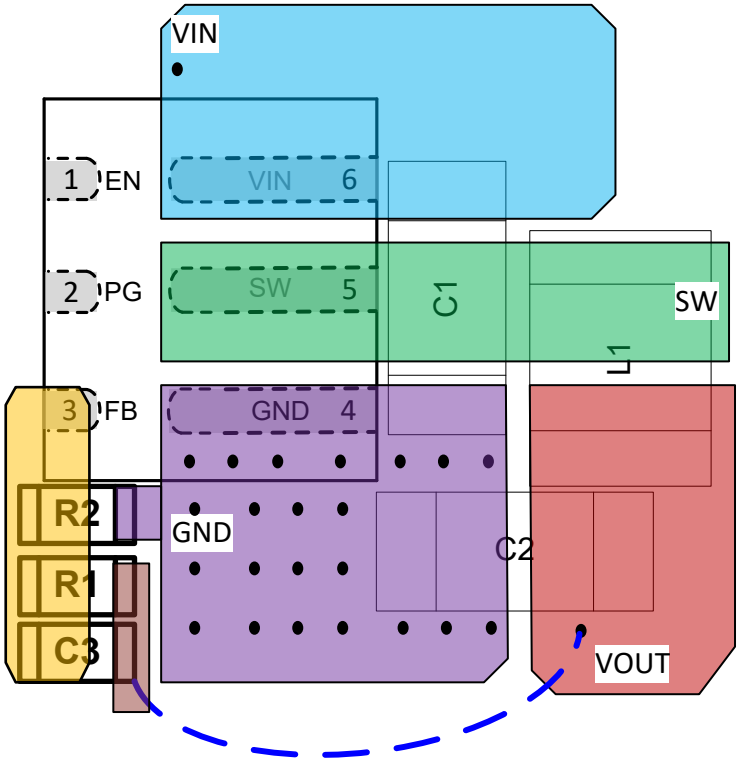
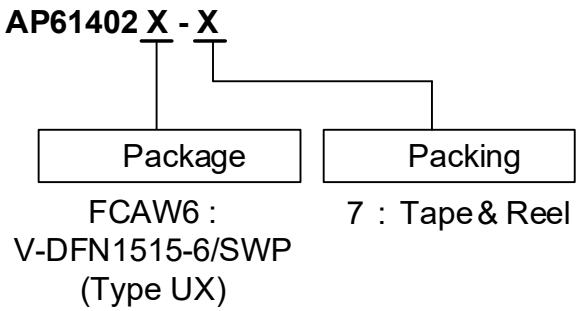


Figure 42. Recommended Layout

Ordering Information (Note 10)



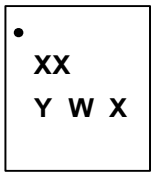
Orderable Part Number	Package	Package Code	Packing	
			Qty.	Carrier
AP61402FCAW6-7	V-DFN1515-6/SWP (Type UX)	FCAW6	3000	Tape & Reel

Note: 10. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information

V-DFN1515-6/SWP (Type UX)

(Top View)



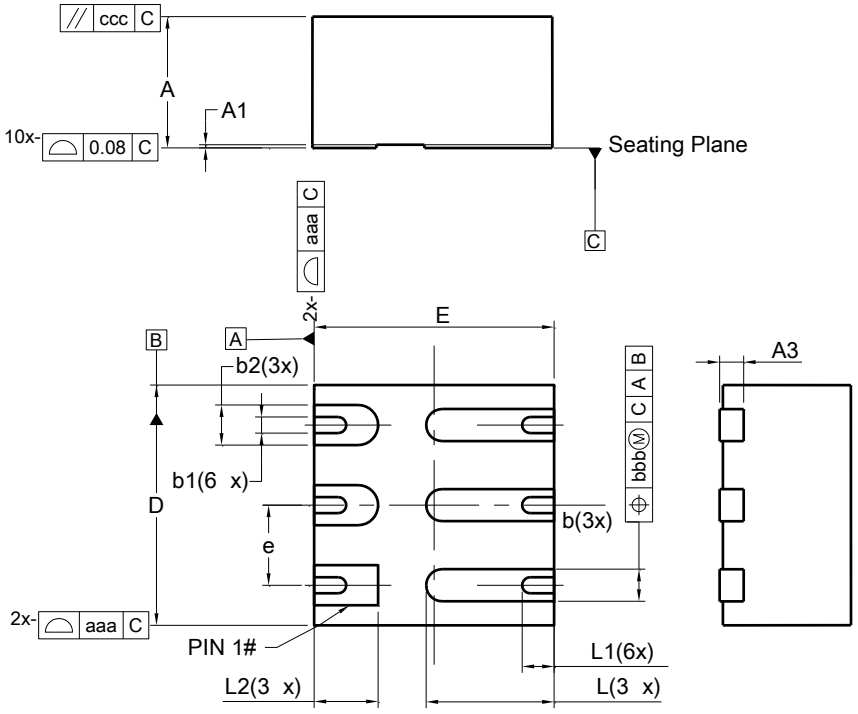
XX : Identification Code
Y : Year 0 to 9 (ex: 5 = 2025)
W : Week: A to Z: week 1 to 26
a to z: week 27 to 52; z represents
week 52 and 53
X : Internal Code

Orderable Part Number	Package	Identification Code
AP61402FCAW6-7	V-DFN1515-6/SWP (Type UX)	H2

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

V-DFN1515-6/SWP (Type UX)

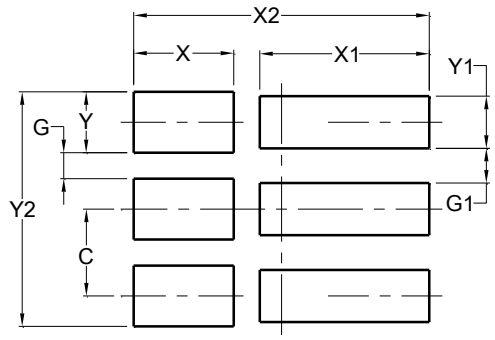


V-DFN1515-6/SWP (Type UX)			
Dim	**Min**	**Max**	**Typ**
A	0.75	0.85	0.80
A1	0.00	0.05	0.03
A3	--	--	0.127
b	0.150	0.250	0.200
b1	0.070	0.130	0.100
b2	0.200	0.300	0.250
D	1.45	1.55	1.50
E	1.45	1.55	1.50
e	--	--	0.500
L	0.700	0.900	0.800
L1	0.150	0.250	0.200
L2	0.300	0.500	0.400
aaa	0.15		
bbb	0.05		
ccc	0.05		
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

V-DFN1515-6/SWP (Type UX)



Dimensions	Value (in mm)
C	0.500
G	0.150
G1	0.200
X	0.575
X1	0.975
X2	1.700
Y	0.350
Y1	0.300
Y2	1.350

Mechanical Data

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads, Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.008 grams (Approximate)

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