Description

The AP61040 is a low-current synchronous buck converter providing high efficiency, excellent transient response, and high DC output accuracy. The ultra-low I_Q of the AP61040 makes it ideal for applications such as fitness wearables, health monitoring, Bluetooth, and other handheld devices. The AP61040 regulator is optimized to operate with 2.2µH and 10µF output capacitors. The device provides at least 400mA output current and in an input voltage range of 2.15V to 5.5V.

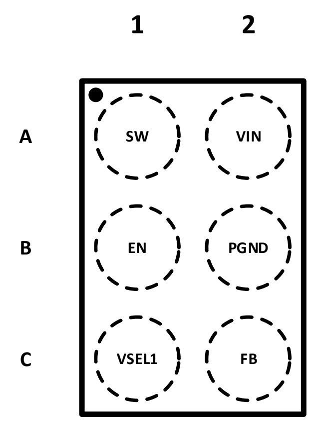
The current control scheme handles wide input/output voltage ratios and provides a low external component count with outstanding performance in line/load transient response and seamless transition between buck and 100% duty cycle modes.

The AP61040 provides three programmable output voltages between 0.6V to 3.3V, selectable by one selection pin. The device also features undervoltage lockout (UVLO), overtemperature protection (OTP), and overcurrent protection (OCP) to protect the circuit.

This IC is available in a small 1.17mm x 0.77mm, 6-ball, WLCSP package.

Pin Assignments

TOP VIEW



X1-WLB1208-6

Features

- V_{IN} 2.15V to 5.5V
- Output Voltage Range: 0.6V to 5.5V
  - Three Selectable Voltages between 0.6V, 2.5V, and 3.3V
- 400mA Continuous Output Current, Efficiency up to 95%
- 930nA Quiescent Current to Maximize Light-Load Efficiency
- 1.1MHz Switching Frequency
- Programmable Operation Mode through EN
  - Pulse-Frequency Modulation
  - Pulse-Width Modulation Regardless of Output Load
- Fully Protected for Overcurrent, Short Circuit, Overtemperature, and Undervoltage Lockout
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/**

Applications

- Wearables
- Fitness trackers
- Smart watches
- Health monitors
- Bluetooth low-energy devices
- Ultra-low power applications
- Energy harvesting

Notes: 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Typical Applications Circuit

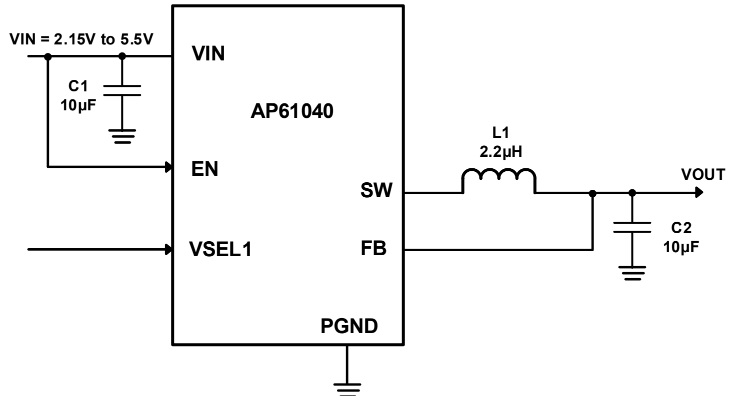


Figure 1. Typical Application Circuit

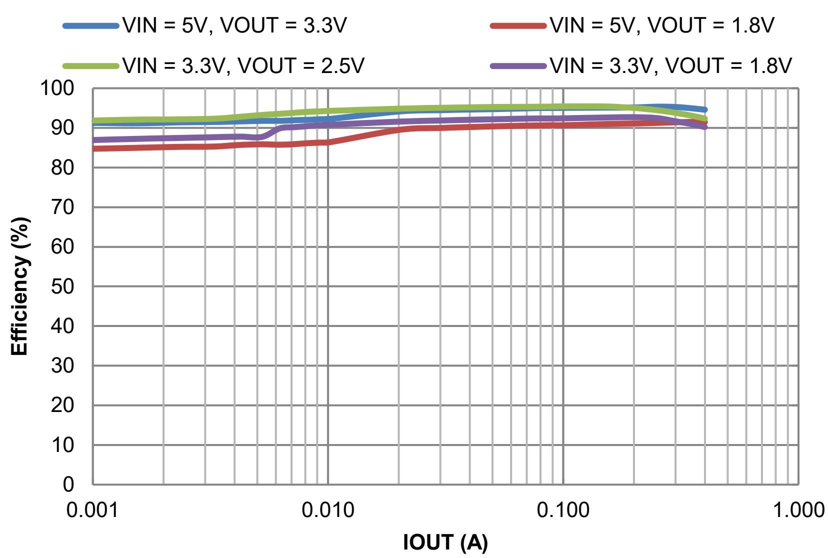


Figure 2. PFM Efficiency vs. Output Current

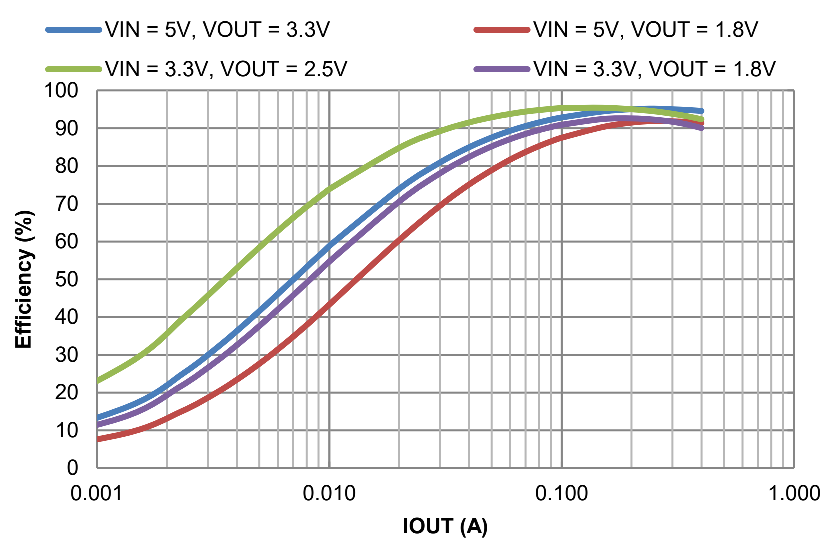


Figure 3. PWM Efficiency vs. Output Current

Pin Descriptions

Pin Name	Pin Number	Function
	6 BALLS	
SW	A1	Switch Node.
VIN	A2	Input supply for the logic control circuitries.
EN	B1	Enable Input. EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator and low to turn it off. EN is used to program the operation mode (PFM or PWM). See *Enable Control* section for more details.
PGND	B2	Power Ground and analog ground that is used for control.
VSEL1	C1	Output voltage select pin 1. See *Setting the Output Voltage* section for more details. This pin can be dynamically changed during operation.
FB	C2	Feedback sensing terminal for the output voltage. Connect this pin to the resistive divider of the output. See *Setting the Output Voltage* section for more details.

Functional Block Diagram

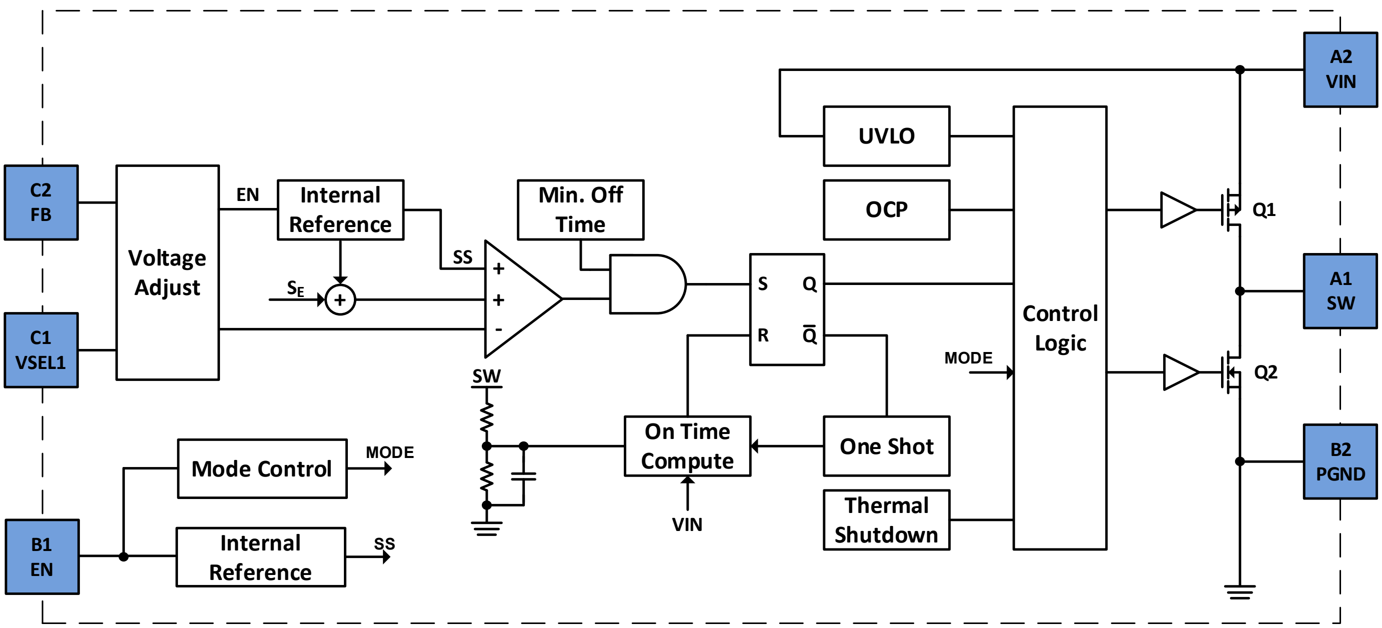


Figure 4. Functional Block Diagram

Absolute Maximum Ratings (Note 4) (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Rating	Unit
V_{IN}	Supply Voltage	-0.3 to +7.0	V
V_{SW}	Switch Node Voltage	-1.0 to V_{IN} +0.3 (DC)	V
V_{SW}	Switch Node Voltage	-2.5 to 8V (20ns)	V
All other pins	-	-0.3V to +7.0	V
T_J	Junction Temperature	+150	°C
T_L	Lead Temperature	+260	°C
ESD Susceptibility (Note 5)			
HBM	Human Body Mode	3000	V
CDM	Charged Device Model	1000	V

Notes: 4. Stresses greater than the 'Absolute Maximum Ratings' specified above may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions exceeding those indicated in this specification is not implied. Device reliability may be affected by exposure to absolute maximum rating conditions for extended periods of time.
5. Semiconductor devices are ESD sensitive and may be damaged by exposure to ESD events. Suitable ESD precautions should be taken when handling and transporting these devices.

Thermal Resistance

Symbol	Parameter	Package	Rating, JEDEC (Note 6)	AP61040 EVM (Note 7)	Unit
θ_{JA}	Junction to Ambient	WLB1208-6	100	60	°C/W
$\theta_{JC(TOP)}$	Junction to Case (Top)	WLB1208-6	49	35	°C/W
θ_{JB}	Junction to Board (bottom)	WLB1208-6	15.7	12	°C/W
ψ_{JT}	Junction to Top Characterization Parameter	WLB1208-6	4.6	1.2	°C/W
ψ_{JB}	Junction to Board Characterization Parameter	WLB1208-6	15	12	°C/W
$\theta_{JC(BOT)}$	Junction to Case (Bottom)	WLB1208-6	-	-	°C/W

Notes: 6. Device mounted on FR-4 substrate, JEDEC 4 layer 50mm x 50mm PCB board (2 oz copper), with minimum recommended pad layout.
7. Device mounted on Diodes evaluation board. See user guide for more detail.

Recommended Operating Conditions (Note 8) (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Min	Max	Unit
VIN	Supply Voltage	2.15	5.5	V
IOUT	Output Current, 2.15V<VIN<2.5V, VOUT<1.8V	-	300	mA
	Output Current, VIN>2.5V	-	400	
T_J	Operating Junction Temperature	-40	+125	°C

Note: 8. The device function is not guaranteed outside of the recommended operating conditions.

Electrical Characteristics (At T_J = +25°C, VIN = 3.6V, V_{EN} = 3.6V unless otherwise specified. Min/Max limits apply across the recommended operating junction temperature range, -40°C to +125°C, and input voltage range, 2.15V to 5.5V, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{SHDN}	Shutdown Supply Current	V_{EN} = 0V, VIN=5.5V	-	34	470	nA
I_Q	Supply Current (Quiescent)	V_{EN} = VIN, VSEL1=Open, V_{FB} = 1.0V	-	930	1500	nA
		PFM, V_{EN} = VIN	-	1000	1600	nA
		PWM, VSEL1=Open, V_{FB} = 1.0V	-	93	-	μA
POR/UVLO	V_{IN} Power On Reset Voltage Threshold, Rising Edge	-	-	2.07	2.15	V
	Vin, Undervoltage Lockout Threshold, Falling Edge	-	-	1.90	2.00	V
	Hysteresis	-	-	170	-	mV
$R_{DS(ON)1}$	High-Side Switch On-Resistance from VIN to SW	-	-	321	440	mΩ
$R_{DS(ON)2}$	Low-Side Switch On-Resistance from SW to PGND	-	-	150	210	mΩ
$R_{Discharge}$	VOUT Soft Discharge On-Resistance	-	-	50	-	Ω
Leakage Current SW	HS Q1 Leakage Current	SW= 0V, VIN=5.5V, EN=0V	-	-	1	μA
I_{LIMIT}	Positive HS Current Limit, Q1	-	600	800	-	mA
I_{LIMIT_VALLEY}	LS Current Limit, Q2 Current from Source to Drain	-	-	470	-	mA
I_{NLIMIT}	Negative LS Current Limit, Q2 Current from Drain to Source	-	-	400	-	mA
F_{SW}	Oscillator Frequency	-	-	1.1	-	MHz
VFB	Feedback Voltage	VSEL1 = OPEN	0.588	0.6	0.612	V
		VSEL1 = GND	2.450	2.500	2.550	V
		VSEL1 = VIN	3.235	3.300	3.365	V
V_{EN}	EN Logic High	-	1.4	-	-	V
	EN Logic Low	-		-	0.4	V
V_{VSEL1}	VSEL1 Logic High	-	1.4	-	-	V
	VSEL1 Logic OPEN	-	0.5	-	0.9	V
	VSEL1 Logic Low	-	-	-	0.4	V
T_{SS}	Soft-Start Period	-	-	0.8	-	ms
T_{SD}	Thermal Shutdown (Note 9)	-	-	150	-	°C
	Thermal Hysteresis (Note 9)	-	-	25	-	°C

Note: 9. Compliance to the datasheet limits is assured by one or more methods: production test, characterization, and/or design.

Typical Performance Characteristics (AP61040 @ TA = +25°C, VIN = 5V, VOUT = 2.5V, PFM, unless otherwise specified.) (continued)

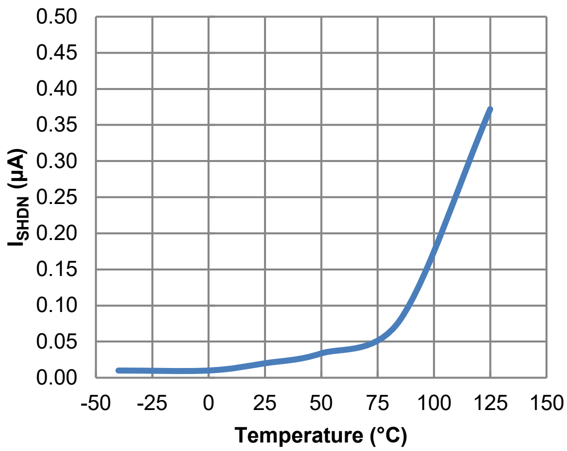


Figure 5. I_{SHDN} vs. Temperature

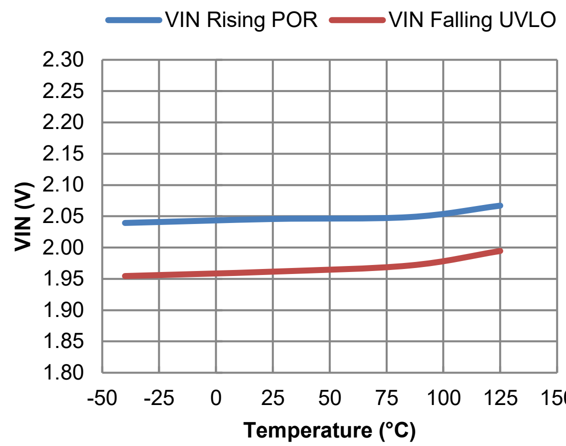


Figure 6. VIN Power-On Reset and UVLO vs. Temperature

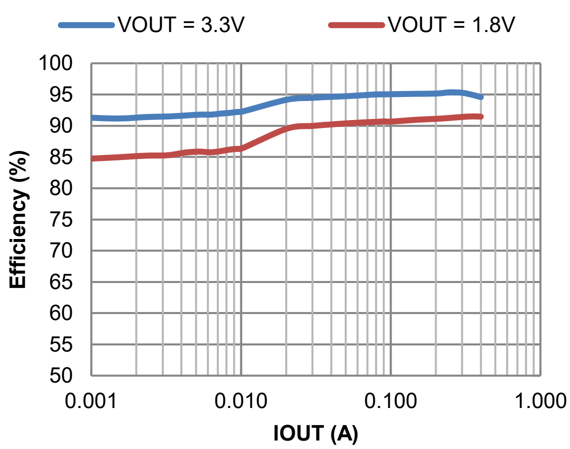


Figure 7. Efficiency vs. Output Current, VIN = 5V

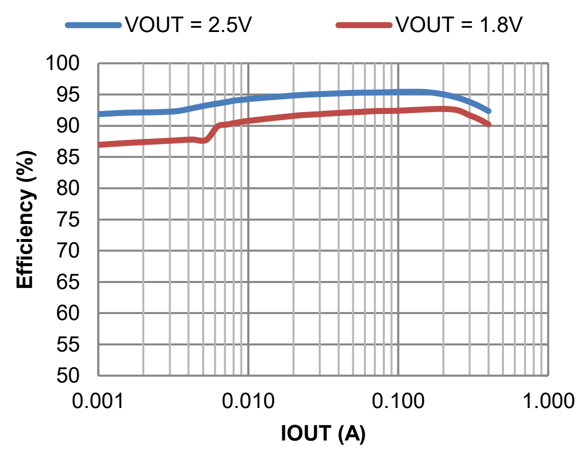


Figure 8. Efficiency vs. Output Current, VIN = 3.3V

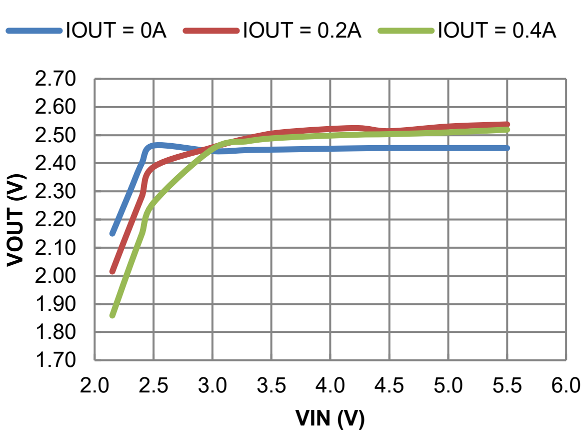


Figure 9. Line Regulation

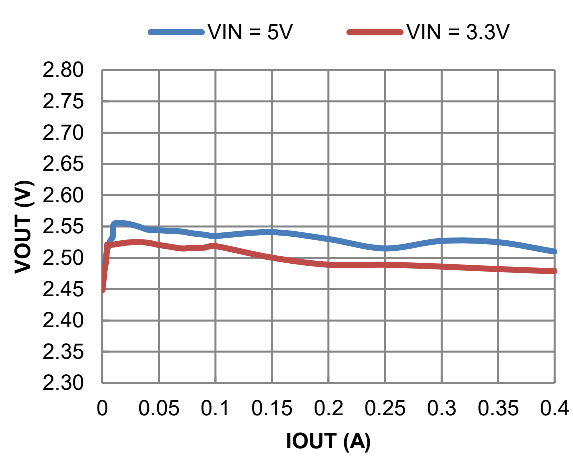


Figure 10. Load Regulation

Typical Performance Characteristics (AP61040 @ TA = +25°C, VIN = 5V, VOUT = 2.5V, PFM, unless otherwise specified.) (continued)

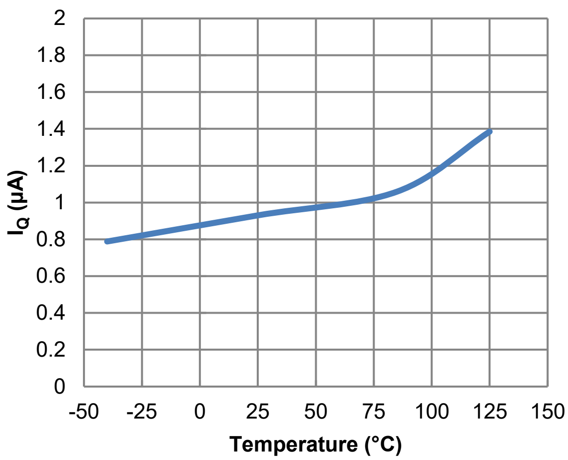


Figure 11. IQ vs. Temperature

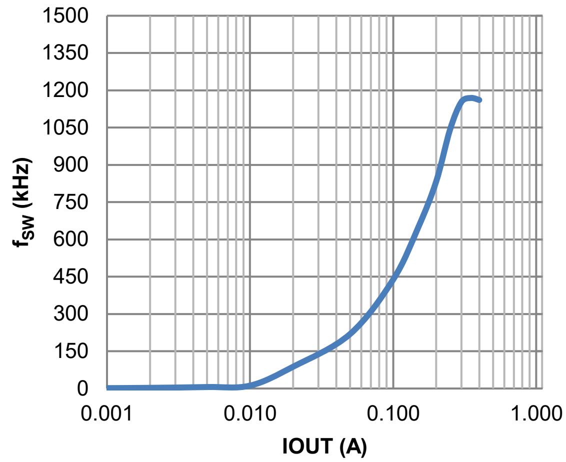


Figure 12. fsw vs. Load

Typical Performance Characteristics (AP61040 @ TA = +25°C, VIN = 5V, VOUT = 2.5V, PFM, unless otherwise specified.) (continued)

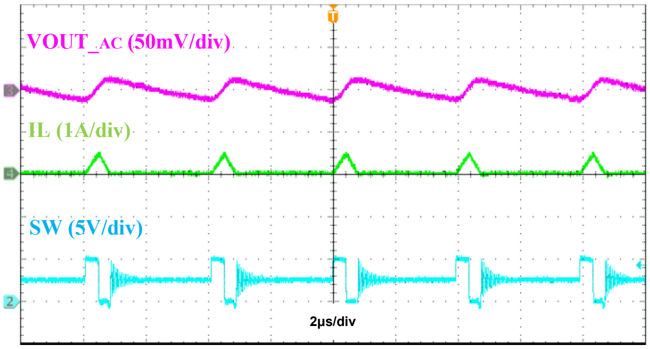


Figure 13. Output Voltage Ripple, IOUT = 50mA

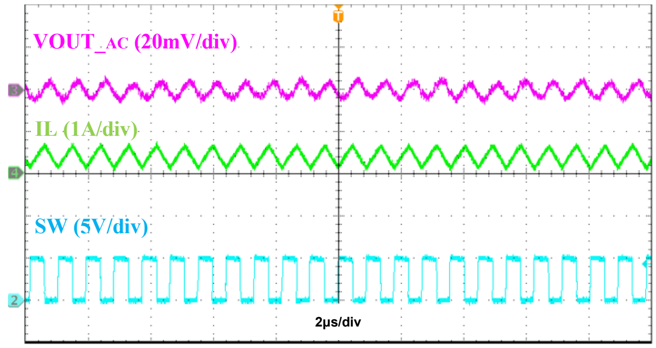


Figure 14. Output Voltage Ripple, IOUT = 0.4A

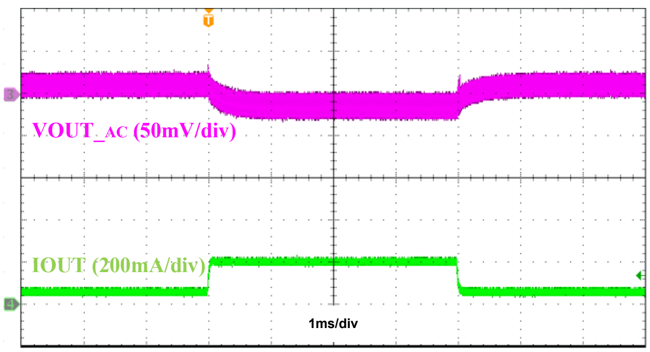


Figure 15. Load Transient, IOUT = 50mA to 200mA to 50mA

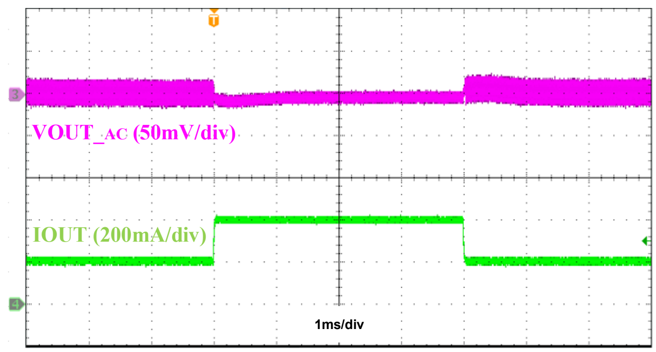


Figure 16. Load Transient, IOUT = 200mA to 400mA to 200mA

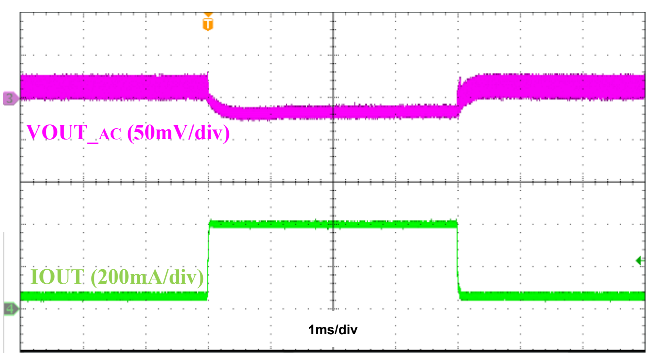


Figure 17. Load Transient, IOUT = 50mA to 400mA to 50mA

Typical Performance Characteristics (AP61040 @ TA = +25°C, VIN = 5V, VOUT = 2.5V, PWM, unless otherwise specified.) (continued)

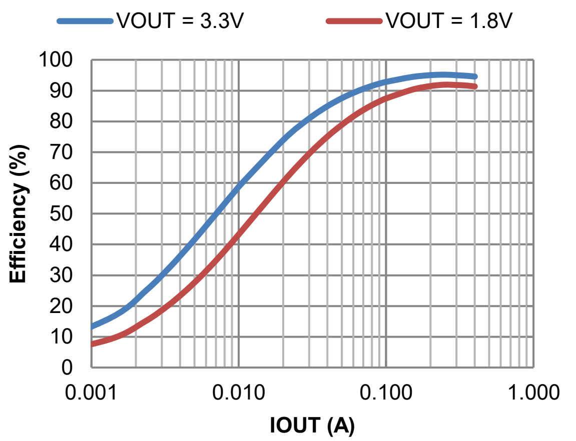


Figure 18. Efficiency vs. Output Current, VIN = 5V

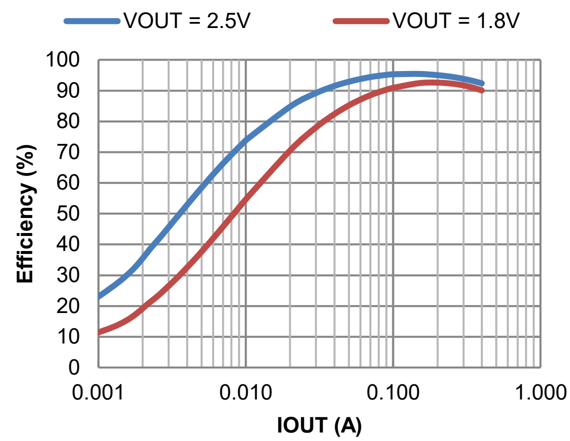


Figure 19. Efficiency vs. Output Current, VIN = 3.3V

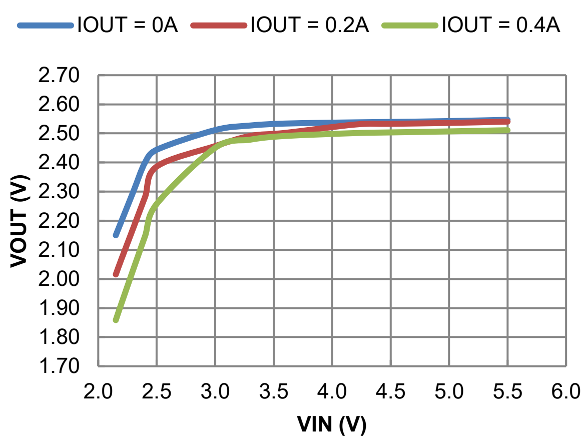


Figure 20. Line Regulation

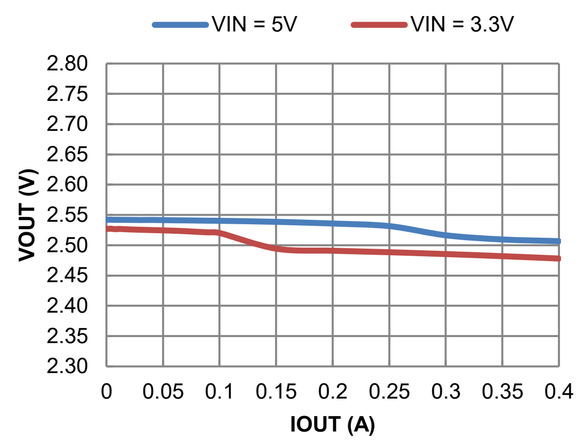


Figure 21. Load Regulation

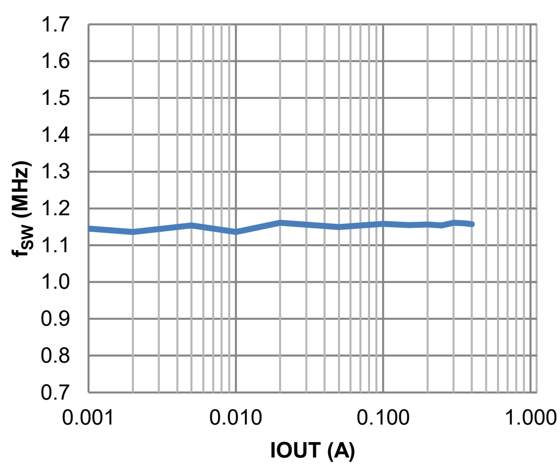


Figure 22. fsw vs. Load

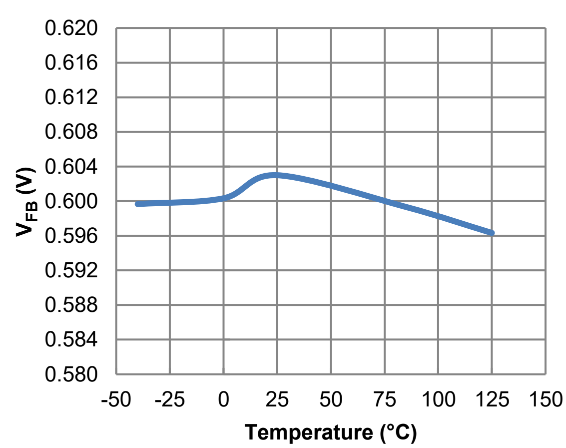


Figure 23. Feedback Voltage vs. Temperature

Typical Performance Characteristics (AP61040 @ TA = +25°C, VIN = 5V, VOUT = 2.5V, PWM, unless otherwise specified.) (continued)

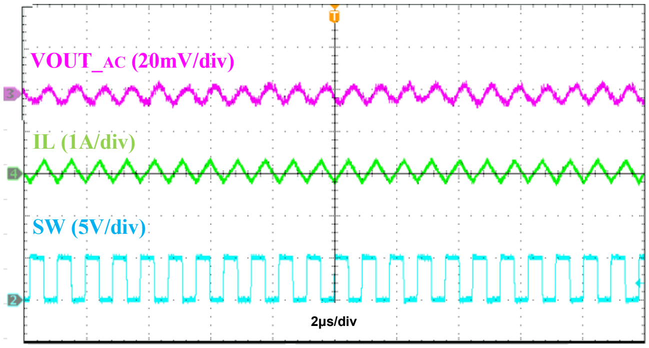


Figure 24. Output Voltage Ripple, IOUT = 50mA

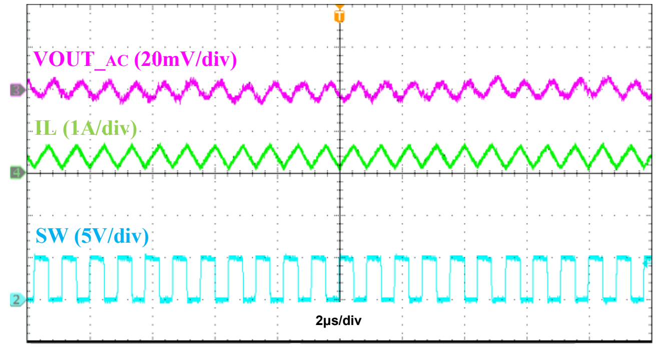


Figure 25. Output Voltage Ripple, IOUT = 0.4A

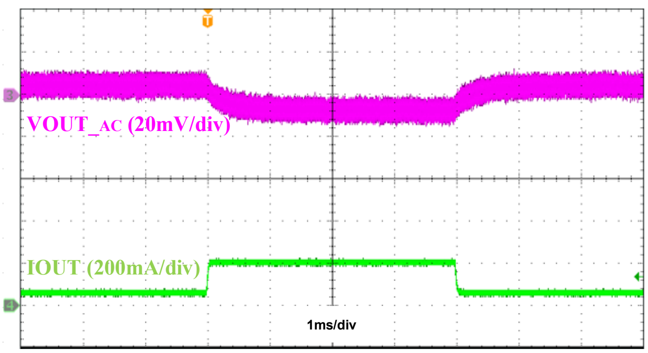


Figure 26. Load Transient, IOUT = 50mA to 200mA to 50mA

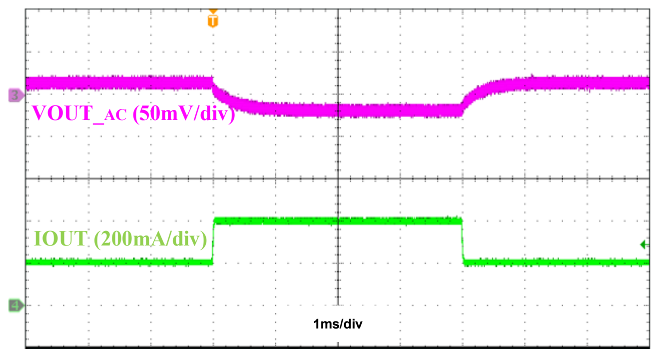


Figure 27. Load Transient, IOUT = 200mA to 400mA to 200mA

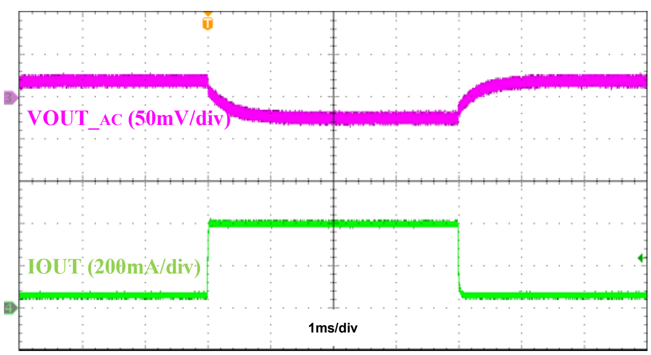


Figure 28. Load Transient, IOUT = 50mA to 400mA to 50mA

Typical Performance Characteristics (AP61040 @ TA = +25°C, VIN = 5V, VOUT = 2.5V, unless otherwise specified.) (continued)

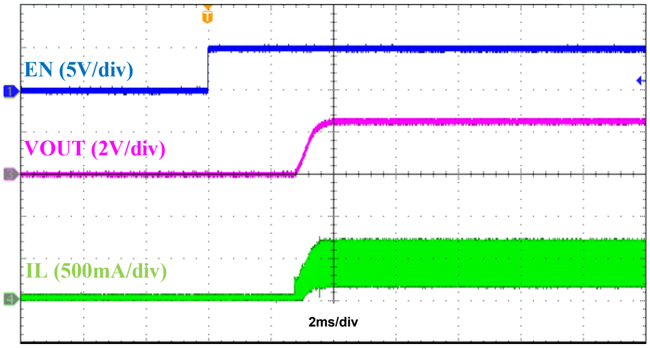


Figure 29. Startup Using EN, IOUT = 0.4A

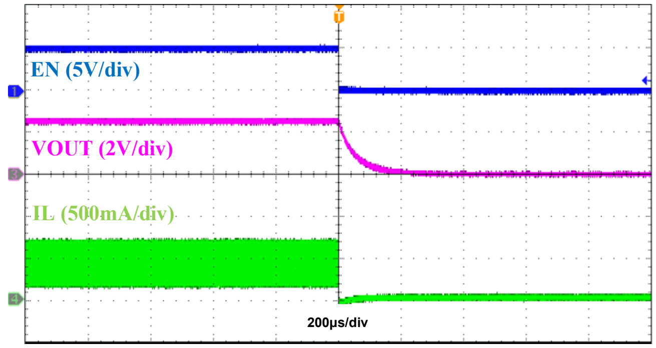


Figure 30. Shutdown Using EN, IOUT = 0.4A

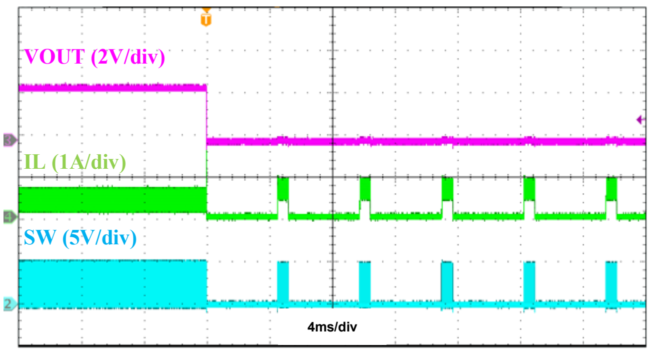


Figure 31. Output Short Protection, IOUT = 0.4A

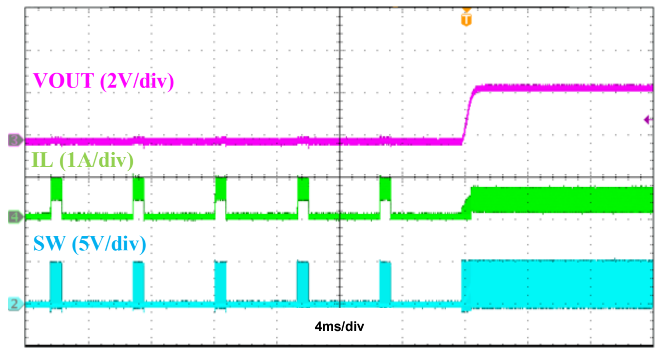


Figure 32. Output Short Protection, IOUT = 0.4A

Application Information

Theory of Operation

The AP61040 is a 400mA current mode control, synchronous buck regulator with integrated power MOSFETs. Current mode control assures excellent line regulation, load regulation, and a wide loop bandwidth for fast response to load transients. Figure 1 and 2 depict the typical application schematic and functional block diagram of the AP61040. The buck controller drives the internal HS PFET and LS NFET. The buck regulator can operate from an unregulated DC source, such as a battery, with a voltage ranging from 2.15V to 5.5V. The converter output can be regulated as low as 0.6V, to as high as 5.5V. There are preselected output voltages that are programmed by the pin VSEL1. See the output selection table for more details.

Enable Control

When disabled, the device shutdown supply current is only 0.1µA. When applying a voltage greater than the EN logic-high threshold (typical 0.91V, rising), the AP61040 enables all functions, and the device initiates the soft-start phase. The AP61040 has a built-in 0.8ms soft-start time to prevent output-voltage overshot and inrush current. When the EN voltage falls below its logic-low threshold (typical 0.83V, falling), the internal SS voltage discharges to ground and the device operation is disabled.

The AP61040 operates in PFM when a logic-high voltage greater than VIN – 200mV is applied to the EN pin. Tying the EN pin to the VIN pin is sufficient to achieve this threshold condition.

The device operates in PWM regardless of output load when a logic-high voltage less than VIN – 200mV is applied to the EN pin. Using an external resistive divider to create a difference in voltage between the VIN and EN pins is sufficient to achieve this threshold condition.

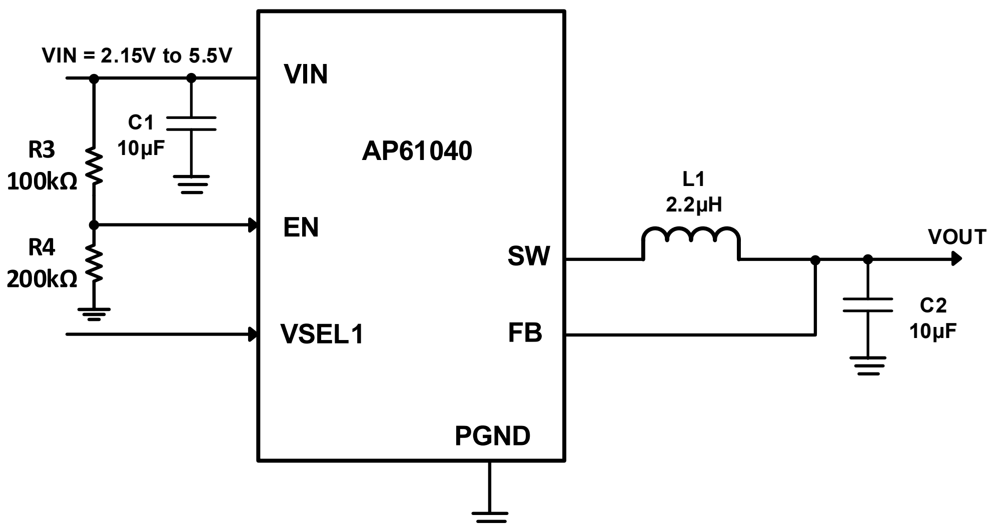


Figure 33. Example Application Circuit for Forced PWM Operation

Setting the Output Voltage

The output voltage can be adjusted from 0.6V using an external resistor divider. Table 1 shows a list of resistor selections for common output voltages. A CFF of 39pF must be added to improve the loop response and maintain output stability. Select R1 approximately 100kΩ, then R2 can be determined by the following equation:

$$R_2 = \frac{R_1(Vout - 0.6V)}{0.6}$$

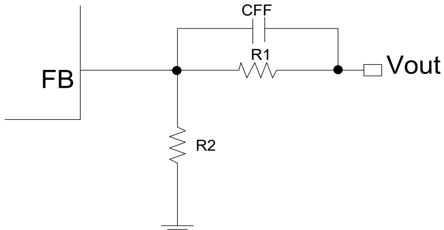


Figure 34. Feedback Divider Network

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	VSEL1	CFF (pF)	L1 (µH)
1.2	100	100	OPEN	39	2.2
1.5	150	100	OPEN	39	2.2
1.8	200	100	OPEN	39	2.2
2.5	316	100	OPEN	39	2.2
3.3	453	100	OPEN	39	2.2

Table 1 Recommended Component Selection

Application Information

Alternatively, the output voltage can be programmed via VSEL1. Table 2 shows the voltage selection settings. Connect FB directly to the output. The maximum transition time of VSEL1 and VSEL2 must be less than 100µs to avoid an undefined voltage state.

V_{FB} (V)	VSEL1	L1 (µH)
0.6	OPEN	2.2
2.5	0	2.2
3.3	1	2.2

Table 2 VSEL1 Selection

Overcurrent Protection

The AP61040 detects the current limit on the high side, Q1, to protect the device against overload or short-circuit conditions. The peak current in the switch is monitored cycle-by-cycle with a comparator delay of approximately 100ns to guard against noise glitches. If the high-side Q1 current limit is reached, the high-side Q1 is turned off and the low-side Q2 is turned on until the switch current decreases below the OC threshold. The frequency is reduced to protect the device from damage. The Q1 peak current limit remains active during this state. After 17 consecutive cycles in this OCP event, the regulator enters hiccup mode where all power FETs are turned off and will wait for 15ms before attempting to restart.

Reverse Current Protection

During fixed frequency operation, a reverse-current comparator on switch Q2 monitors the current entering VOUT. When this current exceeds 400mA (typical), switch Q2 will be turned off for the remainder of the switching cycle. This feature protects the buck converter from excessive reverse current if the buck output is held above the regulation voltage by an external source.

Undervoltage Lockout

The undervoltage lockout (UVLO) feature prevents abnormal operation if the supply voltage is too low to guarantee proper operation. When the VIN voltage falls below the UVLO threshold, the regulator is disabled.

Thermal Shutdown

A built-in thermal protection feature protects the AP61040 if the die temperature reaches +150°C (typical). At this die temperature, the regulator is completely shut down. The die temperature continues to be monitored in this thermal-shutdown mode. When the die temperature falls to +125°C (typical), the device will resume normal operation. When exiting thermal shutdown, the AP61040 will execute its soft-start sequence.

Output Active Discharge

The buck provides an internal 50Ω resistor for output active discharge function. The internal resistor discharges the energy stored in the output capacitor to PGND whenever the regulator is disabled. When the regulator remains enabled, the internal resistor is disconnected from the output.

Inductor Selection

An inductor with a high-frequency core material (e.g., ferrite core) should be used to minimize core losses and provide good efficiency. The inductor must be able to handle the peak switching currents without saturating. A 2.2µH inductor with a ≥600mA saturation current rating is recommended. Select an inductor with a low DCR to provide good efficiency. In applications where radiated noise must be minimized, a toroidal or shielded inductor can be used.

VIN and VOUT Capacitor Selection

The input and output capacitors should be a ceramic X5R type with low ESL and ESR. The recommended input capacitor value is 10µF, as this would provide adequate RMS current to minimize the input voltage ripple. A minimum of 10µF is required to maintain full functionality of the part. The recommended output capacitor is 10µF, 10V, X5R. Note that the effective value of a ceramic capacitor derates with DC voltage bias across it. This decreasing may be up to 70% of the rated capacitance. Refer to the capacitor datasheet to ensure the combined effective output capacitance is at least 30µF for proper operation over the entire recommended load current range. Low output capacitance may lead to a large output voltage drop during load transients or unstable operation.

Application Information

PC Board Layout

The AP61040 works at a 400mA load current. A 2oz copper in both the top and bottom layer is recommended. Correct PCB layout is critical for proper operation of the AP61040. The following are some general guidelines for the recommended layout:

1. The input and output capacitors should be positioned directly across VIN-PGND and as close to the IC as possible to ensure noise-free operation.
2. The ground connections of the input and output capacitors should be kept as short as possible. The objective is to minimize the current loop between the ground pads of the input and output capacitors and the PGND pins of the IC. Use via, if required, to take advantage of a PCB ground layer underneath the regulator.
3. Fill the second layer with PGND. The single point connects the GND to the second layer's PGND.
4. Minimize the trace lengths on the feedback loop to avoid switching noise pick-up. Via should be avoided on the feedback loop to minimize the effect of board parasitic, particularly during load transients.
5. The SW trace should be short.
6. See figure 35 below for more details on the recommended layout.

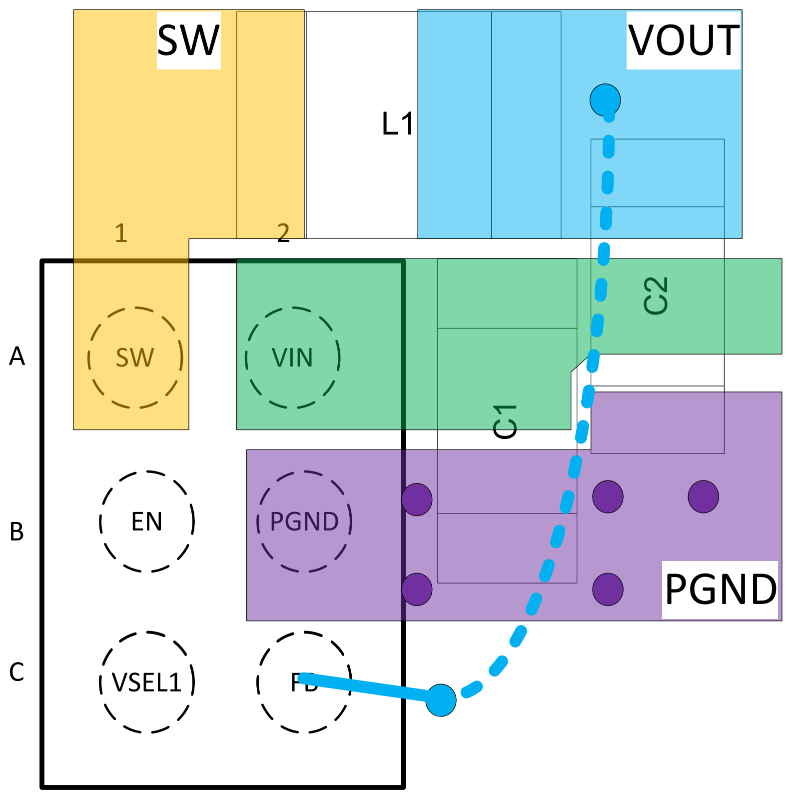
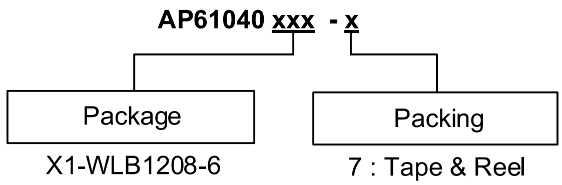


Figure 35. Recommended Layout Design

Ordering Information

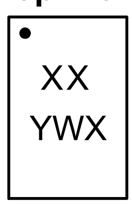


Orderable Part Number	Package	Package Code	Packing		
			Quantity	Carrier	Part Number Suffix
AP61040CP6-7	X1-WLB1208-6	CP6	3,000	Tape and Reel	-7

Marking Information

X1-WLB1208-6

(Top View)



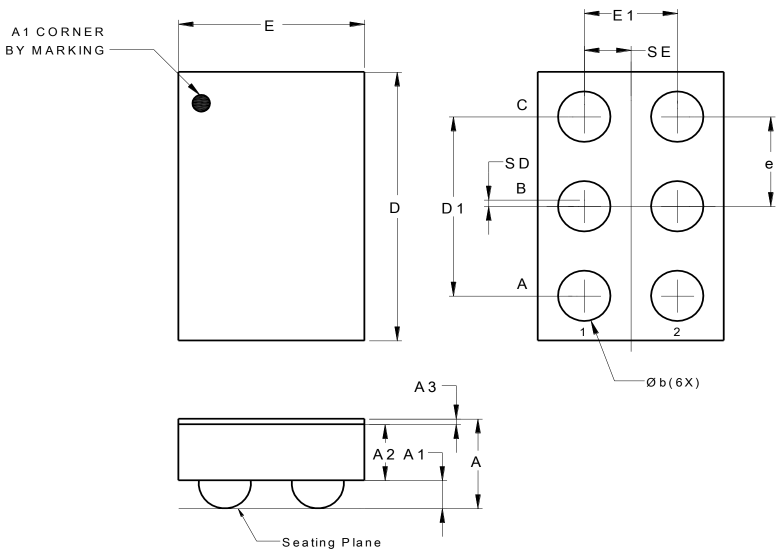
XX : Identification Code
Y : Year : 0~9
W : Week : A~Z : 1~26 week;
a~z: 27~52 week; z represents 52 and 53 week
X : Internal Code

Orderable Part Number	Package	Identification Code
AP61040CP6-7	X1-WLB1208-6	KB

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

X1-WLB1208-6

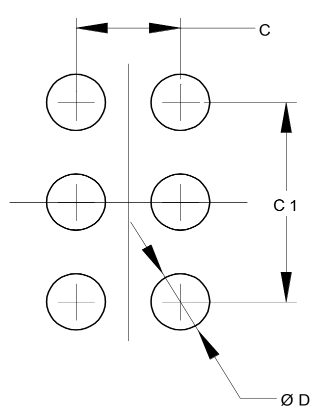


X1-WLB1208-6			
Dim	**Min**	**Max**	**Typ**
A	0.400	0.500	0.450
A1	0.155	0.195	0.175
A2	0.225	0.275	0.250
A3	0.020	0.030	0.025
b	0.200	0.260	0.230
D	1.160	1.220	1.190
D1	0.770	0.830	0.800
E	0.760	0.820	0.790
E1	0.370	0.430	0.400
e	0.400 BSC		
SD	0.000 BSC		
SE	0.200 BSC		
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

X1-WLB1208-6



Dimensions	Value (in mm)
C	0.400
C1	0.800
D	0.250

Mechanical Data

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads, Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.7 mg (Approximate)

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