ALM1412

µASIC
Programmable Mixed-Signal IC

Description

The ALM1412 is an ultra-small programmable µASIC featuring LUTs, Logic Macrocells, Timers, Oscillators, ACMPs, VREF, and more. Each Macrocell within the ALM1412 contains multiple configurable settings and initial states for maximum flexibility.

The ALM1412's Macrocells are connected via hardware-defined matrix connections, not abstracted firmware. This enables asynchronous design at low power, as well as more reliable operation compared to microcontrollers. Unlike a fixed ASIC, the timing and event sequences can be updated with a programming code change.

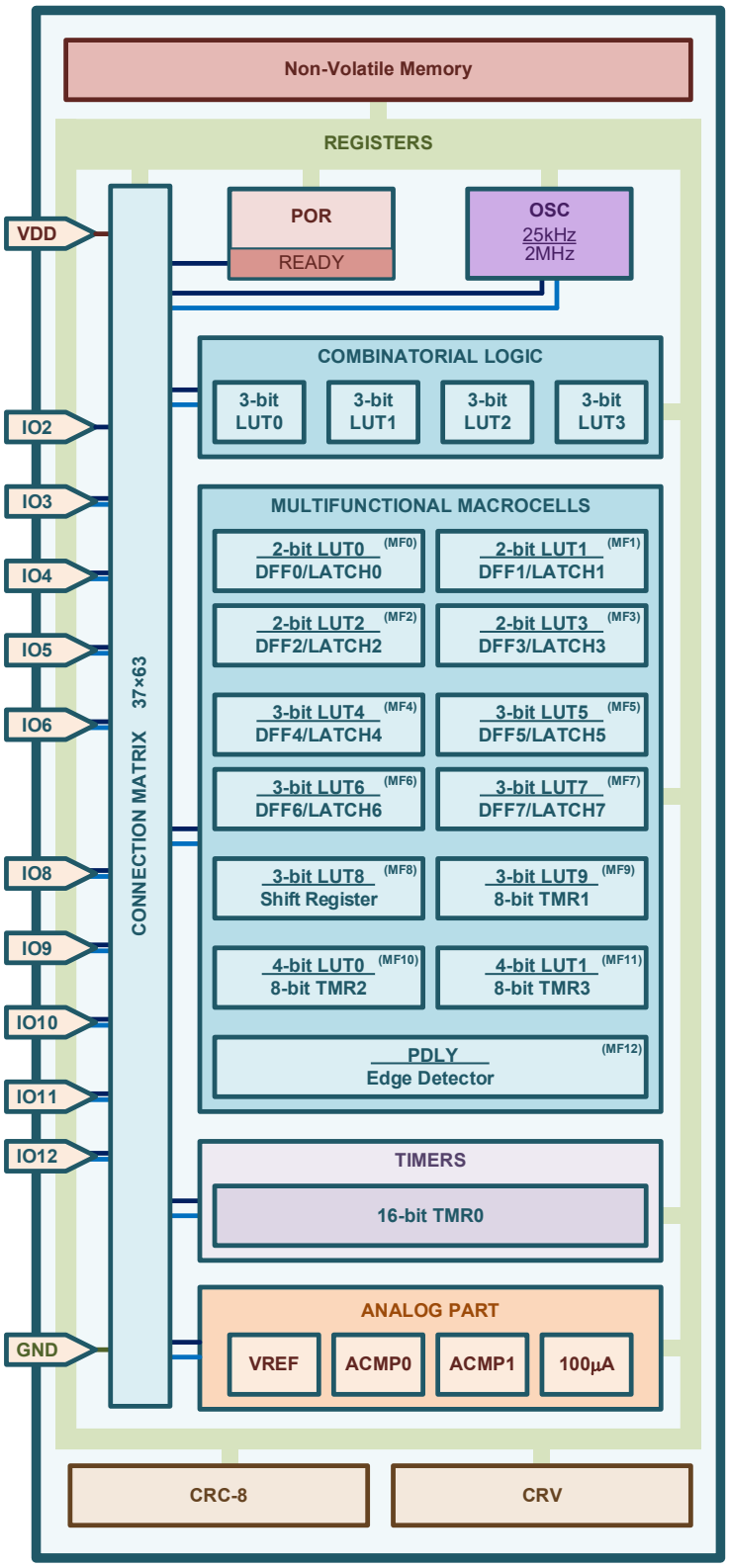
The ALM1412's functional reliability is enhanced by CRC-8 and Continuous Register Verification (CRV).

Features

- 1.71V to 5.50V Supply (V_{DD})
- Operating Temperature Range: -40°C to 85°C
- RoHS Compliant/Halogen-Free/Pb-Free
- Two Analog Comparators (ACMP)
- Voltage Reference (VREF)
- 100µA Current Source
- Four Combinatorial Logic Macrocells
- Thirteen Multifunctional Macrocells
  - Four Selectable 2-bit LUTs or DFF/LATCHs
  - Four Selectable 3-bit LUTs or DFF/LATCHs
  - One Selectable 3-bit LUT or 16-bit Shift Register
  - One Selectable 3-bit LUTs or 8-bit Timers (TMR)
  - Two Selectable 4-bit LUTs or 8-bit Timers
  - One Programmable Delay or Edge Detector
- One 16-bit Timer
- One Oscillator (OSC)
- Power On Reset (POR)
- Data Protection Feature
  - CRC-8
  - Continuous Registers Verification (CRV)
- Package Options
  - X1-QFN1616-12 (Type AX)
  - (1.6×1.6×0.42 mm, 0.4 mm pitch)
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green " Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.**
  https://www.diodes.com/quality/product-definitions/

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Architecture Block Diagram



The ALM1412 (Figure 1, Table 1) has 10 multi-function IO pins which can function as a user-defined Input or Output. Refer to Table 1 for pin definitions. Of the 10 user-defined IO pins on the ALM1412, the pins can serve as Digital Input and Digital Output. IO2 can only serve as a Digital Input. IO3, IO4, IO6, and IO10 can also serve as Analog Input/Output.

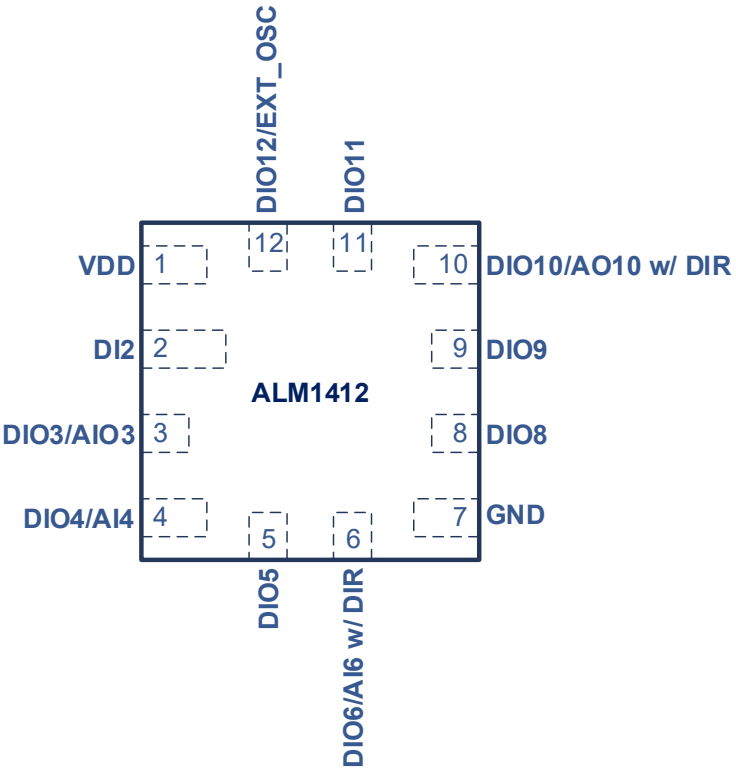


Figure 1. Top View (X1-QFN1616-12 (Type AX))

Table 1 Functional PIN Description

PIN # X1-QFN1616-12 (Type AX)	PIN Name	Signal Name	Function	Input Options	Output Options
1	VDD	VDD	Power Supply	--	--
2	IO2	DI2	Digital Input	Digital Input w/o Schmitt Trigger Digital Input w/ Schmitt Trigger Digital Input Low Voltage	--
3	IO3	DIO3	Digital IO	Digital Input w/o Schmitt Trigger Digital Input w/ Schmitt Trigger Digital Input Low Voltage	Push-Pull ×1 Push-Pull ×2 Open Drain NMOS ×1 Open Drain NMOS ×2 Open Drain PMOS ×1 Open Drain PMOS ×2
		AIO3	Analog Comparator 0 Positive Input (ACMP0+) 100µA Current Source	Analog	Analog
4	IO4	DIO4	Digital IO	Digital Input w/o Schmitt Trigger Digital Input w/ Schmitt Trigger Digital Input Low Voltage	Push-Pull ×1 Push-Pull ×2 Open Drain NMOS ×1 Open Drain NMOS ×2 Open Drain PMOS ×1 Open Drain PMOS ×2
		AI4	Analog Comparator 0/1 Negative Input (ACMP0/1-)	Analog	--
5	IO5	DIO5	Digital IO	Digital Input w/o Schmitt Trigger Digital Input w/ Schmitt Trigger Digital Input Low Voltage	Push-Pull ×1 Push-Pull ×2 Open Drain NMOS ×1 Open Drain NMOS ×2 Open Drain PMOS ×1 Open Drain PMOS ×2
6	IO6	DIO6	Digital IO	Digital Input w/o Schmitt Trigger Digital Input w/ Schmitt Trigger Digital Input Low Voltage	Push-Pull ×1 Push-Pull ×2 Open Drain NMOS ×1 Open Drain NMOS ×2 Open Drain PMOS ×1 Open Drain PMOS ×2
		AI6	Analog Comparator 1 Positive Input (ACMP1+)	Analog	--
7	GND	GND	Ground	--	--
8	IO8	DIO8	Digital IO	Digital Input w/o Schmitt Trigger Digital Input w/ Schmitt Trigger Digital Input Low Voltage	Push-Pull ×1 Push-Pull ×2 Open Drain NMOS ×1 Open Drain NMOS ×2 Open Drain PMOS ×1 Open Drain PMOS ×2
9	IO9	DIO9	Digital IO	Digital Input w/o Schmitt Trigger Digital Input w/ Schmitt Trigger Digital Input Low Voltage	Push-Pull ×1 Push-Pull ×2 Open Drain NMOS ×1 Open Drain NMOS ×2 Open Drain PMOS ×1 Open Drain PMOS ×2
10	IO10	DIO10	Digital IO	Digital Input w/o Schmitt Trigger Digital Input w/ Schmitt Trigger Digital Input Low Voltage	Push-Pull ×1 Push-Pull ×2 Open Drain NMOS ×1 Open Drain NMOS ×2 Open Drain PMOS ×1 Open Drain PMOS ×2
		AO10	Voltage Reference Output (VREF_OUT)	--	Analog
11	IO11	DIO11	Digital IO	Digital Input w/o Schmitt Trigger Digital Input w/ Schmitt Trigger Digital Input Low Voltage	Push-Pull ×1 Push-Pull ×2 Open Drain NMOS ×1 Open Drain NMOS ×2 Open Drain PMOS ×1 Open Drain PMOS ×2

PIN # X1-QFN1616-12 (Type AX)	PIN Name	Signal Name	Function	Input Options	Output Options
12	IO12	DIO12	Digital IO	Digital Input w/o Schmitt Trigger Digital Input w/ Schmitt Trigger Digital Input Low Voltage	Push-Pull ×1 Push-Pull ×2 Open Drain NMOS ×1 Open Drain NMOS ×2 Open Drain PMOS ×1 Open Drain PMOS ×2
		EXT_OSC_IN	External CLK of OSC Connection	Digital Input w/o Schmitt Trigger Digital Input w/ Schmitt Trigger Digital Input Low Voltage	--

Macrocell Manifest

Macrocell Name	Description	Number of Units	Total Units	Referenced Section
IOs			**10**	**5**
Digital Input	• Digital Input (low or normal voltage; with or without a Schmitt Trigger) • 10kΩ/100kΩ/1MΩ Pull-Up/Pull-Down resistors	• One Digital Input	1	5.4, 5.11.1
Digital Input/Output	• Digital Input (low or normal voltage; with or without a Schmitt Trigger) • Open Drain Outputs: NMOS ×1(2), PMOS ×1(2) • Push Pull Outputs: PP ×1(2) • 10kΩ/100kΩ/1MΩ Pull-Up/Pull-Down resistors	• Eleven Digital IOs	9	5.5, 5.6, 5.7, 5.8, 5.9, 5.10, 5.11.2, 5.11.3, 5.11.4, 5.11.5, 5.11.6, 5.11.7, 5.11.8, 5.11.9, 5.11.10
Analog Input	• Analog Input	• Two Analog Inputs	2	5.6, 5.8, 5.11.3, 5.11.5
Analog Output	• Analog Output	• One Analog Output	1	5.9, 5.11.8
Analog Input/Output	• Analog Input/Output	• One Analog Input/Outputs	1	5.5, 5.11.2
Connection Matrix			**1**	**6**
Connection Matrix	• Digital matrix connections	• Size 37×63	1	6.1, 6.2, 6.3
Combinatorial Logic Macrocells			**16**	**7, 8**
2-bit LUT	• 2-bit Look-Up Table	• Four 2-bit LUTs shared with DFF/LATCH w/o RST	4	8.1
3-bit LUT	• 3-bit Look-Up Table	• Four 3-bit LUTs • Four 3-bit LUTs shared with DFF/LATCH w/ RST • One 3-bit LUT shared with Shift Register • One 3-bit LUT shared with 8-bit Timers	10	7.1, 8.2, 8.3, 8.4
4-bit LUT	• 4-bit Look-Up Table	• Two 4-bit LUTs shared with 8-bit timers	2	8.5
Sequential Logic Macrocells			**24**	**8, 9**
DFF w/o RST	• D Flip-Flop w/o RST	• Four DFFs shared with 2-bit LUTs or LATCHs w/o RST	4	8.1
LATCH w/o RST	• LATCH w/o RST	• Four LATCHs shared with 2-bit LUTs or DFFs w/o RST	4	8.1
DFF w/ RST	• D Flip-Flop w/ RST	• Four DFFs shared with 3-bit LUTs or LATCHs w/ RST	4	8.2
LATCH w/ RST	• LATCH w/ RST	• Four LATCHs shared with 3-bit LUTs or DFFs w/ RST	4	8.2
Shift Register	• 16 stages/3 outputs • Two outputs of 1st to 16th selectable stages • One output of 1st stage	• One Shift Register shared with 3-bit LUT	1	8.3
8-bit TMR	• 8-bit Timer	• One 8-bit TMRs shared with 3-bit LUTs • Two 8-bit TMRs shared with 4-bit LUTs	3	8.4, 8.5
16-bit TMR	• 16-bit Timer	• One 16-bit TMRs	1	9.1
WS	• Wake&Sleep Control	• One WS (Wake&Sleep mode of 16-bit TMR)	1	9.1.1
PDLY	• Programmable Delay • 140 ns/280 ns/420 ns/560 ns @ VDD = 3.30V	• One PDLY shared with Edge Detector	1	8.6
Edge Detector	• Rising Edge Detector • Falling Edge Detector • Both Edge Detector	• One Edge Detector shared with PDLY	1	8.6
Data Protection			**2**	**11**
CRC-8	• Cyclic redundancy check of NVM content	• $x^8 + x^6 + x^3 + 1$	1	11.1
CRV	• Continuous Registers Verification	• 32 bits of CRV	1	11.2
Oscillators			**1**	**15**
25kHz 2MHz	• 25 kHz or 2 MHz selectable frequency • Main prescaler: OSC/1, OSC/2, OSC/4, and OSC/8 • Two clock outputs with selectable PRESCALER_OUT: 1(OUT0), 1/2(OUT1), 1/4, 1/8, 1/16, 1/32, 1/64, 1/128(OUT0) or 1/256(OUT1)	• One OSC (25kHz/2MHz)	1	15
Analog Part			**4**	**12, 13, 14**
Analog Comparator	• Selectable Hysteresis 0 mV, 25 mV, Custom Hysteresis • Wake and Sleep Control (Part of Multifunctional macrocell)	• Two ACMPs	2	12, 9.1.1

Macrocell Name	Description	Number of Units	Total Units	Referenced Section
100µA Current Source	• Enabled Current Sourced connected to IO3 pad	• One 100µA Current Source	1	4.10, 14
Voltage Reference	• Used as Analog Comparators references • Can be route to external pin	• One VREF	1	13
POR			**1**	**16**
IO2 Reset	• Reset by events of IO2		1	16.4

Contents

1. Application Examples

The ALM1412 is a programable mixed-signal IC, which can be configured and used for a wide array of applications. Below, you can find four simple use-cases for the ALM1412.

Example 1.1: Power sequencer (~23% of blocks are used)

Most of the complex electronic systems have definite power-supply controls to ensure that every part of the system starts up properly. This example (Figure 1.2) shows the implementation of such a system based on the ALM1412. IN rising event runs the two-channel start-up power-supply sequence, and the IN falling event runs the power-down sequence (Figure 1.1).

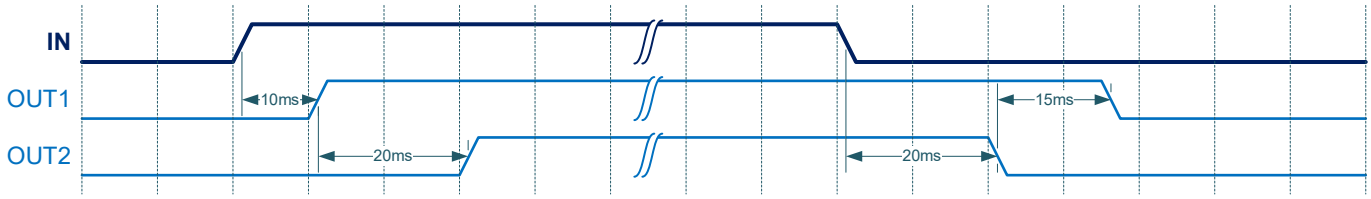


Figure 1.1. Power Sequencer requirements

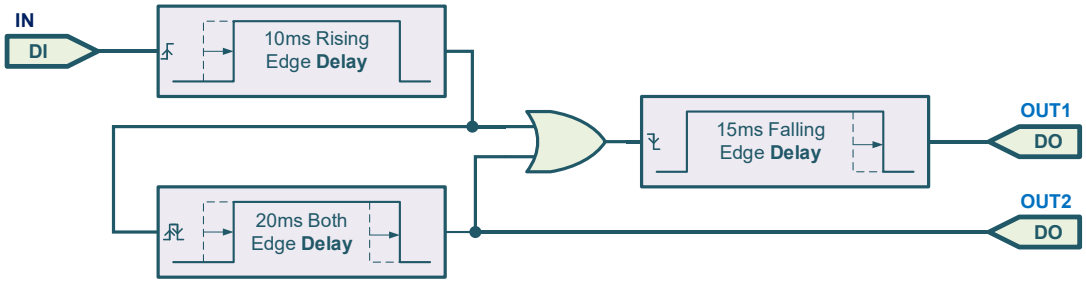


Figure 1.2. Power Sequencer implementation

Example 1.2 Watchdog timer (~18% of blocks are used)

The ALM1412 allows the user to implement a watchdog timer (Figure 1.4). If the device does not detect either the rising or falling edge of the IN signal during 100ms, it generates a 500ms LOW pulse (Figure 1.3).

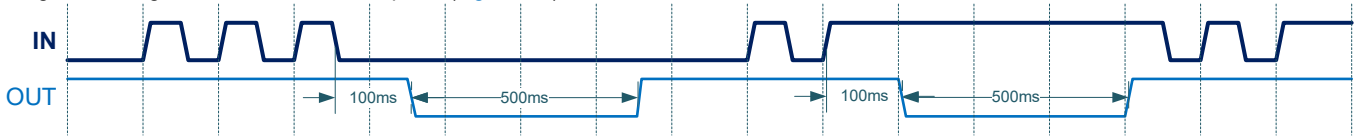


Figure 1.3. Watchdog requirements

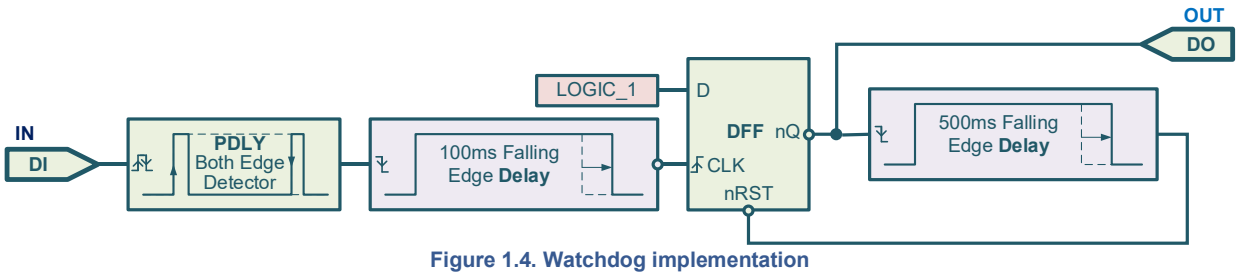


Figure 1.4. Watchdog implementation

Example 1.3 Sawtooth-waveform generator (~15% of blocks are used)

The current application example shows the user how to use the analog part of the ALM1412. The design can generate sawtooth waveform (Figure 1.5). There is a possibility to set the value of the high (VREFH) and low (VREFL) levels of the generated signal with a user-setting hysteresis for the ACMP0 (Figure 1.6). The period (T) of signal is determined by the capacitance value (C). The design uses 100µA Current Source, which is directly connected to the pad of the IO3. The positive input of the ACMP0 is also connected to the IO3. At the same time, the IO3 is configured as a digital output with open drain (NMOS). The capacitor voltage increases with this current. When the voltage reaches the VREFH level, the ACMP0 switches its output to HIGH. Therefore, the NMOS of the IO3 is ON and discharges the capacitor (C). After reaching VREFL level, the ACMP0 switches its output to LOW. Consequently, the IO3 is in HIGH-Z, and the capacitor voltage begins increasing. This cycle repeats (see Figure 1.6).

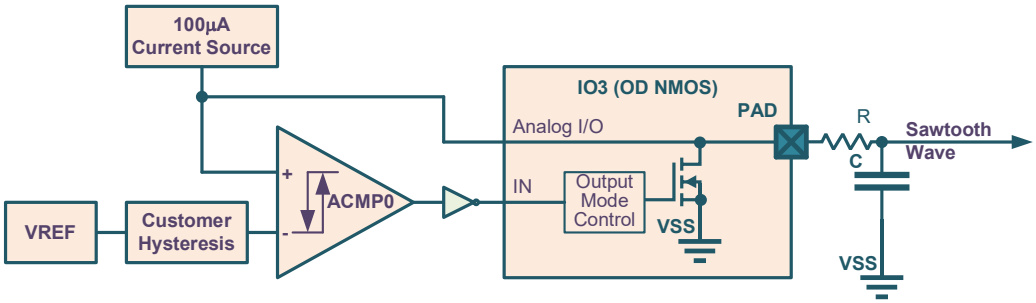


Figure 1.5. Sawtooth-waveform generator

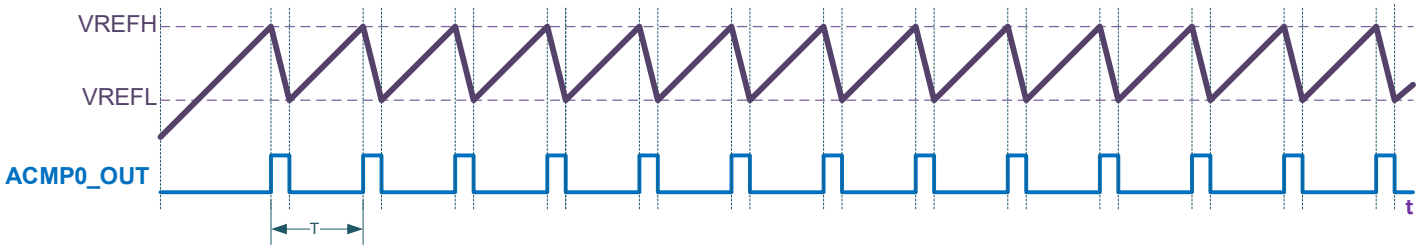


Figure 1.6. Timing diagrams of sawtooth-waveform generator

2. How to Get Samples and Go to Production

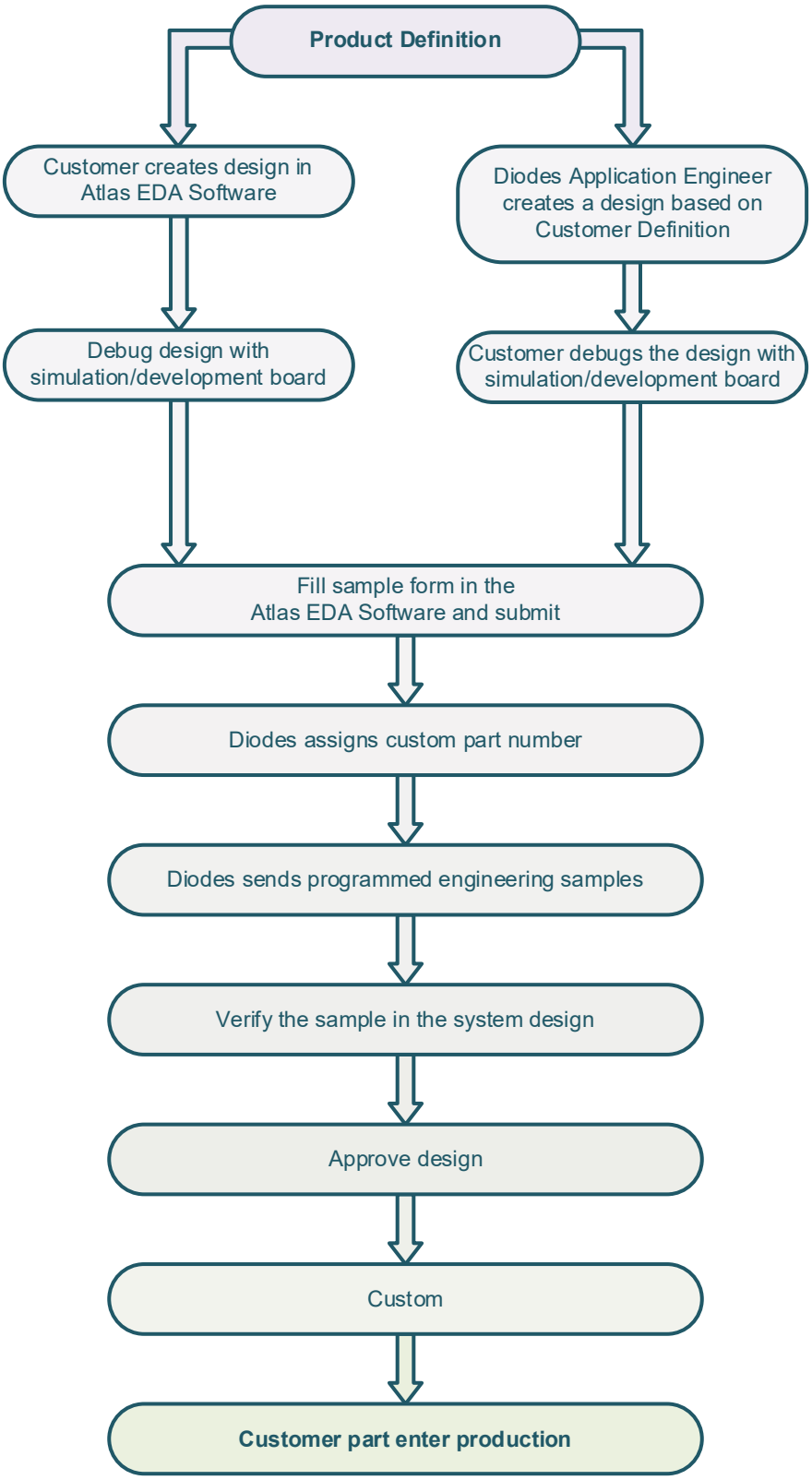


Figure 2.1. Stages of development in a custom µASIC device

3. Ordering Information

3.1. Ordering Information for Custom Programmed Part

Part Number	Package	Packing	
		Qty.	Carrier
ALMxxxxxx	X1-QFN1616-12 (Type AX)	3,000	7” Tape and Reel

The custom program part number is created when design is submitted.

4. Electrical Specifications

4.1. Absolute Maximum Conditions

Table 4.1. Absolute Maximum Conditions

Parameter		Min	Max	Unit
Supply voltage on VDD relative to GND		-0.5	7	V
DC Input voltage		GND - 0.5	V_{DD} + 0.5	V
Maximum Average or DC Current Through VDD PIN			100	mA
Maximum Average or DC Current Through GND PIN (Per chip side, see Note 4.1)			100	mA
Maximum Average or DC Current (Through pin)	PP×1	--	18	mA
	PP×2	--	28	
	OD(NMOS)×1	--	18	
	OD(NMOS)×2	--	28	
	OD(PMOS)×1	--	18	
	OD(PMOS)×2	--	28	
Current at Input PIN (Note 4.2)		-10.0	10.0	mA
Input leakage (Absolute Value)		--	10	nA
Storage Temperature Range		-65	150	°C
Junction Temperature		--	150	°C
ESD Protection (Human Body Model)		4000	--	V
ESD Protection (Charged Device Model)		1000	--	V
Moisture Sensitivity Level		1		

Note 4.1 *The power rails are divided in two sides. IOs 2, 3, 4, 5, and 6 are connected to one side, IOs 8, 9, 10, 11 and 12 to another*

Note 4.2 *Limiting input pin current is only necessary for input voltages that exceed absolute maximum input voltage ratings*

4.2. Recommended Operating Conditions

Table 4.2. Recommended Operating Conditions

Symbol	Parameter	Condition/Note	Min	Typ	Max	Unit
V_{DD}	Supply Voltage		1.71	3.30	5.50	V
T_A	Operating Temperature		-40	25	85	°C
V_O	Operating Voltage Applied to any PIN in HIGH-Impedance State		GND – 0.3	--	V_{DD}+0.3	V
C_{VDD}	Capacitor Value at VDD		--	0.1	--	µF

4.3. General Specifications

Table 4.3. General characteristics

Symbol	Parameter	Condition/Note	Min	Typ	Max	Unit
T_{SU}	Startup Time	From V_{DD} rising past PON_{THR}	--	0.34	0.60	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.42	1.54	1.66	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	1.21	1.39	1.52	V

4.4. IO Specifications

Table 4.4. IO Electrical Characteristics

@ V_{DD} = 1.71V to 5.50V, T = - 40 °C to +85 °C Unless Otherwise Noted

Symbol	Parameter	Condition/Note	Min	Typ	Max	Unit
V_{IH}	HIGH-Level Input Voltage	Logic Input (Note 4.3)	0.7xV_{DD}	--	V_{DD}+0.3	V
		Logic Input with Schmitt Trigger	0.8xV_{DD}	--	V_{DD}+0.3	V
		LOW-Level Logic Input (Note 4.3)	1.25	--	V_{DD}+0.3	V
V_{IL}	LOW-Level Input Voltage	Logic Input (Note 4.3)	GND-0.3	--	0.3xV_{DD}	V
		Logic Input with Schmitt Trigger	GND-0.3	--	0.2xV_{DD}	V
		LOW-Level Logic Input (Note 4.3)	GND-0.3	--	0.4	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage	Logic Input with Schmitt Trigger	--	0.5	--	V
V_{OH}	HIGH-Level Output Voltage	Push-Pull ×1, Open Drain PMOS ×1, I_{OH} = -100 µA, V_{DD} = 1.8 V	1.791	1.795	--	V
		Push-Pull ×2, Open Drain PMOS ×2, I_{OH} = -100 µA, V_{DD} = 1.8 V	1.794	1.798	--	V
		Push-Pull ×1, Open Drain PMOS ×1, I_{OH} = -3 mA, V_{DD} = 3.3 V	3.198	3.220	--	V
		Push-Pull ×2, Open Drain PMOS ×2, I_{OH} = -3 mA, V_{DD} = 3.3 V	3.247	3.259	--	V
		Push-Pull ×1, Open Drain PMOS ×1, I_{OH} = -5 mA, V_{DD} = 5.0 V	4.830	4.901	--	V
		Push-Pull ×2, Open Drain PMOS ×2, I_{OH} = -5 mA, V_{DD} = 5.0 V	4.936	4.949	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull ×1, Open Drain NMOS ×1, I_{OL} = 100 µA, V_{DD} = 1.8 V	--	0.0028	0.0035	V
		Push-Pull ×2, Open Drain NMOS ×2, I_{OL} = 100 µA, V_{DD} = 1.8 V	--	0.0012	0.0018	V
		Push-Pull ×1, Open Drain NMOS ×1, I_{OL} = 3 mA, V_{DD} = 3.3 V	--	0.0448	0.0559	V
		Push-Pull ×2, Open Drain NMOS ×2, I_{OL} = 3 mA, V_{DD} = 3.3 V	--	0.0230	0.0300	V
		Push-Pull ×1, Open Drain NMOS ×1, I_{OL} = 5 mA, V_{DD} = 5.0 V	--	0.0560	0.0715	V
		Push-Pull ×2, Open Drain NMOS ×2, I_{OL} = 5 mA, V_{DD} = 5.0 V	--	0.0294	0.0371	V
I_{OH}	HIGH-Level Output Current (see Note 4.4)	Push-Pull ×1, Open Drain PMOS ×1, V_{OH} = VDD - 0.2, V_{DD} = 1.8 V	-2.581	-3.180	--	mA
		Push-Pull ×2, Open Drain PMOS ×2, V_{OH} = VDD - 0.2, V_{DD} = 1.8 V	-5.176	-6.280	--	mA
		Push-Pull ×1, Open Drain PMOS ×1, V_{OH} = 2.4, V_{DD} = 3.3 V	-19.406	-24.190	--	mA
		Push-Pull ×2, Open Drain PMOS ×2, V_{OH} = 2.4, V_{DD} = 3.3 V	-38.128	-47.600	--	mA
		Push-Pull ×1, Open Drain PMOS ×1, V_{OH} = 2.4, V_{DD} = 5.0 V	-57.080	-65.830	--	mA
		Push-Pull ×2, Open Drain PMOS ×2, V_{OH} = 2.4, V_{DD} = 5.0 V	-99.500	-124.352	--	mA
I_{OL}	LOW-Level Output Current (see Note 4.4)	Push-Pull ×1, Open Drain NMOS ×1, V_{OL} = 0.15 V, V_{DD} = 1.8 V	3.736	4.558	--	mA
		Push-Pull ×2, Open Drain NMOS ×2, V_{OL} = 0.15 V, V_{DD} = 1.8 V	7.286	9.150	--	mA
		Push-Pull ×1, Open Drain NMOS ×1, V_{OL} = 0.40 V, V_{DD} = 3.3 V	19.093	24.054	--	mA
		Push-Pull ×2, Open Drain NMOS ×2, V_{OL} = 0.40 V, V_{DD} = 3.3 V	37.405	46.801	--	mA
		Push-Pull ×1, Open Drain NMOS ×1, V_{OL} = 0.40 V, V_{DD} = 5.0 V	26.671	33.410	--	mA
		Push-Pull ×2, Open Drain NMOS ×2, V_{OL} = 0.40 V, V_{DD} = 5.0 V	51.805	65.700	--	mA
R_{PULL}	Pull-Up or Pull-Down Resistance	1000 kΩ; For Pull-Up V_{IN} = GND; For Pull-Down V_{IN} = V_{DD}	--	1000	--	kΩ
		100 kΩ; For Pull-Up V_{IN} = GND; For Pull-Down V_{IN} = V_{DD}	--	100	--	kΩ
		10 kΩ; For Pull-Up V_{IN} = GND; For Pull-Down V_{IN} = V_{DD}	--	10	--	kΩ
C_{IN}	Input Capacitance		--	4	10	pF

Symbol	Parameter	Condition/Note	Min	Typ	Max	Unit
Note 4.3	*No hysteresis*					
Note 4.4	*DC or average current through any pin should not exceed value given in Absolute Maximum Conditions*					

4.5. Typical Current Consumption

Table 4.5. Typical Current Consumption for Each Macrocell

Symbol	Parameter	Note	VDD = 1.8 V	VDD = 3.3 V	VDD = 5.0 V	Unit
I_{DD}	Current	Chip Quiescent	0.40	0.50	0.60	µA
		OSC 2 MHz, IDLE State	180.0	180.0	180.0	nA
		OSC 2 MHz, PreScaler = 1	5.9	11.6	19.6	µA
		OSC 2 MHz, PreScaler = 2	5.3	10.6	17.9	µA
		OSC 2 MHz, PreScaler = 4	5.1	10.1	17.2	µA
		OSC 2 MHz, PreScaler = 8	4.9	9.9	16.8	µA
		OSC 25 kHz, IDLE State	40	40	40	nA
		OSC 25 kHz, PreScaler = 1	0.17	0.25	0.37	µA
		OSC 25 kHz, PreScaler = 2	0.16	0.24	0.35	µA
		OSC 25 kHz, PreScaler = 4	0.16	0.24	0.34	µA
		OSC 25 kHz, PreScaler = 8	0.16	0.23	0.34	µA
		V_{REF}(50 mV – 1200 mV)	4.6	4.6	4.6	µA
		V_{REF}(VDD)	3.5	6.4	10.6	µA
		V_{REF} Output buffer	13.8	13.9	14.0	µA
		ACMP (high speed mode)	10.0	10.2	10.5	µA
		ACMP (low current mode)	1.2	1.2	1.2	µA
		ACMP (high speed w/ buffer)	12.9	12.9	13.5	µA
		ACMP (low current w/ buffer)	4.0	4.1	4.2	µA
		100µA Current Source	7.35	7.40	7.45	µA

4.6. Timing Estimator

Table 4.6 Typical Propagation Time for Each Macrocell

Start Point	End point	Note	VDD = 1.8 V		VDD = 3.3 V		VDD = 5.0 V		Unit
			Low to High	High to Low	Low to High	High to Low	Low to High	High to Low	
DI w/o ST	DO PP×1	IO	51.35	35.75	15.33	12.52	10.05	8.63	ns
DI w/o ST	DO PP×2	IO	51.12	35.35	15.05	12.31	9.81	8.45	ns
DI w/ ST	DO PP×1	IO	53.52	37.46	16.47	13.31	11.25	9.23	ns
DI w/ ST	DO PP×2	IO	53.18	37.09	16.22	13.11	11.05	9.06	
DI LV	DO PP×1	IO	33.53	62.94	10.72	22.2	6.64	17.94	ns
DI LV	DO PP×2	IO	33.24	62.72	10.51	22.09	6.46	17.97	ns
DI w/o ST	DO NMOS×1	IO	--	34.35	--	12.06	--	8.26	ns
DI w/o ST	DO NMOS×2	IO	--	33.96	--	11.88	--	8.11	ns
DI w/o ST	DO PMOS×1	IO	48.67	--	14.26	--	9.3	--	ns
DI w/o ST	DO PMOS×2	IO	47.97	--	14.23	--	9.09	--	ns
IN	OUT	2-bit LUT	26.65	22.09	5.72	6.85	3.63	4.20	ns
IN	OUT	3-bit LUT	31.41	27.23	7.81	8.73	4.95	5.43	ns
IN	OUT	4-bit LUT	29.70	29.06	8.89	9.30	5.35	5.86	ns
CLK	Q	DFF w/o nRST(nSET)	23.78	23.73	7.25	8.07	4.68	5.40	ns
CLK	nQ	DFF w/o nRST(nSET)	23.02	24.39	7.06	8.11	5.04	5.45	ns
CLK	Q	DFF w/ nRST(nSET)	25.04	24.78	7.67	8.35	4.90	5.81	ns
nRST	Q	DFF w/ nRST	--	26.50	--	8.51	--	5.41	ns
RST	Q	DFF w/ RST	--	25.54	--	8.51	--	5.86	ns
nSET	Q	DFF w/ nSET	28.76	--	9.17	--	6.35	--	ns
SET	Q	DFF w/ SET	27.33	--	8.62	--	5.32	--	ns
CLK	nQ	DFF w/ nRST(nSET)	24.50	25.36	7.54	8.43	4.91	6.01	ns
nRST	nQ	DFF w/ nRST	26.46	--	8.66	--	5.91	--	ns
RST	nQ	DFF w/ RST	25.24	--	7.75	--	4.97	--	ns
nSET	nQ	DFF w/ nSET	--	28.71	--	9.46	--	5.77	ns
SET	nQ	DFF w/ SET	--	27.72	--	9.04	--	6.28	ns
D	Q	LATCH w/o nRST(nSET)	22.79	23.27	7.81	7.66	4.27	4.93	ns
nL	Q	LATCH w/o nRST(nSET)	21.97	22.35	7.94	7.50	4.20	4.85	ns
D	nQ	LATCH w/o nRST(nSET)	25.49	25.29	7.82	8.29	4.92	5.60	ns

Start Point	End point	Note	VDD = 1.8 V		VDD = 3.3 V		VDD = 5.0 V		Unit
			Low to High	High to Low	Low to High	High to Low	Low to High	High to Low	
nL	nQ	LATCH w/o nRST(nSET)	25.08	25.02	7.69	8.22	4.84	5.52	ns
D	Q	LATCH w/ nRST(nSET)	24.28	25.82	7.44	8.23	4.70	5.30	ns
nL	Q	LATCH w/ nRST(nSET)	24.88	26.62	7.72	8.51	4.92	5.46	ns
nRST	Q	LATCH w/ nRST	29.02	26.55	9.24	8.72	6.15	6.06	ns
RST	Q	LATCH w/ RST	24.46	25.93	7.48	8.28	4.73	5.31	ns
nSET	Q	LATCH w/ nSET	25.32	26.46	7.96	8.52	5.14	5.60	ns
SET	Q	LATCH w/ SET	28.56	26.64	9.06	8.73	5.93	6.05	ns
D	nQ	LATCH w/ nRST(nSET)	27.24	26.83	8.38	8.74	5.30	5.99	ns
nL	nQ	LATCH w/ nRST(nSET)	26.55	25.68	8.66	8.48	5.84	5.97	ns
nRST	nQ	LATCH w/ nRST	27.99	28.11	8.56	9.17	5.38	5.87	ns
RST	nQ	LATCH w/ RST	27.31	26.93	8.39	8.75	5.31	5.99	ns
nSET	nQ	LATCH w/ nSET	26.94	26.39	8.67	8.69	5.74	5.82	ns
SET	nQ	LATCH w/ SET	27.76	27.71	8.59	9.03	5.48	5.87	ns
CLK	OUT0	Shift register	34.91	38.01	29.91	32.55	8.66	9.13	ns
CLK	OUT1	Shift register	36.19	40.33	31.44	34	9.04	9.48	ns
CLK	Q[1]	Shift register	28.35	27.64	24.68	23.63	7.46	6.31	ns
CLK	nOUT1	Shift register	40.49	36.91	34.1	31.59	9.49	8.77	ns
nRST	OUT0	Shift register	--	38.76	--	33.02	--	9.47	ns
nRST	OUT1	Shift register	--	40.26	--	34.46	--	9.8	ns
nRST	Q[1]	Shift register	--	28.59	--	24.46	--	7.09	ns
nRST	nOUT1	Shift register	40.67	--	34.68	--	9.39	--	ns
IN	OUT	8-bit TMR (Delay)	40.80	40.46	13.04	13.42	8.41	8.81	ns
IN	OUT	8-bit TMR (One-Shot)	45.52	--	14.85	--	9.33	--	ns
RST	OUT	8-bit TMR (Counter)	55.69	--	17.81	--	11.14	--	ns
IN	OUT	8-bit TMR (Frequency Detector)	44.15	--	14.34	--	9.00	--	ns
IN	OUT	8-bit TMR (Edge Detector)	35.73	--	11.63	--	7.45	--	ns
CLK	OUT	8-bit TMR (Delay)	62.92	77.33	20.06	23.90	12.67	14.76	ns
CLK	OUT	8-bit TMR (One-Shot)	--	80.00	--	24.99	--	15.16	ns
CLK	OUT	8-bit TMR (Counter)	61.40	78.63	19.62	24.75	12.39	15.36	ns
CLK	OUT	8-bit TMR (Frequency Detector)	--	78.10	--	24.39	--	15.05	ns
CLK	OUT	8-bit TMR (Delayed Edge Detector)	78.26	--	24.40	--	14.93	--	ns
IN	OUT	16-bit TMR (Delay)	64.67	52.09	18.99	17.91	12.02	11.86	ns
IN	OUT	16-bit TMR (One-Shot)	67.91	--	20.32	--	12.74	--	ns
RST	OUT	16-bit TMR (Counter)	85.11	--	25.58	--	15.97	--	ns
IN	OUT	16-bit TMR (Frequency Detector)	66.24	--	19.30	--	12.33	--	ns
CLK	OUT	16-bit TMR (Delay)	95.10	99.33	28.55	31.15	17.77	19.57	ns
CLK	OUT	16-bit TMR (One-Shot)	--	102.04	--	32.01	--	20.17	ns
CLK	OUT	16-bit TMR (Counter)	92.87	91.61	27.89	29.35	17.26	18.61	ns
CLK	OUT	16-bit TMR (Frequency Detector)	--	100.59	--	31.60	--	19.87	ns
CLK	OUT	16-bit TMR (Delayed Edge Detector)	110.93	--	33.42	--	20.70	--	ns

Table 4.7 Expected Delays and Widths for Programmable Delay/Edge Detector

Symbol	Parameter	Note	V_{DD} = 1.8V	V_{DD} = 3.3V	V_{DD} = 5.0V	Unit
T_{Width}	Width, 140ns	Mode:(any)Edge Detect, Edge Detect Output	144.5	134.8	137.9	ns
T_{Width}	Width, 280ns	Mode:(any)Edge Detect, Edge Detect Output	273.4	269.5	281.6	ns
T_{Width}	Width, 420ns	Mode:(any)Edge Detect, Edge Detect Output	399.7	400.9	422.5	ns
T_{Width}	Width, 560ns	Mode:(any)Edge Detect, Edge Detect Output	526.9	533.3	564.4	ns
T_{PROP}	Delay, 140ns	Mode:(any)Edge Detect, Edge Detect Output	38.9	11.5	7.1	ns
T_{PROP}	Delay, 280ns	Mode:(any)Edge Detect, Edge Detect Output	38.9	11.5	7.1	ns
T_{PROP}	Delay, 420ns	Mode:(any)Edge Detect, Edge Detect Output	38.9	11.5	7.1	ns
T_{PROP}	Delay, 560ns	Mode:(any)Edge Detect, Edge Detect Output	38.9	11.5	7.1	ns
T_{DLY}	Delay, 140ns	Mode: Both Edge Delay, Edge Detect Output	183.4	146.3	145	ns
T_{DLY}	Delay, 280ns	Mode: Both Edge Delay, Edge Detect Output	312.3	281	288.7	ns
T_{DLY}	Delay, 420ns	Mode: Both Edge Delay, Edge Detect Output	438.6	412.4	429.6	ns
T_{DLY}	Delay, 560ns	Mode: Both Edge Delay, Edge Detect Output	565.8	544.8	571.5	ns

4.7. OSC Specifications

4.7.1. 25 kHz Oscillator

Table 4.8 25 kHz OSC Frequency Limits

Power Supply Range V_{DD}, V	Temperature Range					
	+25 °C		0 °C ... +85 °C		-40 °C ... +85 °C	
	Min, kHz	Max, kHz	Min, kHz	Max, kHz	Min, kHz	Max, kHz
1.8 V ±5%	24.611	25.366	--	--	22.559	28.063
3.3 V ±10%	24.550	25.454	--	--	22.628	27.982
5 V ±10%	24.548	25.681	--	--	22.514	28.270
1.71 V…5.50 V	24.548	25.827	--	--	22.514	28.462

Table 4.9 25 kHz OSC Frequency Error (Error Calculated Relative to Nominal Value)

Power Supply Range V_{DD}, V	Temperature Range					
	+25 °C		0 °C ... +85 °C		-40 °C ... +85 °C	
	Min	Max	Min	Max	Min	Max
1.8 V ±5%	-1.56%	1.47%			-9.77%	12.26%
3.3 V ±10%	-1.80%	1.82%			-9.49%	11.93%
5 V ±10%	-1.81%	2.73%			-9.95%	13.08%
1.71 V…5.50 V	-1.81%	3.31%			-9.95%	13.85%

Table 4.10 25 kHz OSC Power on time at Room Temperature

Power Supply Range V_{DD}, V	Normal		Fast	
	Typ, us	Max, us	Typ, us	Max, us
1.80	347.0	404.8	17.5	39.8
3.30	347.0	385.2	17.5	38.3
5.00	347.0	361.1	17.5	40.9
1.71 V…5.50 V	347.0	405.1	17.5	41.7

Table 4.11 25 kHz OSC Frequency Settling Time

Parameter	Description	Typ	Max	Unit
Frequency Settling Time	To reach the 7.0% error	0	1	Cycles

4.7.2. 2 MHz Oscillator

Table 4.12 2 MHz OSC Frequency Limits

Power Supply Range V_{DD}, V	Temperature Range					
	+25 °C		0 °C ... +85 °C		-40 °C ... +85 °C	
	Min, MHz	Max, MHz	Min, MHz	Max, MHz	Min, MHz	Max, MHz
1.8 V ±5%	1.958	2.045	--	--	1.828	2.223
3.3 V ±10%	1.958	2.041	--	--	1.827	2.220
5 V ±10%	1.958	2.058	--	--	1.824	2.242
1.71 V…5.50 V	1.955	2.068	--	--	1.824	2.252

Table 4.13 2 MHz OSC Frequency Error (Error Calculated in Relation to Nominal Value)

Power Supply Range V_{DD}, V	Temperature Range					
	+25 °C		0 °C ... +85 °C		-40 °C ... +85 °C	
	Min	Max	Min	Max	Min	Max
1.8 V ±5%	-2.10%	2.25%	--	--	-8.60%	11.15%
3.3 V ±10%	-2.10%	2.05%	--	--	-8.65%	11.00%
5 V ±10%	-2.10%	2.90%	--	--	-8.80%	12.10%
1.71 V…5.50 V	-2.25%	3.40%	--	--	-8.80%	12.60%

Table 4.14 2 MHz OSC Power on time at Room Temperature

Power Supply Range V_{DD}, V	Normal		Fast	
	Typ, us	Max, us	Typ, us	Max, us
1.80	70.00	95.00	0.45	1.23
3.30	70.00	88.05	0.45	1.29
5.00	70.00	79.40	0.45	1.05
1.71 V…5.50 V	70.00	95.39	0.45	1.29

Table 4.15 2 MHz OSC Frequency Settling Time

Parameter	Description	Typ	Max	Unit
Frequency Settling Time	To reach the 6.0% error	4	10	Cycles

4.8. ACMP Specifications

Table 4.16 ACMP Specifications

Symbol	Parameter	Description/Note	Conditions	Min	Typ	Max	Unit
V_{ACMP}	ACMP Input Voltage Range	Positive Input		0	--	VDD	V
		Negative Input		0	--	VDD	V
V_{OFFSET}	ACMP Input Offset Voltage	Low Current - Enable, V_{HYS} = 0 mV, Gain = 1, V_{REF} = (50…1200) mV, V_{DD} = (1.71…5.50) V	T = 25°C	-6	--	6	mV
			T = (-40…85)°C	-7	--	7	mV
		Low Current - Disable, V_{HYS} = 0 mV, Gain = 1, V_{REF} = (50...1200) mV, V_{DD} = (1.71…5.50) V	T = 25°C	-6	--	6	mV
			T = (-40...85)°C	-7	--	7	mV
t_{START}	ACMP Power On Time	ACMP Power on time, Minimal required wake time for the "Wake and Sleep function"	T = 25°C	--	70.0	89.2	µs
			T = (-40…85)°C	--	70.0	101.4	µs
R_{SIN}	Series Input Resistance	GAIN = 1×		--	100.0	--	MΩ
		GAIN = 0.5×		--	2.0	--	MΩ
		GAIN = 0.33×		--	2.0	--	MΩ
		GAIN = 0.25×		--	2.0	--	MΩ
t_{PROP}	Propagation Delay, Response Time	Low Power, Gain = 1, Overdrive = 10 mV V_{REF} = (50…1200) mV	Low to High T = 25°C	--	20.00	--	µs
			High to Low T = 25°C	--	25.00	--	µs
			Low to High T = (-40...+85)°C	--	20.00	--	µs
			High to Low T = (-40...+85)°C	--	25.00	--	µs
		High Speed, Gain = 1, Overdrive = 10 mV V_{REF} = (50…1200) mV	Low to High T = 25°C	--	1.00	--	µs
			High to Low T = 25°C	--	1.00	--	µs
			Low to High T = (-40...+85)°C	--	1.0	--	µs
			High to Low T = (-40...+85)°C	--	1.0	--	µs
G	Gain error (including threshold and internal V_{REF} error)	G = 1		--	1	--	
		G = 0.5		0.497	--	0.501	
		G = 0.33		0.331	--	0.335	
		G = 0.25		0.248	--	0.251	

4.9. Voltage Reference Specification

Table 4.17 VREF Specifications

Symbol	Parameter	Description/Note	Conditions	Min	Typ	Max	Unit
ΔV_{REF}	Internal V_{REF} error	V_{DD} = 1.71 V…5.50 V	T = 25°C	-0.70	--	1.30	%
			T = (-40...85)°C	-2.06	--	1.73	%
$\Delta V_{REF\ OUT}$	Output V_{REF} error (Buffered)	V_{DD} = 1.71 V…5.50 V Loading is 1µA	T = 25°C	-0.72	--	1.38	%
			T = (-40...85)°C	-2.93	--	1.75	%
$C_{VREF\ OUT}$	Output Capacitance Loading	R_{LR} – Load Resistance	R_{LR} = 1MΩ	--	--	25	pF
R_{VDD_DIV}		VDD Divider is 1		--	100.0	--	MΩ

Symbol	Parameter	Description/Note	Conditions	Min	Typ	Max	Unit
	VDD Divider Stage Input Resistance	VDD Divider is 1/2		--	2.0	--	MΩ
		VDD Divider is 1/3		--	2.0	--	MΩ
		VDD Divider is 1/4		--	2.0	--	MΩ
R_{EXT_DIV}	External VREF (IO4) Divider Stage Input Resistance	External Divider is 1		--	100.0	--	MΩ
		External Divider is 1/2		--	2.0	--	MΩ
		External Divider is 1/3		--	2.0	--	MΩ
		External Divider is 1/4		--	2.0	--	MΩ

4.10. 100µA Current Source Specifications

Table 4.18 Current Source Electrical Characteristics

Symbol	Parameter	Condition/Note	Min	Typ	Max	Unit
I_O	Output Current	V_{DD} = 1.71, V_{IO} = 0…V_{DD}-0.3V, T = 25°C	81.2	100.0	115.0	µA
		V_{DD} = 1.71, V_{IO} = 0…V_{DD}-1.0V T = 25°C	82.6	100.0	115.0	µA
		V_{DD} = 3.3, V_{IO} = V_{DD}-0.7V T = 25°C	79.8	100	112.8	µA
		V_{DD} = 5.5, V_{IO} = V_{DD}-0.7V T = 25°C	77.4	100	119.9	µA
		V_{DD} = 1.71, V_{IO} = V_{DD}-0.7V T = (-40…85)°C	81.2	100	115.0	µA
		V_{DD} = 3.3, V_{IO} = V_{DD}-0.7V T = (-40…85)°C	79.7	100	112.8	µA
		V_{DD} = 5.5, V_{IO} = V_{DD}-0.7V T = (-40…85)°C	77.4	100	119.9	µA
R_{OUT}	Output Impedance	T = 25°C	310.9	--	653.4	MΩ
		T = (-40…85)°C	299.1	--	669.5	MΩ

5. IO PINs

5.1. Input Modes

Each of the IOs can be configured as a Digital Input PIN with or without a buffered Schmitt trigger, or they can also be configured as a Digital Input Low Voltage. IO12 can be configured as External CLK Connection. IO3, IO4, and IO6 can be configured as Analog Inputs.

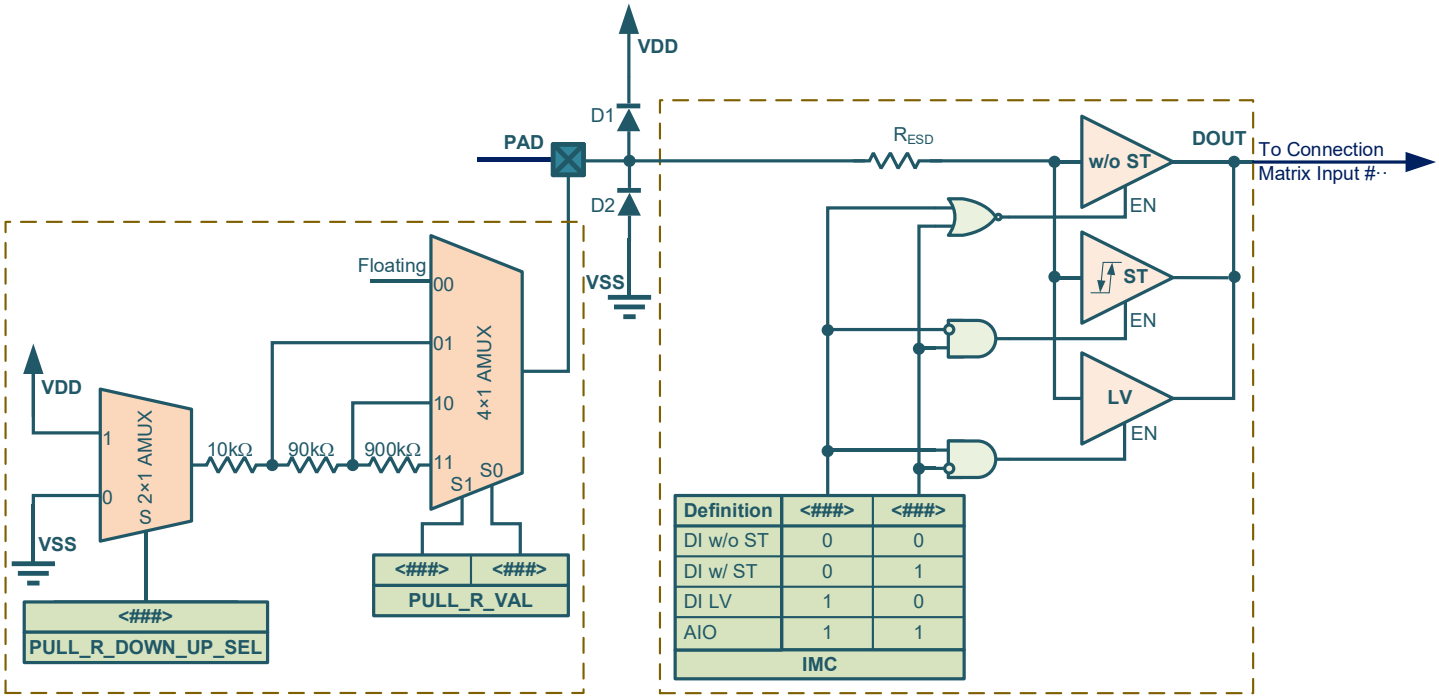
5.2. Output Modes

All IOs, except IO2, can be configurable as digital outputs. IO10 can output V_{REF}.

5.3. Pull Up/Down Resistors

All IOs have an option for user-selectable resistors to be connected to the input structure, with the selectable values being 10 kΩ, 100 kΩ, and 1 MΩ. The internal resistors can be configured as pull-up or pull-down.

5.4. Digital Input Structure (for IO2)



Definition	<###>	<###>
DI w/o ST	0	0
DI w/ ST	0	1
DI LV	1	0
AIO	1	1
IMC		

Figure 5.1. IO2 Structure Diagram

5.5. IO Structure (for IO3)

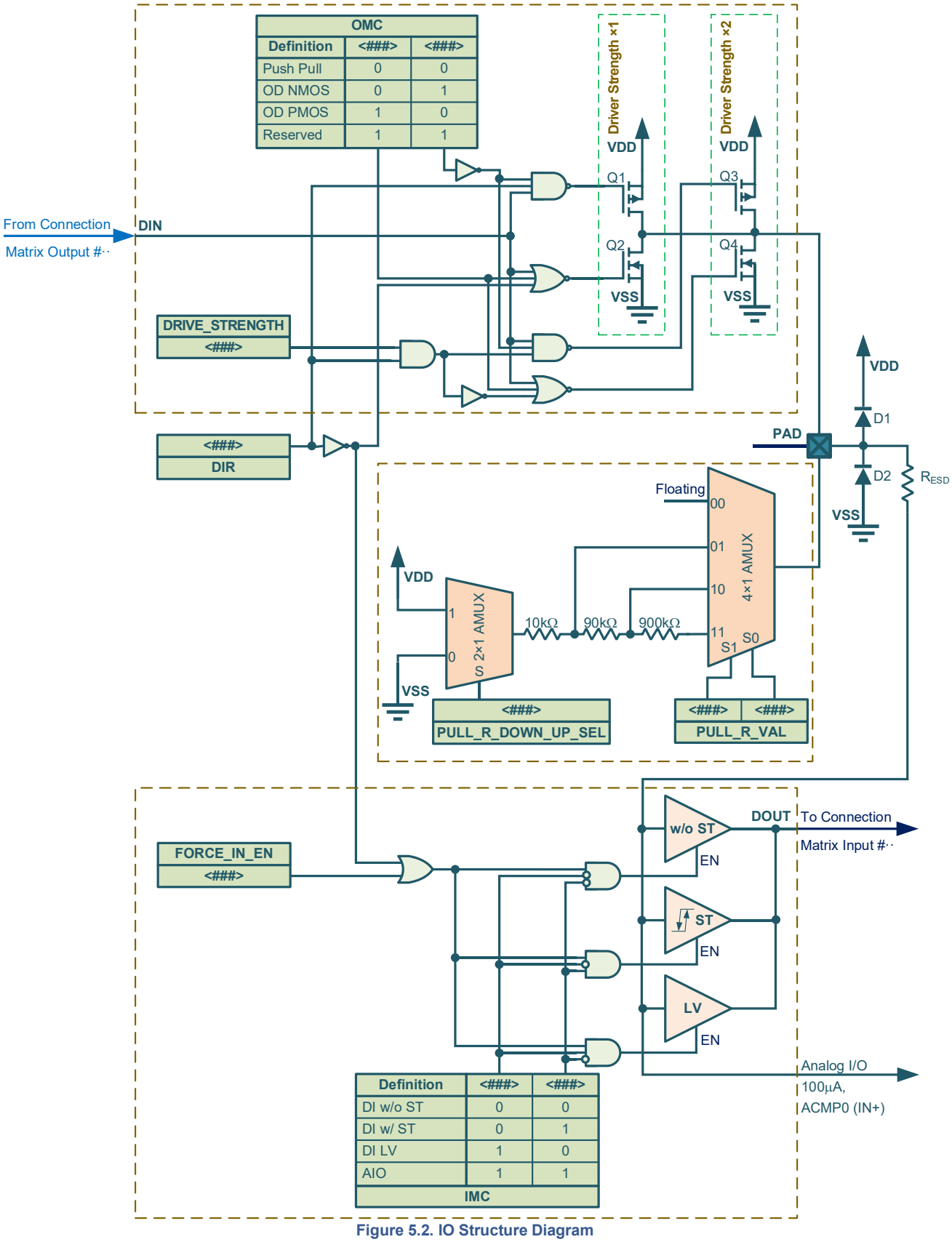


Figure 5.2. IO Structure Diagram

5.6. IO Structure (for IO4)

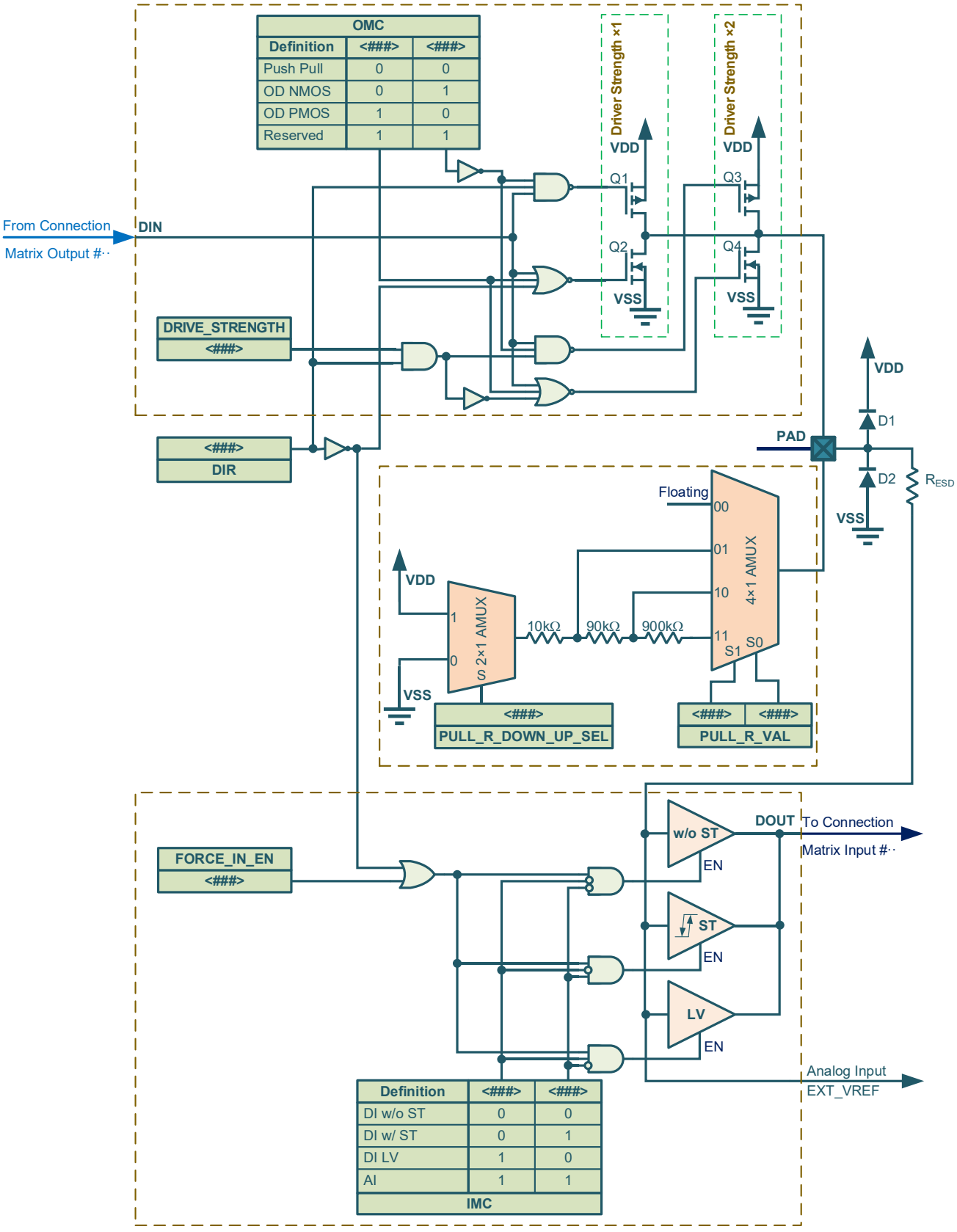


Figure 5.3. Digital IO Structure Diagram

5.7. Digital IO Structure (for IO5, IO8, IO9 and IO11)

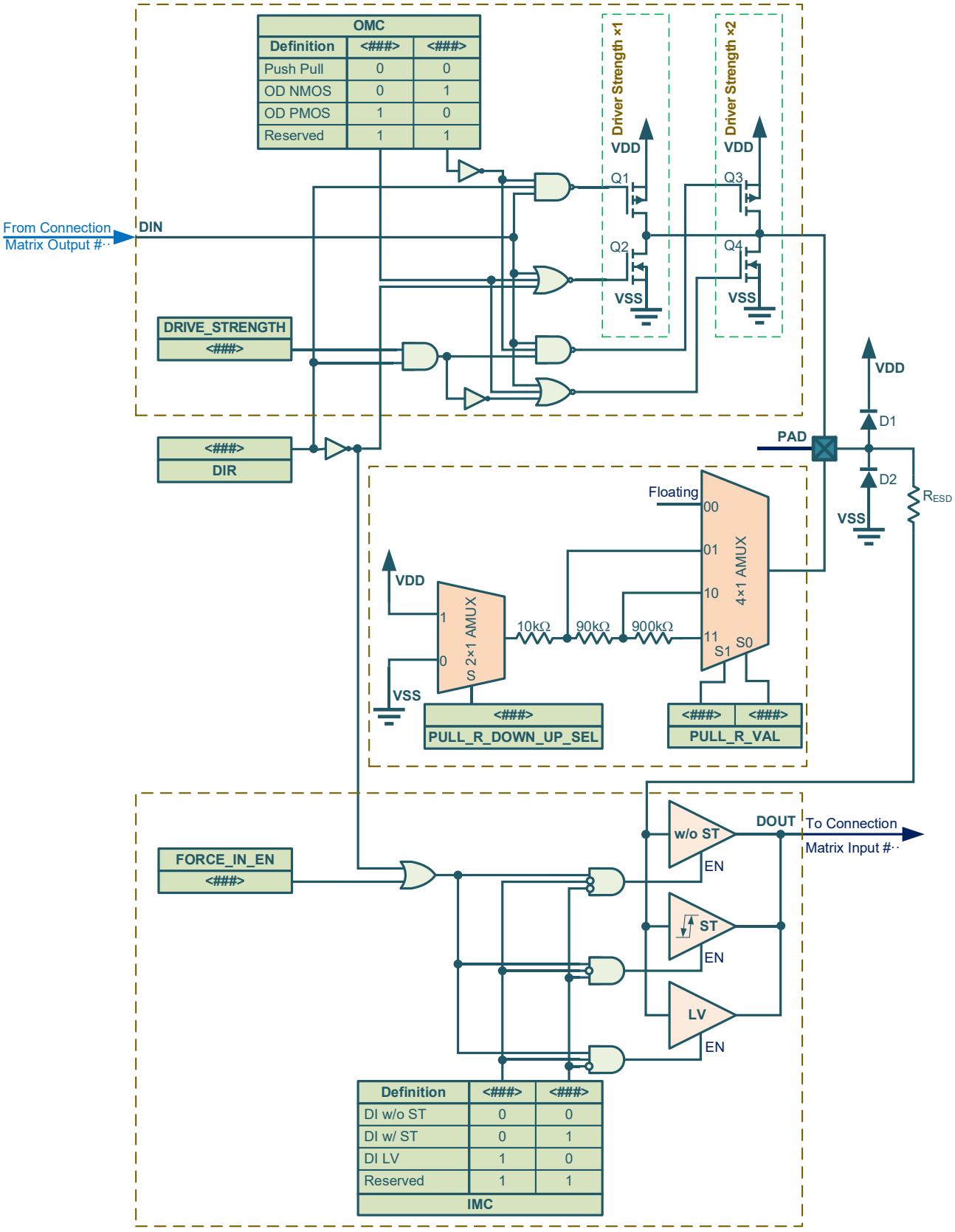


Figure 5.4. IO Structure Diagram

5.8. IO Structure (for IO6)

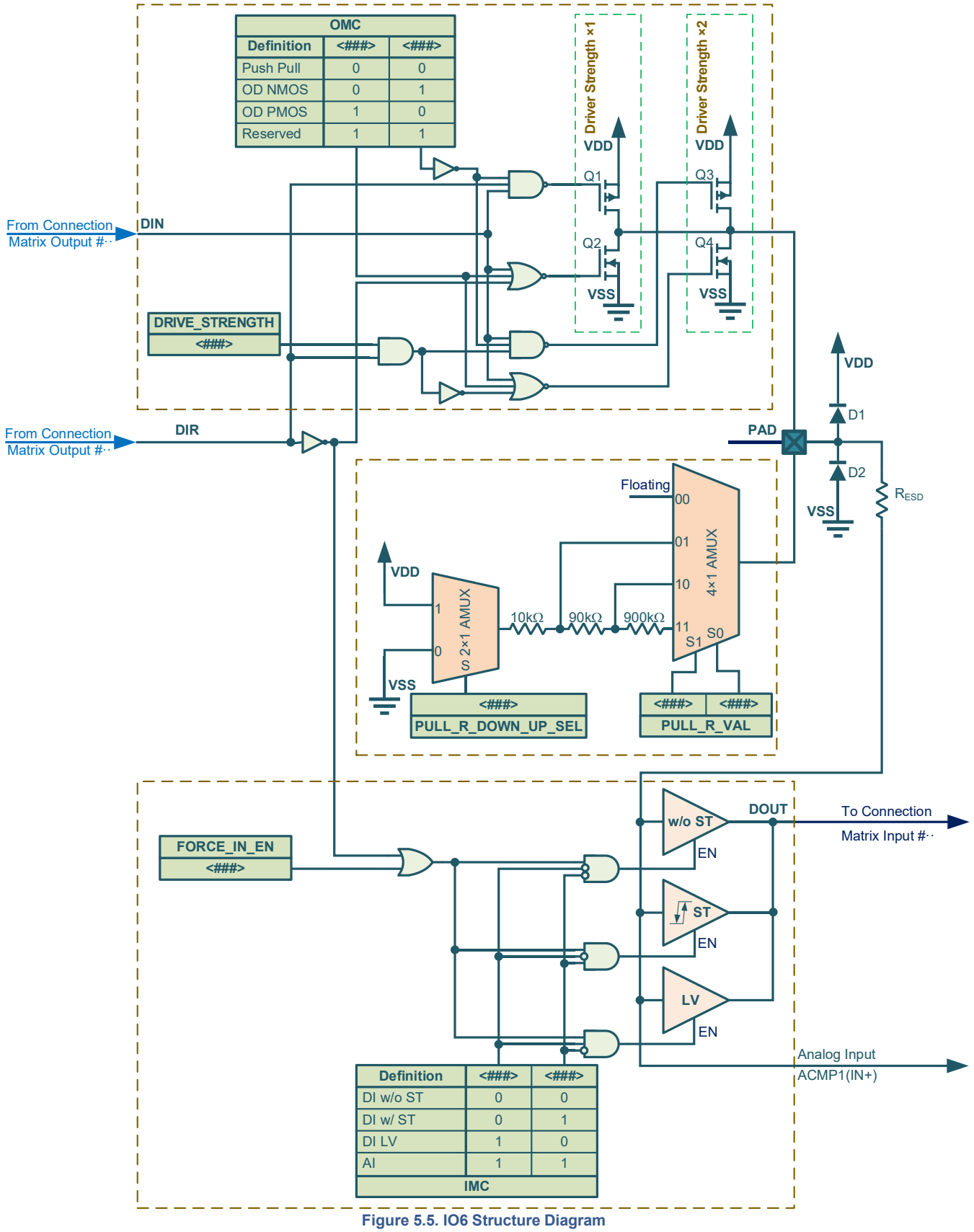


Figure 5.5. IO6 Structure Diagram

5.9. IO Structure (for IO10)

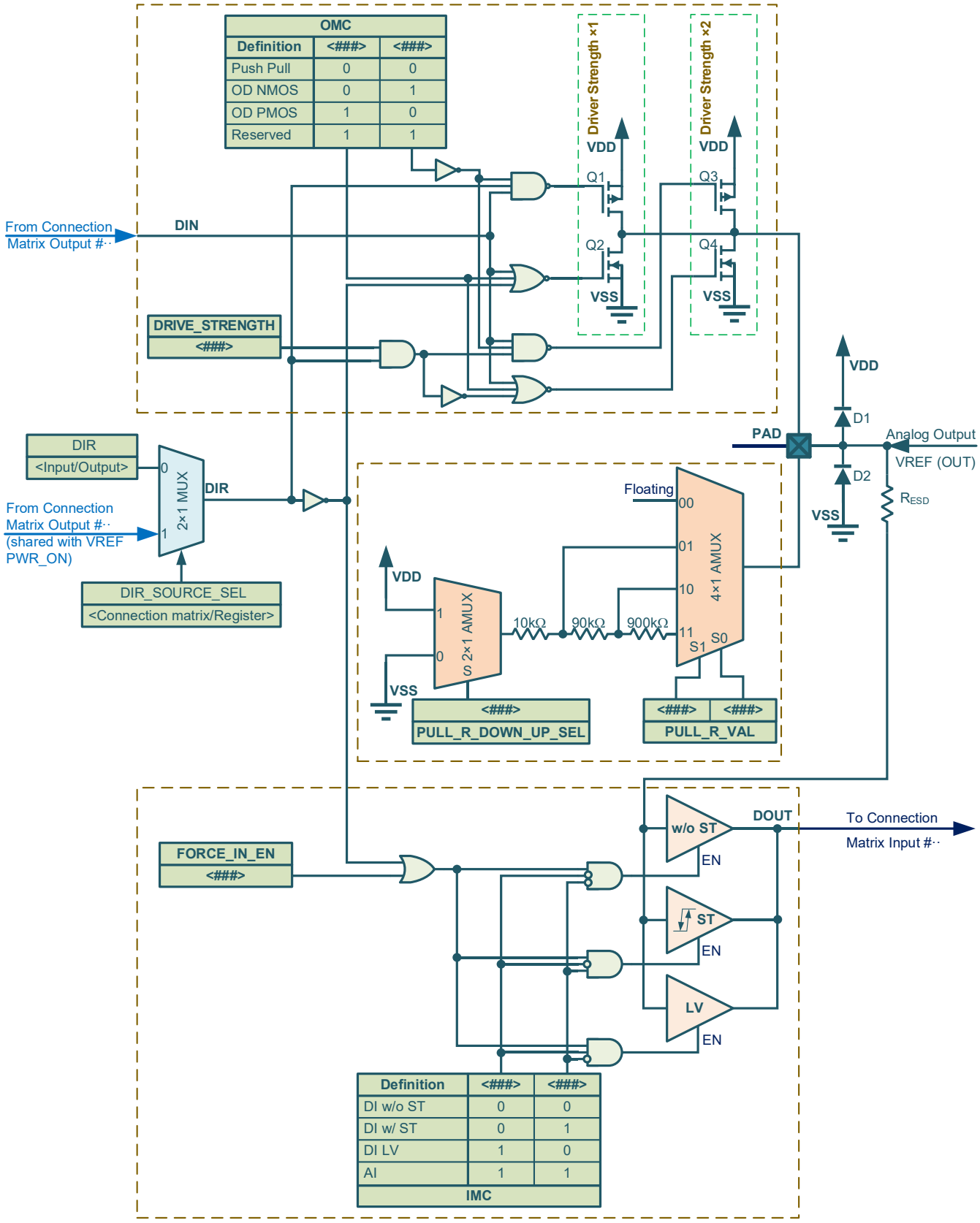


Figure 5.6. IO10 Structure Diagram

5.10. Digital IO Structure (for IO12)

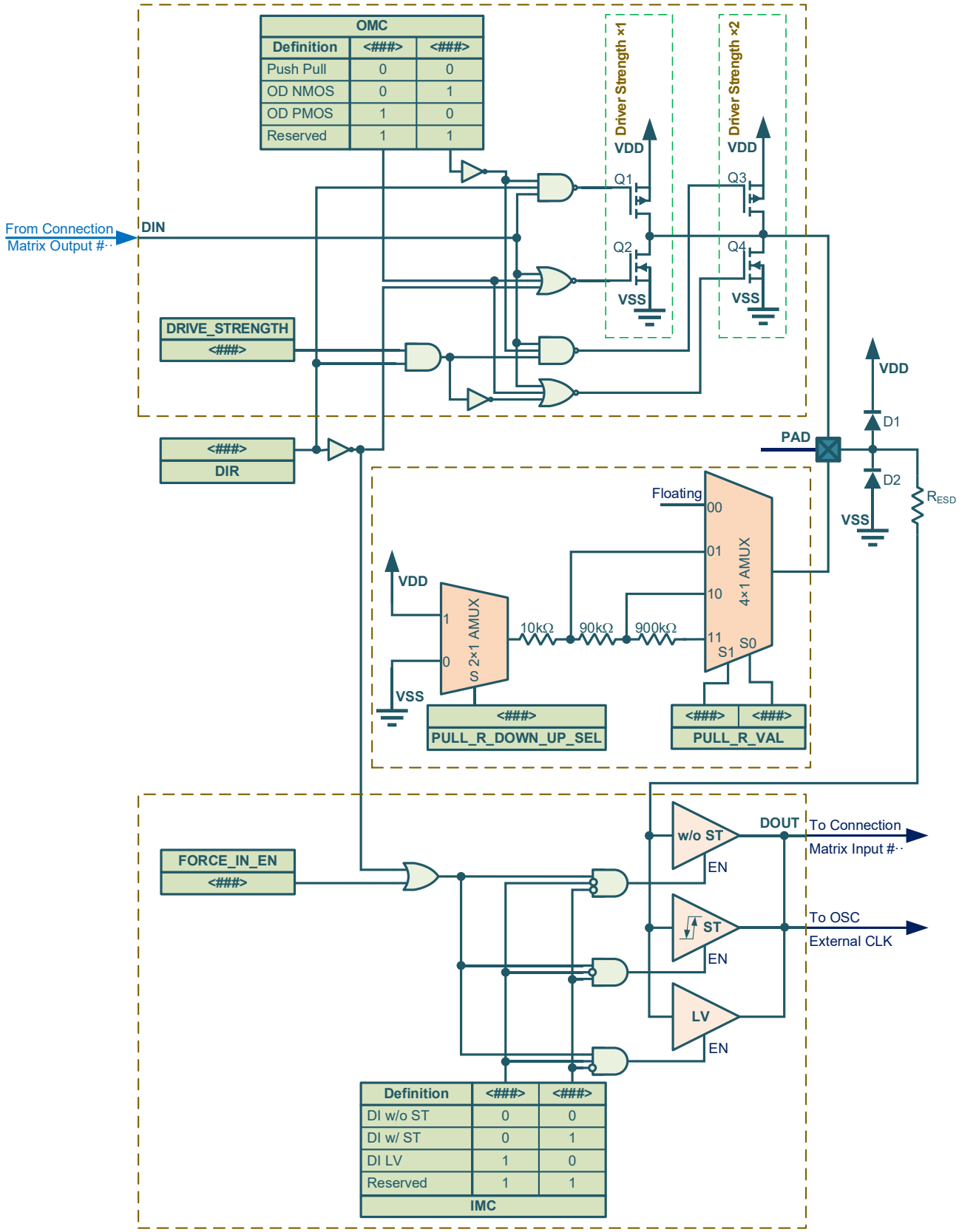


Figure 5.7. IO Structure Diagram

5.11. IO Registers

5.11.1. IO2 Registers

Table 5.1 IO2 Registers

Register Bit Address	Register Name	Register Definition
IO2		
<472:471>	IO2_IMC	Input mode control: 00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Digital Input Low Voltage 11: Reserved
<473>	IO2_PULL_R_DOWN_UP_SEL	Pull resistor: 0: Down 1: Up
<475:474>	IO2_PULL_R_VAL	Pulled resistor value: 00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor

5.11.2. IO3 Registers

Table 5.2 IO3 Registers

Register Bit Address	Register Name	Register Definition
IO3		
<477>	IO3_DIR	Direction: 0: Input 1: Output
<478>	IO3_FORCE_IN_EN	Force input: 0: Disable 1: Enable (Input is always ON)
<480:479>	IO3_IMC	Input mode control: 00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Digital Input Low Voltage 11: Analog IO
<482:481>	IO3_OMC	Output mode control: 00: Push Pull 01: Open Drain NMOS 10: Open Drain PMOS 11: Reserved
<483>	IO3_DRIVE_STRENGTH	Drive strength: 0: ×1 1: ×2
<484>	IO3_PULL_R_DOWN_UP_SEL	Pull resistor: 0: Down 1: Up
<486:485>	IO3_PULL_R_VAL	Pulled resistor value: 00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor

5.11.3. IO4 Registers

Table 5.3 IO4 Registers

Register Bit Address	Register Name	Register Definition
IO4		
<488>	IO4_DIR	Direction: 0: Input 1: Output
<489>	IO4_FORCE_IN_EN	Force input: 0: Disable 1: Enable (Input is always ON)
<491:490>	IO4_IMC	Input mode control: 00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Digital Input Low Voltage 11: Analog IO
<493:492>	IO4_OMC	Output mode control: 00: Push Pull 01: Open Drain NMOS 10: Open Drain PMOS 11: Reserved
<494>	IO4_DRIVE_STRENGTH	Drive strength: 0: ×1 1: ×2
<495>	IO4_PULL_R_DOWN_UP_SEL	Pull resistor: 0: Down 1: Up
<497:496>	IO4_PULL_R_VAL	Pulled resistor value: 00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor

5.11.4. IO5 Registers

Table 5.4 IO5 Registers

Register Bit Address	Register Name	Register Definition
IO5		
<499>	IO5_DIR	Direction: 0: Input 1: Output
<500>	IO5_FORCE_IN_EN	Force input: 0: Disable 1: Enable (Input is always ON)
<502:501>	IO5_IMC	Input mode control: 00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Digital Input Low Voltage 11: Reserved
<504:503>	IO5_OMC	Output mode control: 00: Push Pull 01: Open Drain NMOS 10: Open Drain PMOS 11: Reserved
<505>	IO5_DRIVE_STRENGTH	Driver strength: 0: ×1 1: ×2
<506>	IO5_PULL_R_DOWN_UP_SEL	Pull resistor: 0: Down 1: Up
<508:507>	IO5_PULL_R_VAL	Pulled resistor value: 00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor

5.11.5. IO6 Registers

Table 5.5 IO6 Registers

Register Bit Address	Register Name	Register Definition
IO6		
<510>	IO6_FORCE_IN_EN	Force input: 0: Disable 1: Enable (Input is always ON)
<512:511>	IO6_IMC	Input mode control: 00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Digital Input Low Voltage 11: Analog IO
<514:513>	IO6_OMC	Output mode control: 00: Push Pull 01: Open Drain NMOS 10: Open Drain PMOS 11: Reserved
<515>	IO6_DRIVE_STRENGTH	Drive strength: 0: ×1 1: ×2
<516>	IO6_PULL_R_DOWN_UP_SEL	Pull resistor: 0: Down 1: Up
<518:517>	IO6_PULL_R_VAL	Pulled resistor value: 00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor

5.11.6. IO8 Registers

Table 5.6 IO8 Registers

Register Bit Address	Register Name	Register Definition
IO8		
<519>	IO8_DIR	Direction: 0: Input 1: Output
<520>	IO8_FORCE_IN_EN	Force input: 0: Disable 1: Enable (Input is always ON)
<522:521>	IO8_IMC	Input mode control: 00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Digital Input Low Voltage 11: Reserved
<524:523>	IO8_OMC	Output mode control: 00: Push Pull 01: Open Drain NMOS 10: Open Drain PMOS 11: Reserved
<525>	IO8_DRIVE_STRENGTH	Drive strength: 0: ×1 1: ×2
<526>	IO8_PULL_R_DOWN_UP_SEL	Pull resistor: 0: Down 1: Up
<528:527>	IO8_PULL_R_VAL	Pulled resistor value: 00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor

5.11.7. IO9 Registers

Table 5.7 IO9 Registers

Register Bit Address	Register Name	Register Definition
IO9		
<530>	IO9_DIR	Direction: 0: Input 1: Output
<531>	IO9_FORCE_IN_EN	Force input: 0: Disable 1: Enable (Input is always ON)
<533:532>	IO9_IMC	Input mode control: 00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Digital Input Low Voltage 11: Reserved
<535:534>	IO9_OMC	Output mode control: 00: Push Pull 01: Open Drain NMOS 10: Open Drain PMOS 11: Reserved
<536>	IO9_DRIVE_STRENGTH	Drive strength: 0: ×1 1: ×2
<537>	IO9_PULL_R_DOWN_UP_SEL	Pull resistor: 0: Down 1: Up
<539:538>	IO9_PULL_R_VAL	Pulled resistor value: 00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor

5.11.8. IO10 Registers

Table 5.8 IO10 Registers

Register Bit Address	Register Name	Register Definition
IO10		
<541>	IO10_DIR	Direction: 0: Input 1: Output
<542>	IO10_FORCE_IN_EN	Force input: 0: Disable 1: Enable (Input is always ON)
<544:543>	IO10_IMC	Input mode control: 00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Digital Input Low Voltage 11: Analog IO
<546:545>	IO10_OMC	Output mode control: 00: Push Pull 01: Open Drain NMOS 10: Open Drain PMOS 11: Reserved
<547>	IO10_DRIVE_STRENGTH	Drive strength: 0: ×1 1: ×2
<548>	IO10_PULL_R_DOWN_UP_SEL	Pull resistor: 0: Down 1: Up
<550:549>	IO10_PULL_R_VAL	Pulled resistor value: 00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
<551>	IO10_DIR_SOURCE_SEL	Direction source selection: 0: Register IO10_DIR 1: Connection matrix CMO10

5.11.9.IO11 Registers

Table 5.9 IO11 Registers

Register Bit Address	Register Name	Register Definition
IO11		
<553>	IO11_DIR	Direction: 0: Input 1: Output
<554>	IO11_FORCE_IN_EN	Force input: 0: Disable 1: Enable (Input is always ON)
<556:555>	IO11_IMC	Input mode control: 00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Digital Input Low Voltage 11: Reserved
<558:557>	IO11_OMC	Output mode control: 00: Push Pull 01: Open Drain NMOS 10: Open Drain PMOS 11: Reserved
<559>	IO11_DRIVE_STRENGTH	Drive strength: 0: ×1 1: ×2
<560>	IO11_PULL_R_DOWN_UP_SEL	Pull resistor: 0: Down 1: Up
<562:561>	IO11_PULL_R_VAL	Pulled resistor value: 00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor

5.11.10. IO12 Registers

Table 5.10 IO12 Registers

Register Bit Address	Register Name	Register Definition
IO12		
<564>	IO12_DIR	Direction: 0: Input 1: Output
<565>	IO12_FORCE_IN_EN	Force input: 0: Disable 1: Enable (Input is always ON)
<567:566>	IO12_IMC	Input mode control: 00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Digital Input Low Voltage 11: Reserved
<569:568>	IO12_OMC	Output mode control: 00: Push Pull 01: Open Drain NMOS 10: Open Drain PMOS 11: Reserved
<570>	IO12_DRIVE_STRENGTH	Drive strength: 0: ×1 1: ×2
<571>	IO12_PULL_R_DOWN_UP_SEL	Pull resistor: 0: Down 1: Up
<573:572>	IO12_PULL_R_VAL	Pulled resistor value: 00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor

6. Connection Matrix

The ALM1412 Connection Matrix is used to create internal routing between cells, which in turn allows the user to retrieve customized functionality of the device. All of the connections of each cell within the ALM1412 are defined by the value of the corresponding register bits. These values are loaded from the NVM during power up of the device.

The Connection Matrix has 37 inputs and 63 outputs. Each individual input to the Connection Matrix is hard-wired to a particular macrocell output: including IO pins, Multifunctional Macrocells, Logic **1**, Logic **0,** etc. Each individual output from the Connection Matrix is hard-wired to a particular macrocell input and uses a 6-bit register to select one of the 37 input lines (see Section 6.1. Example of Connection).

For a complete list of the ALM1412 register table, see Section 18 Appendix A – ALM1412 Register Definition.

6.1. Example of Connection Matrix

A simple design example to showcase the Matrix Connection is shown in the Figure 6.1.

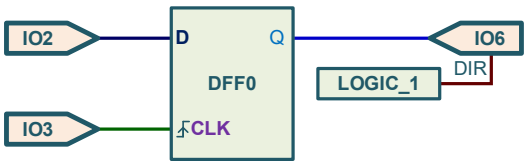


Figure 6.1. Example Design

Figure 6.2 and Figure 6.3 explain the strategy of Connection Matrix configuration.

Function	IN	Logic 0	Logic 1	IO2 (DOUT)	IO3 (DOUT)	IO4 (DOUT)	. . .	3BLUT3 (OUT)	DFF0 (Q)	MF1 (OUT)	. . .	OSC0 (OUT1)	Ready (OUT)
OUT		00	01	02	03	04	. . .	15	16	17	. . .	35	36
IO3 (DIN) <84:79>	00												
IO4 (DIN) <90:85>	01												
IO5(DIN) <96:91>	02												
IO6(DIN) <102:97>	03												
IO8(DIN) <108:103>	04												
. .	. .												
IO6(DIR) <138:133>	09												
. .	. .												
DFF0(CLK) <230:225>	24												
DFF0(D) <236:231>	25												
. .	. .												
. .	. .												
ACMP1 (PWR_ON) <462:457	62												

Figure 6.2. Connection Matrix Structure

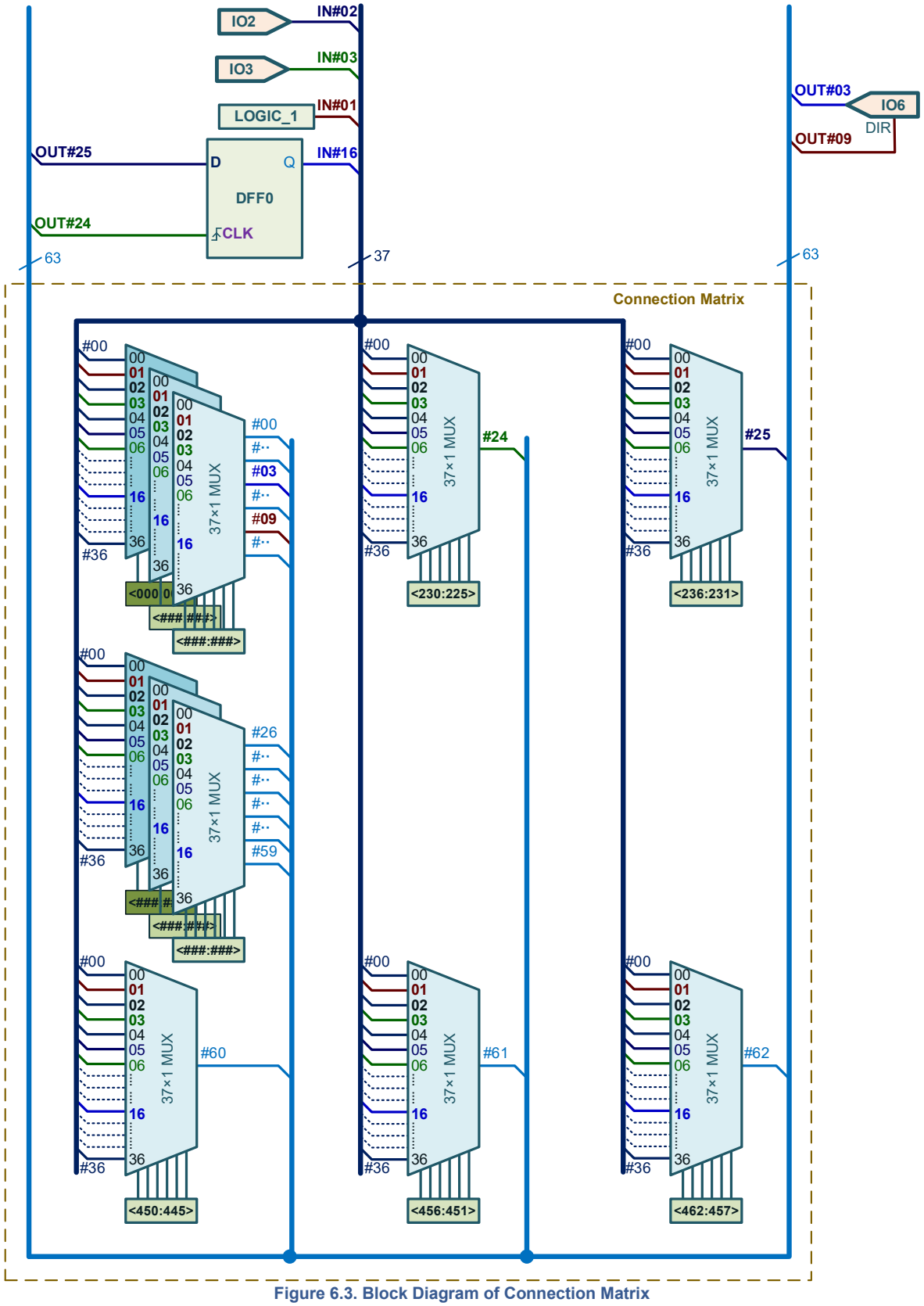


Figure 6.3. Block Diagram of Connection Matrix

6.2. Matrix Input

Table 6.1. Matrix Input Table

Matrix Input Number	Matrix Input Signal Function	Matrix Decode					
		5	4	3	2	1	0
00	Logic 0	0	0	0	0	0	0
01	Logic 1	0	0	0	0	0	1
02	IO2 DOUT	0	0	0	0	1	0
03	IO3 DOUT	0	0	0	0	1	1
04	IO4 DOUT	0	0	0	1	0	0
05	IO5 DOUT	0	0	0	1	0	1
06	IO6 DOUT	0	0	0	1	1	0
07	IO8 DOUT	0	0	0	1	1	1
08	IO9 DOUT	0	0	1	0	0	0
09	IO10 DOUT	0	0	1	0	0	1
10	IO11 DOUT	0	0	1	0	1	0
11	IO12 DOUT	0	0	1	0	1	1
12	3-bit LUT0 OUT	0	0	1	1	0	0
13	3-bit LUT1 OUT	0	0	1	1	0	1
14	3-bit LUT2 OUT	0	0	1	1	1	0
15	3-bit LUT3 OUT	0	0	1	1	1	1
16	MF0(2-bit LUT0/DFF0/LATCH0) OUT/Q/nQ	0	1	0	0	0	0
17	MF1(2-bit LUT1/DFF1/LATCH1) OUT/Q/nQ	0	1	0	0	0	1
18	MF2(2-bit LUT2/DFF2/LATCH2) OUT/Q/nQ	0	1	0	0	1	0
19	MF3(2-bit LUT3/DFF3/LATCH3) OUT/Q/nQ	0	1	0	0	1	1
20	MF4(3-bit LUT4/DFF4/LATCH4) OUT/Q/nQ	0	1	0	1	0	0
21	MF5(3-bit LUT5/DFF5/LATCH5) OUT/Q/nQ	0	1	0	1	0	1
22	MF6(3-bit LUT6/DFF6/LATCH6) OUT/Q/nQ	0	1	0	1	1	0
23	MF7(3-bit LUT7/DFF7/LATCH7) OUT/Q/nQ	0	1	0	1	1	1
24	MF8(3-bit LUT8/Shift Register) OUT0	0	1	1	0	0	0
25	MF8(3-bit LUT8/Shift Register) OUT1/nOUT1	0	1	1	0	0	1
26	MF8(3-bit LUT8/ Shift Register) OUT2(LUT)/Q(1)	0	1	1	0	1	0
27	MF9(3-bit LUT9/8-bit TMR1) OUT	0	1	1	0	1	1
28	MF10(4-bit LUT0/8-bit TMR2) OUT	0	1	1	1	0	0
29	MF11(4-bit LUT1/8-bit TMR3) OUT	0	1	1	1	0	1
30	MF12(PDLY/Edge Detector) OUT/nOUT	0	1	1	1	1	0
31	16-bit TMR0 OUT	0	1	1	1	1	1
32	ACMP0 OUT	1	0	0	0	0	0
33	ACMP1 OUT	1	0	0	0	0	1
34	OSC0 OUT0	1	0	0	0	1	0
35	OSC0 OUT1	1	0	0	0	1	1
36	Ready	1	1	0	0	0	0

6.3. Matrix Output

Table 6.2. Matrix Output Registers

Register Bit Address	Register Name	Register Definition
Connection matrix outputs		
<84:79>	CMO0_IO3_DIN	IO3 DIN
<90:85>	CMO1_IO4_DIN	IO4 DIN
<96:91>	CMO2_IO5_DIN	IO5 DIN
<102:97>	CMO3_IO6_DIN	IO6 DIN
<108:103>	CMO4_IO8_DIN	IO8 DIN
<114:109>	CMO5_IO9_DIN	IO9 DIN
<120:115>	CMO6_IO10_DIN	IO10 DIN
<126:121>	CMO7_IO11_DIN	IO11 DIN
<132:127>	CMO8_IO12_DIN	IO12 DIN
<138:133>	CMO9_IO6_DIR	IO6 DIR
<144:139>	CMO10_IO10_DIR_VREF_PWR_ON	IO10 DIR shared with PWR_ON of VREF
<151:146>	CMO11_OSC_CTRL_IN	OSC CTRL IN
<157:152>	CMO12_3BLUT0_IN0	3-bit LUT0 IN0
<163:158>	CMO13_3BLUT0_IN1	3-bit LUT0 IN1
<169:164>	CMO14_3BLUT0_IN2	3-bit LUT0 IN2
<175:170>	CMO15_3BLUT1_IN0	3-bit LUT1 IN0

Register Bit Address	Register Name	Register Definition
Connection matrix outputs		
<181:176>	CMO16_3BLUT1_IN1	3-bit LUT1 IN1
<187:182>	CMO17_3BLUT1_IN2	3-bit LUT1 IN2
<193:188>	CMO18_3BLUT2_IN0	3-bit LUT2 IN0
<199:194>	CMO19_3BLUT2_IN1	3-bit LUT2 IN1
<205:200>	CMO20_3BLUT2_IN2	3-bit LUT2 IN2
<211:206>	CMO21_3BLUT3_IN0	3-bit LUT3 IN0
<217:212>	CMO22_3BLUT3_IN1	3-bit LUT3 IN1
<223:218>	CMO23_3BLUT3_IN2	3-bit LUT3 IN2
<230:225>	CMO24_MF0_2BLUT0_DFF0_IN0_CLK	MF0(2-bit LUT0/DFF0/LATCH0) IN0/CLK/nL
<236:231>	CMO25_MF0_2BLUT0_DFF0_IN1_D	MF0(2-bit LUT0/DFF0/LATCH0) IN1/D
<242:237>	CMO26_MF1_2BLUT1_DFF1_IN0_CLK	MF1(2-bit LUT1/DFF1/LATCH1) IN0/CLK/nL
<248:243>	CMO27_MF1_2BLUT1_DFF1_IN1_D	MF1(2-bit LUT1/DFF1/LATCH1) IN1/D
<254:249>	CMO28_MF2_2BLUT2_DFF2_IN0_CLK	MF2(2-bit LUT2/DFF2/LATCH2) IN0/CLK/nL
<260:255>	CMO29_MF2_2BLUT2_DFF2_IN1_D	MF2(2-bit LUT2/DFF2/LATCH2) IN1/D
<266:261>	CMO30_MF3_2BLUT3_DFF3_IN0_CLK	MF3(2-bit LUT3/DFF3/LATCH3) IN0/CLK/nL
<272:267>	CMO31_MF3_2BLUT3_DFF3_IN1_D	MF3(2-bit LUT3/DFF3/LATCH3) IN1/D
<279:274>	CMO32_MF4_3BLUT4_DFF4_IN0_CLK	MF4(3-bit LUT4/DFF4/LATCH4) IN0/CLK/nL
<285:280>	CMO33_MF4_3BLUT4_DFF4_IN1_D	MF4(3-bit LUT4/DFF4/LATCH4) IN1/D
<291:286>	CMO34_MF4_3BLUT4_DFF4_IN2_RST	MF4(3-bit LUT4/DFF4/LATCH4) IN2/(n)RST/(n)SET
<297:292>	CMO35_MF5_3BLUT5_DFF5_IN0_CLK	MF5(3-bit LUT5/DFF5/LATCH5) IN0/CLK/nL
<303:298>	CMO36_MF5_3BLUT5_DFF5_IN1_D	MF5(3-bit LUT5/DFF5/LATCH5) IN1/D
<309:304>	CMO37_MF5_3BLUT5_DFF5_IN2_RST	MF5(3-bit LUT5/DFF5/LATCH5) IN2/(n)RST/(n)SET
<315:310>	CMO38_MF6_3BLUT6_DFF6_IN0_CLK	MF6(3-bit LUT6/DFF6/LATCH6) IN0/CLK/nL
<321:316>	CMO39_MF6_3BLUT6_DFF6_IN1_D	MF6(3-bit LUT6/DFF6/LATCH6) IN1/D
<327:322>	CMO40_MF6_3BLUT6_DFF6_IN2_RST	MF6(3-bit LUT6/DFF6/LATCH6) IN2/(n)RST/(n)SET
<333:328>	CMO41_MF7_3BLUT7_DFF7_IN0_CLK	MF7(3-bit LUT7/DFF7/LATCH7) IN0/CLK/nL
<339:334>	CMO42_MF7_3BLUT7_DFF7_IN1_D	MF7(3-bit LUT7/DFF7/LATCH7) IN1/D
<345:340>	CMO43_MF7_3BLUT7_DFF7_IN2_RST	MF7(3-bit LUT7/DFF7/LATCH7) IN2/(n)RST/(n)SET
<352:347>	CMO44_MF8_3BLUT8_SH_REG_IN0_CLK	MF8(3-bit LUT8/Shift Register) IN0/CLK
<358:353>	CMO45_MF8_3BLUT8_SH_REG_IN1_D	MF8(3-bit LUT8/Shift Register) IN1/D
<364:359>	CMO46_MF8_3BLUT8_SH_REG_IN2_nRST	MF8(3-bit LUT8/Shift Register) IN2/nRST
<370:365>	CMO47_MF9_3BLUT9_8BTMR1_IN2_CLK	MF9(3-bit LUT9/8-bit TMR1) IN2/CLK
<376:371>	CMO48_MF9_3BLUT9_8BTMR1_IN1_RST	MF9(3-bit LUT9/8-bit TMR1) IN1/IN/RST
<382:377>	CMO49_MF9_3BLUT9_8BTMR1_IN0_KEEP	MF9(3-bit LUT9/8-bit TMR1) IN0/KEEP
<389:384>	CMO50_MF10_4BLUT0_8BTMR2_IN0_CLK	MF10(4-bit LUT0/8-bit TMR2) IN0/CLK
<395:390>	CMO51_MF10_4BLUT0_8BTMR2_IN1_RST	MF10(4-bit LUT0/8-bit TMR2) IN1/IN/RST
<401:396>	CMO52_MF10_4BLUT0_8BTMR2_IN2_KEEP	MF10(4-bit LUT0/8-bit TMR2) IN2/KEEP
<407:402>	CMO53_MF10_4BLUT0_8BTMR2_IN3	MF10(4-bit LUT0/8-bit TMR2) IN3
<413:408>	CMO54_MF11_4BLUT1_8BTMR3_IN0_CLK	MF11(4-bit LUT1/8-bit TMR3) IN0/CLK
<419:414>	CMO55_MF11_4BLUT1_8BTMR3_IN1_RST	MF11(4-bit LUT1/8-bit TMR3) IN1/IN/RST
<425:420>	CMO56_MF11_4BLUT1_8BTMR3_IN2_KEEP	MF11(4-bit LUT1/8-bit TMR3) IN2/KEEP
<431:426>	CMO57_MF11_4BLUT1_8BTMR3_IN3	MF11(4-bit LUT1/8-bit TMR3) IN3
<438:433>	CMO58_MF12_PDLY_ED_IN	MF12(PDLY/Edge Detector) IN
<444:439>	CMO59_16BTMR0_CLK_KEEP	16-bit TMR0 CLK/KEEP
<450:445>	CMO60_16BTMR0_IN_RST	16-bit TMR0 IN/RST
<456:451>	CMO61_ACMP0_PWR_ON	ACMP0 PWR ON
<462:457>	CMO62_ACMP1_PWR_ON	ACMP1 PWR ON

7. Combinatorial Logic

Sixteen Look Up Tables (LUTs) within the ALM1412 provide the support for combinatorial logic. There are four 3-bit LUTs, and twelve Multifunctional Macrocells that can be used as LUTs. For more details, please see Section 8. Multifunctional Macrocells.

IOs for the four LUTs are configured from the connection matrix. The specific logic functions are defined by the state of the NVM bits.

7.1. 3-bit LUT

The four 3-bit LUTs take in three input signals, each from the connection matrix and produce a single output, and this output goes back into the connection matrix (Figure 7.1). The LUT allows the user to implement used-defined combinatorial logic functionss, including standard digital logic gates (AND, NAND, OR, NOR, XOR, XNOR). Standard logic gate configuration of the LUT is shown in the Table 7.1.

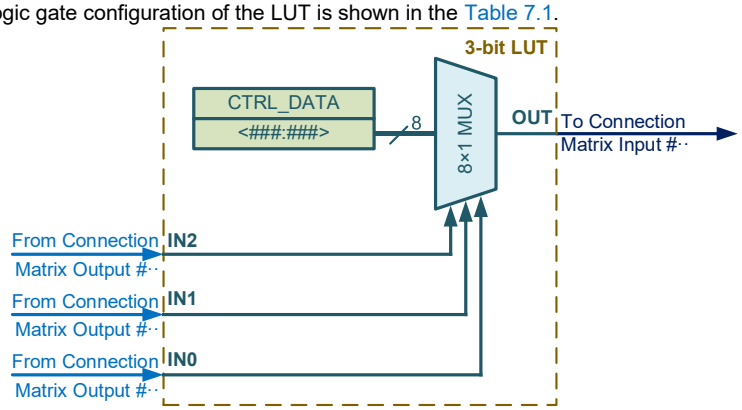


Figure 7.1. Schematic diagram of 3-bit LUT

Table 7.1. 3-bit LUT Truth Table of Standard Logic Gates

Function	MSB							LSB
AND-3	1	0	0	0	0	0	0	0
NAND-3	0	1	1	1	1	1	1	1
OR-3	1	1	1	1	1	1	1	0
NOR-3	0	0	0	0	0	0	0	1
XOR-3	1	0	0	1	0	1	1	0
XNOR-3	0	1	1	0	1	0	0	1

7.1.1. 3-bit LUT0

Registers of the 3-bit LUT0 macrocell are set out in Table 7.2.

Table 7.2. 3-bit LU0 Registers

Register Bit Address	Register Name	Register Definition
3-bit LUT0		
<582:575>	3BLUT0_CTRL_DATA	OUT LUT control data

The 3-bit LUT0 uses an 8-bit register to define its output function (Table 7.3).

Table 7.3. 3-bit LUT0 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	3BIT_LUT0_CTRL_DATA<0>	LSB
0	0	1	3BIT_LUT0_CTRL_DATA<1>	
0	1	0	3BIT_LUT0_CTRL_DATA<2>	
0	1	1	3BIT_LUT0_CTRL_DATA<3>	
1	0	0	3BIT_LUT0_CTRL_DATA<4>	
1	0	1	3BIT_LUT0_CTRL_DATA<5>	
1	1	0	3BIT_LUT0_CTRL_DATA<6>	
1	1	1	3BIT_LUT0_CTRL_DATA<7>	MSB

7.1.2. 3-bit LUT1

Registers of the 3-bit LUT1 macrocell are set out in Table 7.4.

Table 7.4. 3-bit LU1 Registers

Register Bit Address	Register Name	Register Definition
3-bit LUT1		
<590:583>	3BLUT1_CTRL_DATA	OUT LUT control data

The 3-bit LUT1 uses an 8-bit register to define its output function (Table 7.5).

Table 7.5. 3-bit LUT1 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	3BIT_LUT1_CTRL_DATA<0>	LSB
0	0	1	3BIT_LUT1_CTRL_DATA<1>	
0	1	0	3BIT_LUT1_CTRL_DATA<2>	
0	1	1	3BIT_LUT1_CTRL_DATA<3>	
1	0	0	3BIT_LUT1_CTRL_DATA<4>	
1	0	1	3BIT_LUT1_CTRL_DATA<5>	
1	1	0	3BIT_LUT1_CTRL_DATA<6>	
1	1	1	3BIT_LUT1_CTRL_DATA<7>	MSB

7.1.3. 3-bit LUT2

Registers of the 3-bit LUT2 macrocell are set out in Table 7.6.

Table 7.6. 3-bit LU2 Registers

Register Bit Address	Register Name	Register Definition
3-bit LUT2		
<598:591>	3BLUT2_CTRL_DATA	OUT LUT control data

The 3-bit LUT2 uses an 8-bit register to define its output function (Table 7.7).

Table 7.7. 3-bit LUT2 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	3BIT_LUT2_CTRL_DATA<0>	LSB
0	0	1	3BIT_LUT2_CTRL_DATA<1>	
0	1	0	3BIT_LUT2_CTRL_DATA<2>	
0	1	1	3BIT_LUT2_CTRL_DATA<3>	
1	0	0	3BIT_LUT2_CTRL_DATA<4>	
1	0	1	3BIT_LUT2_CTRL_DATA<5>	
1	1	0	3BIT_LUT2_CTRL_DATA<6>	
1	1	1	3BIT_LUT2_CTRL_DATA<7>	MSB

7.1.4. 3-bit LUT3

Registers of the 3-bit LUT3 macrocell are set out in Table 7.8.

Table 7.8. 3-bit LU3 Registers

Register Bit Address	Register Name	Register Definition
3-bit LUT3		
<606:599>	3BLUT3_CTRL_DATA	OUT LUT control data

The 3-bit LUT3 uses an 8-bit register to define its output function (Table 7.9).

Table 7.9. 3-bit LUT3 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	3BIT_LUT3_CTRL_DATA<0>	LSB
0	0	1	3BIT_LUT3_CTRL_DATA<1>	
0	1	0	3BIT_LUT3_CTRL_DATA<2>	
0	1	1	3BIT_LUT3_CTRL_DATA<3>	
1	0	0	3BIT_LUT3_CTRL_DATA<4>	
1	0	1	3BIT_LUT3_CTRL_DATA<5>	
1	1	0	3BIT_LUT3_CTRL_DATA<6>	
1	1	1	3BIT_LUT3_CTRL_DATA<7>	MSB

8. Multifunctional Macrocells

Thirteen multifunction macrocells (MF) in the ALM1412 can serve more than one logic or timing function. They can serve as a Look Up Table (LUT) or as another logic or timing function in eight of the cases. Functions that can be implemented in these macrocells are below:

- Four selectable 2-bit LUTs or DFF/LATCHs;
- Four selectable 3-bit LUTs or DFF/LATCHs;
- One selectable 3-bit LUT or 16-bit Shift Register;
- One Selectable 3-bit LUTs or 8-bit Timers (TMR);
- Two Selectable 4-bit LUTs or 8-bit Timers;
- One Programmable Delay or Edge Detector.

8.1. MF (2-bit LUT/DFF/LATCH) Macrocells

The ALM1412 has MF macrocells capable of serving as either 2-bit LUTs, DFFs, or LATCHs (see Figure 8.1).

When the MF macrocells are used as LUT, the 2-bit LUT takes in two input signals from the connection matrix and produces a single output that goes back into the connection matrix. The LUT allows the user to implement used-defined combinatorial logic functions, including standard digital logic gates (AND, NAND, OR, NOR, XOR, XNOR). Standard logic gate configurations of the LUT are shown in Table 8.1.

When the macrocells are used as DFF or LATCH, the two input signals from the connection matrix go to the data (D) and clock/nlatch (CLK/nL) inputs for the DFF/LATCH, and the output goes back to the connection matrix. Operations of the DFF and LATCH are shown in Table 8.2, Table 8.3.

Table 8.1. 2-bit LUT Truth Table of Standard Logic Gates

Function	MSB			LSB
AND-2	1	0	0	0
NAND-2	0	1	1	1
OR-2	1	1	1	0
NOR-2	0	0	0	1
XOR-2	0	1	1	0

Table 8.2. Operation of the DFF

nRST/nSET	D	CLK	Q(t)
1	0	↓	0/1
1	0	↑	t–1
1	1	↓	1/0
1	1	↑	t–1

Note 8.1: X – Don't Care
Note 8.2: t–1 – Previous State

Table 8.3. Operation of the LATCH

nRST/nSET	nL	D	Q(t)/nQ(t)
1	0	0	t–1
1	0	1	t–1
1	1	0	0/1
1	1	1	1/0

Note 8.3: X – Don't Care
Note 8.4: t–1 – Previous State

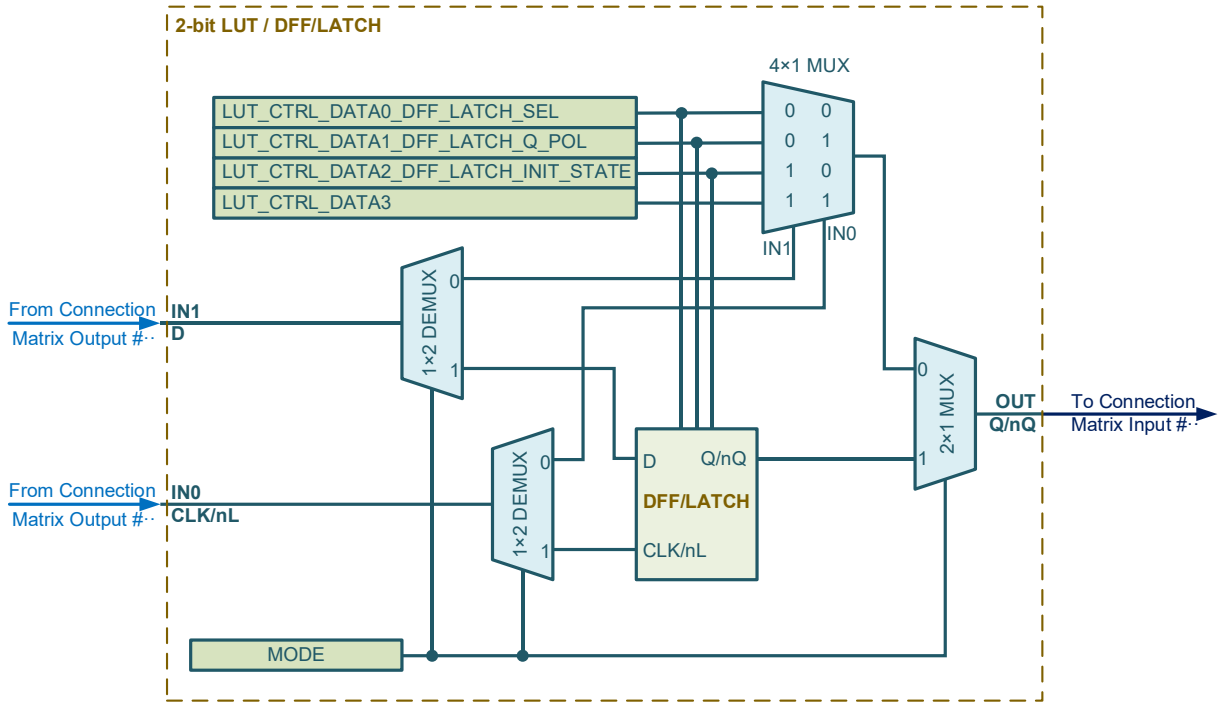


Figure 8.1. Schematic diagram of MF (2-bit LUT/DFF/LATCH)

8.1.1. MF0 (2-bit LUT0/DFF0/LATCH0) Macrocell

Registers of MF0 (2-bit LUT0/DFF0/LATCH0) macrocell are set out in Table 8.4.

Table 8.4. MF0(2-bit LUT0/DFF0/LATCH0) Registers

Register Bit Address	Register Name	Register Definition
MF0 (2-bit LUT0/DFF0/LATCH0)		
<613>	MF0_MODE	MF mode: 0: LUT 1: DFF/LATCH
<614>	MF0_LUT_CTRL_DATA0_DFF_LATCH_SEL	0th bit of LUT control data: 0: LOW 1: HIGH or DFF/LATCH selection: 0: DFF 1: LATCH
<615>	MF0_LUT_CTRL_DATA1_DFF_LATCH_Q_POL	1st bit of LUT control data: 0: LOW 1: HIGH or Q polarity of DFF/LATCH: 0: Q 1: nQ
<616>	MF0_LUT_CTRL_DATA2_DFF_LATCH_INIT_STATE	2nd bit of LUT control data: 0: LOW 1: HIGH or Initial state of DFF/LATCH: 0: LOW 1: HIGH
<617>	MF0_LUT_CTRL_DATA3	3rd bit of LUT control data: 0: LOW 1: HIGH

The MF0 (2-bit LUT0/DFF0/LATCH0) macrocell, if programmed for a LUT function, uses 4 bits to define its output function by MF0_1_CONF<3:0> (see Table 8.5).

Table 8.5. 2-bit LUT0 Truth Table

IN1	IN0	OUT	
0	0	MF0_LUT_CTRL_DATA0_DFF_LATCH_SEL	LSB
0	1	MF0_LUT_CTRL_DATA1_DFF_LATCH_Q_POL	
1	0	MF0_LUT_CTRL_DATA2_DFF_LATCH_INIT_STATE	
1	1	MF0_LUT_CTRL_DATA3	MSB

8.1.2. MF1 (2-bit LUT1/DFF1/LATCH1) Macrocell

Registers of MF1 (2-bit LUT1/DFF1/LATCH1) macrocell are set out in Table 8.6.

Table 8.6. MF1(2-bit LUT0/DFF0/LATCH0) Registers

Register Bit Address	Register Name	Register Definition
MF1 (2-bit LUT1/DFF1/LATCH1)		
<619>	MF1_MODE	MF mode: 0: LUT 1: DFF/LATCH
<620>	MF1_LUT_CTRL_DATA0_DFF_LATCH_SEL	0th bit of LUT control data: 0: LOW 1: HIGH or DFF/LATCH selection: 0: DFF 1: LATCH
<621>	MF1_LUT_CTRL_DATA1_DFF_LATCH_Q_POL	1st bit of LUT control data: 0: LOW 1: HIGH or Q polarity of DFF/LATCH: 0: Q 1: nQ
<622>	MF1_LUT_CTRL_DATA2_DFF_LATCH_INIT_STATE	2nd bit of LUT control data: 0: LOW 1: HIGH or Initial state of DFF/LATCH: 0: LOW 1: HIGH
<623>	MF1_LUT_CTRL_DATA3	3rd bit of LUT control data: 0: LOW 1: HIGH

The MF1 (2-bit LUT1/DFF1/LATCH1) macrocell, if programmed for a LUT function, uses 4 bits to define its output function by MF0_1_CONF<7:4> (see Table 8.7).

Table 8.7. 2-bit LUT1 Truth Table

IN1	IN0	OUT	
0	0	MF1_LUT_CTRL_DATA0_DFF_LATCH_SEL	LSB
0	1	MF1_LUT_CTRL_DATA1_DFF_LATCH_Q_POL	
1	0	MF1_LUT_CTRL_DATA2_DFF_LATCH_INIT_STATE	
1	1	MF1_LUT_CTRL_DATA3	MSB

8.1.3. MF2 (2-bit LUT2/DFF2/LATCH2) Macrocell

Registers of MF2 (2-bit LUT2/DFF2/LATCH2) macrocell are set out in Table 8.8.

Table 8.8. 2-bit LUT2/DFF2/LATCH2 Registers

Register Bit Address	Register Name	Register Definition
MF2 (2-bit LUT2/DFF2/LATCH2)		
<624>	MF2_MODE	MF mode: 0: LUT 1: DFF/LATCH
<625>	MF2_LUT_CTRL_DATA0_DFF_LATCH_SEL	0th bit of LUT control data: 0: LOW 1: HIGH or DFF/LATCH selection: 0: DFF 1: LATCH
<626>	MF2_LUT_CTRL_DATA1_DFF_LATCH_Q_POL	1st bit of LUT control data: 0: LOW 1: HIGH or Q polarity of DFF/LATCH: 0: Q 1: nQ
<627>	MF2_LUT_CTRL_DATA2_DFF_LATCH_INIT_STATE	2nd bit of LUT control data: 0: LOW 1: HIGH or Initial state of DFF/LATCH: 0: LOW 1: HIGH
<628>	MF2_LUT_CTRL_DATA3	3rd bit of LUT control data: 0: LOW 1: HIGH

The MF2 (2-bit LUT2/DFF2/LATCH2) macrocell, if programmed for a LUT function, uses 4 bits to define its output function by MF2_3_CONF<3:0> (see Table 8.9).

Table 8.9. 2-bit LUT2 Truth Table

IN1	IN0	OUT	
0	0	MF2_LUT_CTRL_DATA0_DFF_LATCH_SEL	LSB
0	1	MF2_LUT_CTRL_DATA1_DFF_LATCH_Q_POL	
1	0	MF2_LUT_CTRL_DATA2_DFF_LATCH_INIT_STATE	
1	1	MF2_LUT_CTRL_DATA3	MSB

8.1.4. MF3 (2-bit LUT3/DFF3/LATCH3) Macrocell

Registers of MF3 (2-bit LUT3/DFF3/LATCH3) macrocell are set out in Table 8.10.

Table 8.10. 2-bit LUT3/DFF3/LATCH3 Registers

Register Bit Address	Register Name	Register Definition
MF3 (2-bit LUT3/DFF3/LATCH3)		
<630>	MF3_MODE	MF mode: 0: LUT 1: DFF/LATCH
<631>	MF3_LUT_CTRL_DATA0_DFF_LATCH_SEL	0th bit of LUT control data: 0: LOW 1: HIGH or DFF/LATCH selection: 0: DFF 1: LATCH
<632>	MF3_LUT_CTRL_DATA1_DFF_LATCH_Q_POL	1st bit of LUT control data: 0: LOW 1: HIGH or Q polarity of DFF/LATCH: 0: Q 1: nQ
<633>	MF3_LUT_CTRL_DATA2_DFF_LATCH_INIT_STATE	2nd bit of LUT control data: 0: LOW 1: HIGH or Initial state of DFF/LATCH: 0: LOW 1: HIGH
<634>	MF3_LUT_CTRL_DATA3	3rd bit of LUT control data: 0: LOW 1: HIGH

The MF3 (2-bit LUT3/DFF3/LATCH3) macrocell, if programmed for a LUT function, uses 4 bits to define its output function by MF2_3_CONF<7:4> (see Table 8.11).

Table 8.11. 2-bit LUT3 Truth Table

IN1	IN0	OUT	
0	0	MF3_LUT_CTRL_DATA0_DFF_LATCH_SEL	LSB
0	1	MF3_LUT_CTRL_DATA1_DFF_LATCH_Q_POL	
1	0	MF3_LUT_CTRL_DATA2_DFF_LATCH_INIT_STATE	
1	1	MF3_LUT_CTRL_DATA3	MSB

8.2. MF (3-bit LUT/DFF/LATCH) Macrocells

The ALM1412 has MF macrocells that can serve as either 3-bit LUTs or as DFF/LATCHs.

When the MF macrocells are used as LUT, the 3-bit LUT takes in three input signals from the connection matrix and produces a single output that goes back into the connection matrix. The LUT allows the user to implement used-defined combinatorial logic functions, including standard digital logic gates (AND, NAND, OR, NOR, XOR, XNOR). Standard logic gate configurations of the LUT are shown in Table 8.12.

When the macrocells are used as DFF or LATCH, the three input signals from the connection matrix go to the data (D), clock/nlatch (CLK/nL) and (n)RST/(n)SET inputs of the DFF/LATCH, and the output goes back to the connection matrix. Operations of the DFF and LATCH are shown in Table 8.13, Table 8.14.

Table 8.12. 3-bit LUT Truth Table of Standard Logic Gates

Function	MSB							LSB
AND-3	1	0	0	0	0	0	0	0
NAND-3	0	1	1	1	1	1	1	1
OR-3	1	1	1	1	1	1	1	0
NOR-3	0	0	0	0	0	0	0	1
XOR-3	1	0	0	1	0	1	1	0
XNOR-3	0	1	1	0	1	0	0	1

Table 8.13. Operation of the DFF

nRST/nSET	D	CLK	Q(t)
nRST = 0	X	X	0/1
nSET = 0	X	X	1/0
1	0	↓	0/1
1	0	↑	t–1
1	1	↓	1/0
1	1	↑	t–1

Note 8.5: X – Don't Care
Note 8.6: t–1 – Previous State

Table 8.14. Operation of the LATCH

nRST/nSET	nL	D	Q(t)/nQ(t)
nRST = 0	X	X	0/1
nSET = 0	X	X	1/0
1	0	0	t–1
1	0	1	t–1
1	1	0	0/1
1	1	1	1/0

Note 8.7: X – Don't Care
Note 8.8: t–1 – Previous State

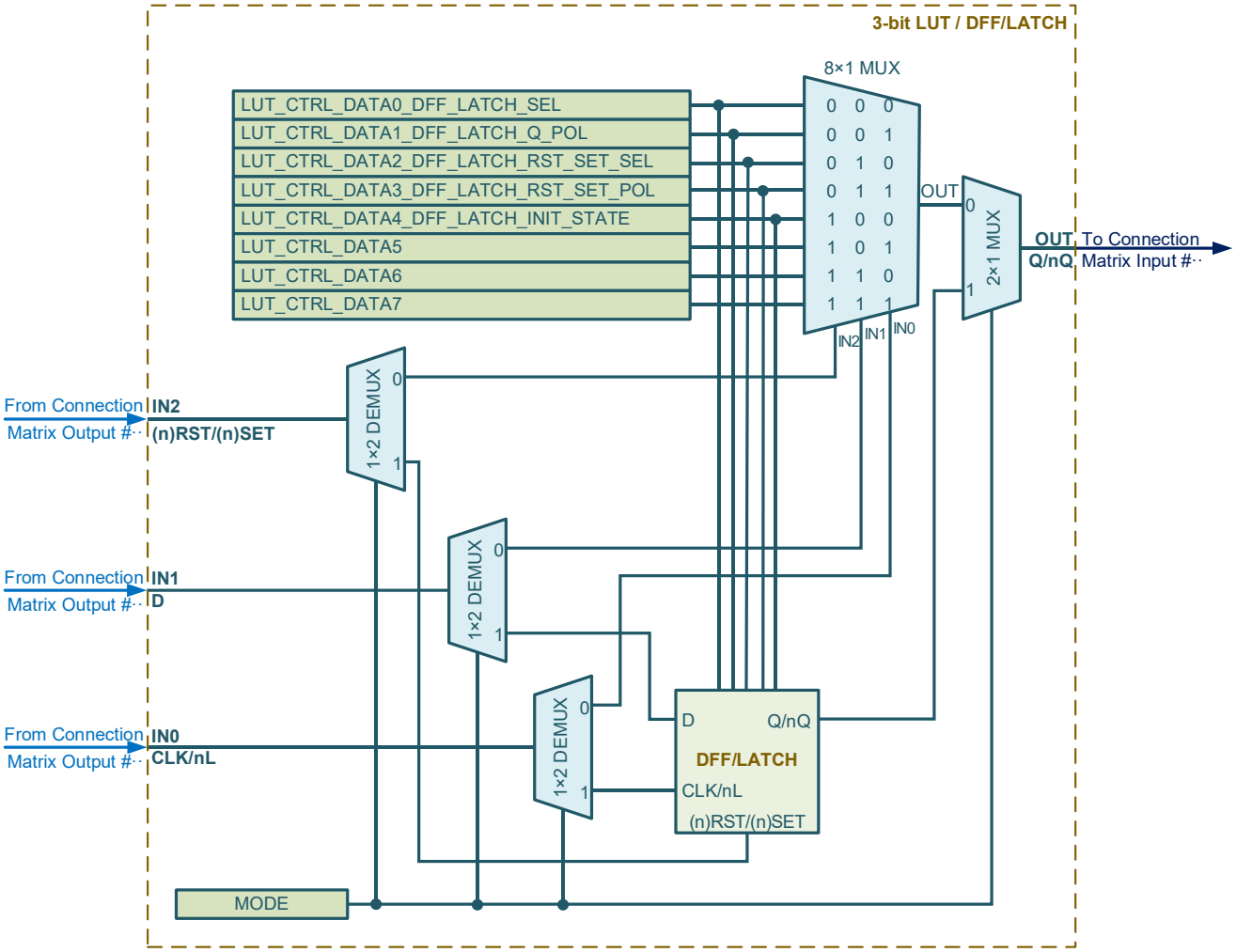


Figure 8.2. Schematic diagram of MF (3-bit LUT/DFF/LATCH)

8.2.1. MF4 (3-bit LUT4/DFF4/LATCH4)

Settings of MF4 (3-bit LUT4/DFF4/LATCH4) is shown in Table 8.15.

Table 8.15. 3-bit LUT4/DFF4/LATCH4 Registers

Register Bit Address	Register Name	Register Definition
MF4 (3-bit LUT4/DFF4/LATCH4)		
<636>	MF4_MODE	MF mode: 0: LUT 1: DFF/LATCH
<637>	MF4_LUT_CTRL_DATA0_DFF_LATCH_SEL	0th bit of LUT control data: 0: LOW 1: HIGH or DFF/LATCH selection: 0: DFF 1: LATCH
<638>	MF4_LUT_CTRL_DATA1_DFF_LATCH_Q_POL	1st bit of LUT control data: 0: LOW 1: HIGH or Q polarity of DFF/LATCH: 0: Q 1: nQ
<639>	MF4_LUT_CTRL_DATA2_DFF_LATCH_RST_SET_SEL	2nd bit of LUT control data: 0: LOW 1: HIGH or reset/set selection: 0: (n)RST 1: (n)SET
<640>	MF4_LUT_CTRL_DATA3_DFF_LATCH_RST_SET_POL	3rd bit of LUT control data: 0: LOW 1: HIGH or reset/set polarity: 0: nRST(nSET) 1: RST(SET)
<641>	MF4_LUT_CTRL_DATA4_DFF_LATCH_INIT_STATE	4th bit of LUT control data: 0: LOW 1: HIGH or Initial state of DFF/LATCH: 0: LOW 1: HIGH
<642>	MF4_LUT_CTRL_DATA_5	5th bit of LUT control data: 0: LOW 1: HIGH
<643>	MF4_LUT_CTRL_DATA_6	6th bit of LUT control data: 0: LOW 1: HIGH
<644>	MF4_LUT_CTRL_DATA_7	7th bit of LUT control data: 0: LOW 1: HIGH

The 3-bit LUT4 uses an 8-bit register to define its output function (see Table 8.16).

Table 8.16. 3-bit LUT4 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	MF4_LUT_CTRL_DATA0_DFF_LATCH_SEL	LSB
0	0	1	MF4_LUT_CTRL_DATA1_DFF_LATCH_Q_POL	
0	1	0	MF4_LUT_CTRL_DATA2_DFF_LATCH_RST_SET_SEL	
0	1	1	MF4_LUT_CTRL_DATA3_DFF_LATCH_RST_SET_POL	
1	0	0	MF4_LUT_CTRL_DATA4_DFF_LATCH_INIT_STATE	
1	0	1	MF4_LUT_CTRL_DATA_5	
1	1	0	MF4_LUT_CTRL_DATA_6	
1	1	1	MF4_LUT_CTRL_DATA_7	MSB

8.2.2. MF5 (3-bit LUT5/DFF5/LATCH5)

Settings of MF5 (3-bit LUT5/DFF5/LATCH5) is shown in Table 8.17.

Table 8.17. MF5 (3-bit LUT5/DFF5/LATCH5) Registers

Register Bit Address	Register Name	Register Definition
MF5 (3-bit LUT5/DFF5/LATCH5)		
<646>	MF5_MODE	MF mode: 0: LUT 1: DFF/LATCH
<647>	MF5_LUT_CTRL_DATA0_DFF_LATCH_SEL	0th bit of LUT control data: 0: LOW 1: HIGH or DFF/LATCH selection: 0: DFF 1: LATCH
<648>	MF5_LUT_CTRL_DATA1_DFF_LATCH_Q_POL	1st bit of LUT control data: 0: LOW 1: HIGH or Q polarity of DFF/LATCH: 0: Q 1: nQ
<649>	MF5_LUT_CTRL_DATA2_DFF_LATCH_RST_SET_SEL	2nd bit of LUT control data: 0: LOW 1: HIGH or reset/set selection: 0: (n)RST 1: (n)SET
<650>	MF5_LUT_CTRL_DATA3_DFF_LATCH_RST_SET_POL	3rd bit of LUT control data: 0: LOW 1: HIGH or reset/set polarity: 0: nRST(nSET) 1: RST(SET)
<651>	MF5_LUT_CTRL_DATA4_DFF_LATCH_INIT_STATE	4th bit of LUT control data: 0: LOW 1: HIGH or Initial state of DFF/LATCH: 0: LOW 1: HIGH
<652>	MF5_LUT_CTRL_DATA_5	5th bit of LUT control data: 0: LOW 1: HIGH
<653>	MF5_LUT_CTRL_DATA_6	6th bit of LUT control data: 0: LOW 1: HIGH
<654>	MF5_LUT_CTRL_DATA_7	7th bit of LUT control data: 0: LOW 1: HIGH

The 3-bit LUT5 uses an 8-bit register to define its output function (see Table 8.18).

Table 8.18. 3-bit LUT5 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	MF5_LUT_CTRL_DATA0_DFF_LATCH_SEL	LSB
0	0	1	MF5_LUT_CTRL_DATA1_DFF_LATCH_Q_POL	
0	1	0	MF5_LUT_CTRL_DATA2_DFF_LATCH_RST_SET_SEL	
0	1	1	MF5_LUT_CTRL_DATA3_DFF_LATCH_RST_SET_POL	
1	0	0	MF5_LUT_CTRL_DATA4_DFF_LATCH_INIT_STATE	
1	0	1	MF5_LUT_CTRL_DATA_5	
1	1	0	MF5_LUT_CTRL_DATA_6	
1	1	1	MF5_LUT_CTRL_DATA_7	MSB

8.2.3. MF6 (3-bit LUT6/DFF6/LATCH6)

Settings of MF6 (3-bit LUT6/DFF6/LATCH6) is shown in Table 8.19.

Table 8.19. 3-bit LUT6/DFF6/LATCH6 Registers

Register Bit Address	Register Name	Register Definition
MF6 (3-bit LUT6/DFF6/LATCH6)		
<656>	MF6_MODE	MF mode: 0: LUT 1: DFF/LATCH
<657>	MF6_LUT_CTRL_DATA0_DFF_LATCH_SEL	0th bit of LUT control data: 0: LOW 1: HIGH or DFF/LATCH selection: 0: DFF 1: LATCH
<658>	MF6_LUT_CTRL_DATA1_DFF_LATCH_Q_POL	1st bit of LUT control data: 0: LOW 1: HIGH or Q polarity of DFF/LATCH: 0: Q 1: nQ
<659>	MF6_LUT_CTRL_DATA2_DFF_LATCH_RST_SET_SEL	2nd bit of LUT control data: 0: LOW 1: HIGH or reset/set selection: 0: (n)RST 1: (n)SET
<660>	MF6_LUT_CTRL_DATA3_DFF_LATCH_RST_SET_POL	3rd bit of LUT control data: 0: LOW 1: HIGH or reset/set polarity: 0: nRST(nSET) 1: RST(SET)
<661>	MF6_LUT_CTRL_DATA4_DFF_LATCH_INIT_STATE	4th bit of LUT control data: 0: LOW 1: HIGH or Initial state of DFF/LATCH: 0: LOW 1: HIGH
<662>	MF6_LUT_CTRL_DATA_5	5th bit of LUT control data: 0: LOW 1: HIGH
<663>	MF6_LUT_CTRL_DATA_6	6th bit of LUT control data: 0: LOW 1: HIGH
<664>	MF6_LUT_CTRL_DATA_7	7th bit of LUT control data: 0: LOW 1: HIGH

The 3-bit LUT6 uses an 8-bit register to define its output function (see Table 8.20).

Table 8.20. 3-bit LUT6 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	MF6_LUT_CTRL_DATA0_DFF_LATCH_SEL	LSB
0	0	1	MF6_LUT_CTRL_DATA1_DFF_LATCH_Q_POL	
0	1	0	MF6_LUT_CTRL_DATA2_DFF_LATCH_RST_SET_SEL	
0	1	1	MF6_LUT_CTRL_DATA3_DFF_LATCH_RST_SET_POL	
1	0	0	MF6_LUT_CTRL_DATA4_DFF_LATCH_INIT_STATE	
1	0	1	MF6_LUT_CTRL_DATA_5	
1	1	0	MF6_LUT_CTRL_DATA_6	
1	1	1	MF6_LUT_CTRL_DATA_7	MSB

8.2.4. MF7 (3-bit LUT7/DFF7/LATCH7)

Settings of MF7 (3-bit LUT7/DFF7/LATCH7) is shown in Table 8.21.

Table 8.21. MF7 (3-bit LUT7/DFF7/LATCH7) Registers

Register Bit Address	Register Name	Register Definition
MF7 (3-bit LUT7/DFF7/LATCH7)		
<666>	MF7_MODE	MF mode: 0: LUT 1: DFF/LATCH
<667>	MF7_LUT_CTRL_DATA0_DFF_LATCH_SEL	0th bit of LUT control data: 0: LOW 1: HIGH or DFF/LATCH selection: 0: DFF 1: LATCH
<668>	MF7_LUT_CTRL_DATA1_DFF_LATCH_Q_POL	1st bit of LUT control data: 0: LOW 1: HIGH or Q polarity of DFF/LATCH: 0: Q 1: nQ
<669>	MF7_LUT_CTRL_DATA2_DFF_LATCH_RST_SET_SEL	2nd bit of LUT control data: 0: LOW 1: HIGH or reset/set selection: 0: (n)RST 1: (n)SET
<670>	MF7_LUT_CTRL_DATA3_DFF_LATCH_RST_SET_POL	3rd bit of LUT control data: 0: LOW 1: HIGH or reset/set polarity: 0: nRST(nSET) 1: RST(SET)
<671>	MF7_LUT_CTRL_DATA4_DFF_LATCH_INIT_STATE	4th bit of LUT control data: 0: LOW 1: HIGH or Initial state of DFF/LATCH: 0: LOW 1: HIGH
<672>	MF7_LUT_CTRL_DATA_5	5th bit of LUT control data: 0: LOW 1: HIGH
<673>	MF7_LUT_CTRL_DATA_6	6th bit of LUT control data: 0: LOW 1: HIGH
<674>	MF7_LUT_CTRL_DATA_7	7th bit of LUT control data: 0: LOW 1: HIGH

The 3-bit LUT7 uses an 8-bit register to define its output function (see Table 8.22).

Table 8.22. 3-bit LUT7 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	MF7_LUT_CTRL_DATA0_DFF_LATCH_SEL	LSB
0	0	1	MF7_LUT_CTRL_DATA1_DFF_LATCH_Q_POL	
0	1	0	MF7_LUT_CTRL_DATA2_DFF_LATCH_RST_SET_SEL	
0	1	1	MF7_LUT_CTRL_DATA3_DFF_LATCH_RST_SET_POL	
1	0	0	MF7_LUT_CTRL_DATA4_DFF_LATCH_INIT_STATE	
1	0	1	MF7_LUT_CTRL_DATA_5	
1	1	0	MF7_LUT_CTRL_DATA_6	
1	1	1	MF7_LUT_CTRL_DATA_7	MSB

8.3. MF (3-bit LUT/Shift Register) Macrocell

The MF macrocell has a capability to serve as either a 3-bit LUT or as a Shift Register (SHR).

When the MF macrocell is used as LUT, the 3-bit LUT takes three input signals from the connection matrix and produces three outputs that go back into the connection matrix. The LUT allows the user to implement used-defined combinatorial logic functions, including standard digital logic gates (AND, NAND, OR, NOR, XOR, XNOR). Standard logic gate configurations of the LUT are shown in Table 8.23.

The Shift Register contains sixteen stages of cascading, positive-edge triggered DFFs. The signal from any stage can be routed to OUT0 and OUT1 independently. The Q[1] output is always connected to the output of the first stage. The Shift Register has Data (D), Clock (CLK), and Reset (nRST) inputs from the connection matrix. Applying a low-level signal to the nRST sets all stage values to zero.

The schematic diagram of the 3-bit LUT/Shift Register macrocell is shown in Figure 8.3.

Table 8.23. 3-bit LUT Truth Table of Standard Logic Gates

Function	MSB							LSB
AND-3	1	0	0	0	0	0	0	0
NAND-3	0	1	1	1	1	1	1	1
OR-3	1	1	1	1	1	1	1	0
NOR-3	0	0	0	0	0	0	0	1
XOR-3	1	0	0	1	0	1	1	0
XNOR-3	0	1	1	0	1	0	0	1

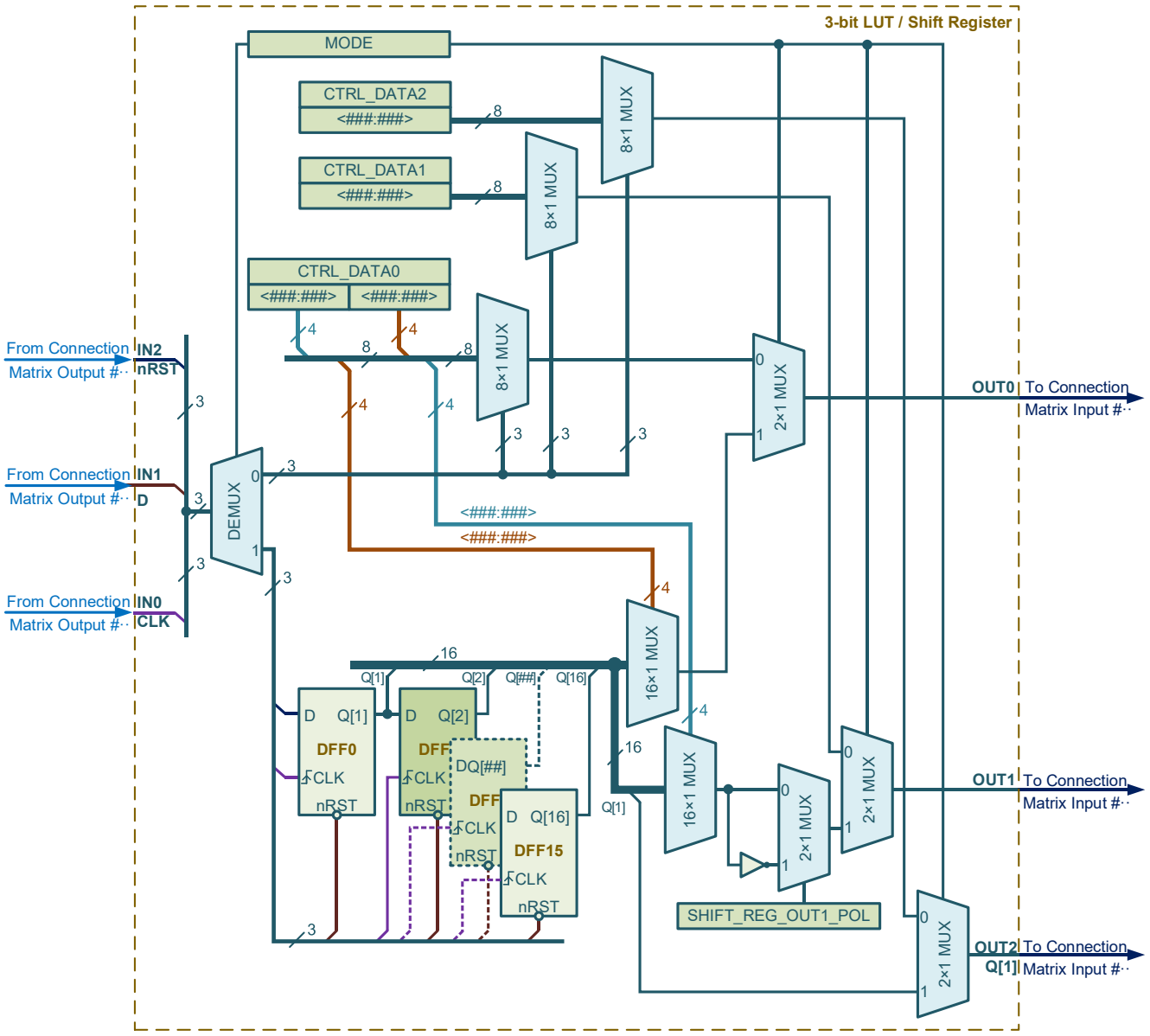


Figure 8.3. Schematic diagram of MF (3-bit LUT/Shift Regsiter)

8.3.1. MF8 (3-bit LUT8/Shift Register) Macrocell

Settings of MF8 (3-bit LUT8/Shift Register) are shown in Table 8.24.

Table 8.24. MF8 (3-bit LUT8/Shift Register) Registers

Register Bit Address	Register Name	Register Definition
MF8 (3-bit LUT8/Shift Register)		
<676>	MF8_MODE	MF mode: 0: LUT 1: Shift register
<677>	MF8_SHIFT_REG_OUT1_POL	Shift register OUT1 polarity: 0: OUT1 1: nOUT1
<681:678>	MF8_LUT_CTRL_DATA3_0_SHIFT_REG_STAGE_OUT0	Low tetrad of OUT0 LUT control data or stage of OUT0 shift register
<685:682>	MF8_LUT_CTRL_DATA7_4_SHIFT_REG_STAGE_OUT1	High tetrad of OUT0 LUT control data or stage of OUT1 shift register
<693:686>	MF8_CTRL_DATA1	OUT1 LUT control data
<701:694>	MF8_CTRL_DATA2	OUT2 LUT control data

The 3-bit LUT8 uses three 8-bit registers to define its outputs function (see Table 8.25).

Table 8.25. 3-bit LUT8 Truth Table

IN2	IN1	IN0	OUT0	OUT1	OUT2	
0	0	0	MF8_LUT_CTRL_DATA3_0_SHIFT_REG_STAGE_OUT0<0>	MF8_CTRL_DATA1<0>	MF8_CTRL_DATA2<0>	LSB
0	0	1	MF8_LUT_CTRL_DATA3_0_SHIFT_REG_STAGE_OUT0<1>	MF8_CTRL_DATA1<1>	MF8_CTRL_DATA2<1>	
0	1	0	MF8_LUT_CTRL_DATA3_0_SHIFT_REG_STAGE_OUT0<2>	MF8_CTRL_DATA1<2>	MF8_CTRL_DATA2<2>	
0	1	1	MF8_LUT_CTRL_DATA3_0_SHIFT_REG_STAGE_OUT0<3>	MF8_CTRL_DATA1<3>	MF8_CTRL_DATA2<3>	
1	0	0	MF8_LUT_CTRL_DATA7_4_SHIFT_REG_STAGE_OUT1<0>	MF8_CTRL_DATA1<4>	MF8_CTRL_DATA2<4>	
1	0	1	MF8_LUT_CTRL_DATA7_4_SHIFT_REG_STAGE_OUT1<1>	MF8_CTRL_DATA1<5>	MF8_CTRL_DATA2<5>	
1	1	0	MF8_LUT_CTRL_DATA7_4_SHIFT_REG_STAGE_OUT1<2>	MF8_CTRL_DATA1<6>	MF8_CTRL_DATA2<6>	
1	1	1	MF8_LUT_CTRL_DATA7_4_SHIFT_REG_STAGE_OUT1<3>	MF8_CTRL_DATA1<7>	MF8_CTRL_DATA2<7>	MSB

8.4. MF (3-bit LUT/8-bit TMR) Macrocell

One macrocell has the capability to serve as either a 3-bit LUTs or as an 8-bit timer (TMR). Schematic diagram of the macrocell is shown in Figure 8.4.

When the MF macrocells are used as LUT, the 3-bit LUT takes in three input signals from the connection matrix and produces a single output that goes back into the connection matrix. The LUT allows the user to implement used-defined combinatorial logic functions, including standard digital logic gates (AND, NAND, OR, NOR, XOR, XNOR). Standard logic gate configurations of the LUT are shown in Table 8.26.

When the macrocells are used as 8-bit TMR function, the three input signals from the connection matrix go to the EXTCLK, IN(RST for Counter mode) and KEEP inputs of the 8-bit TMR, and the output goes back to the connection matrix.

Each timer has the following mode of operation:

- Delay
- Counter
- One Shot
- Frequency Detector
- Delayed Edge Detector
- Edge Detector

The output polarity of the TMR is configurable and can be selected as non-inverted or inverted.

The KEEP input allows the user to pause counting by applying HIGH level to KEEP. Counting is resumed after KEEP goes LOW (Figure 8.11).

In Delay mode, the TMR delays the input signal by the selected edge event (rising edge, falling edge, both edges) for a time determined by the Control Data, input clock signal, and selected prescaler value. If input signal is shorter than the delay value, the signal does not propagate to the output. The timing diagrams of this mode are shown in the Figure 8.5.

In Counter mode, the TMR divides input clock signal by the value determined by the Control Data, input clock signal, and selected prescaler value. The output of the TMR goes HIGH every time when the Counted Value (current value of the counter) is equal 0. The RST of the TMR reset Counted value to 0 by one of the following events: rising edge, falling edge, both edges, high level. The timing diagrams of this mode are shown in the Figure 8.6.

In One-Shot mode, this macrocell generates a high-level pulse with a set width when detecting the edge event, which is selectable by the registers on its IN input. The pulse width is determined by the Control Data, input clock signal, and selected prescaler value. Any incoming edges are ignored during pulse width generation. The timing diagrams of this mode are shown in the Figure 8.7.

In Frequency Detector mode, the TMR functions are seen below in the following scenarios:

- Rising Edge: The output will go HIGH if the time between the two rising edges is less than the delay.
  The output will go LOW if the next rising edge has not come after the last rising edge in specified time.
- Falling Edge: The output will go HIGH if the time between two falling edges is less than the set time.
  The output will go LOW if the next falling edge has not come after the last falling edge in specified time.
- Both Edges: The output will go HIGH if the time between the rising and falling edges is less than the set time, which is equivalent to the length of the pulse.
  The output will go LOW if the next rising/falling edge has not come after the last falling/rising edge in specified time.

The timing diagrams of the Frequency Detector Mode are shown in the Figure 8.8.

In the Delayed Edge Detector mode, the TMR generates delayed short high-level pulse (for non-inverted polarity) when detecting the respective selected edge event (rising edge, falling edge, both edges). The delay time is determined by the Control Data, input clock signal, and selected prescaler value. The timing diagrams of this mode are shown in the Figure 8.9.

In Edge Detector mode, the TMR generates short high-level pulse (for non-inverted polarity) when detecting the respective selected edge event (rising edge, falling edge, both edges). The timing diagrams of this mode are shown in the Figure 8.10.

Time of Timers for each mode can be calculated using the following formulas (Note 8.9, Note 8.10):

- Delay (Figure 8.5)
  Delay Time = (Control Data + 1 + VAR)/F_{CLK};
- Counter (Figure 8.6)
  Output Period = (Control Data + 1)/F_{CLK};
  Output Frequency = F_{CLK}/(Control Data + 1);
- One Shot (Figure 8.7)
  Pulse width = (Control Data + 1 + VAR)/F_{CLK};
- Frequency Detector (Figure 8.8)
  Detected Frequency = F_{CLK}/(Control Data + 1 + VAR);
- Delayed Edge Detector (Figure 8.9)
  Delay Time = (Control Data + 1 + VAR)/F_{CLK}.

Note 8.9 *F_{CLK} – CLK input frequency.*

Note 8.10 *VAR = 0…1 – defined by the asynchronous time between the input signal and the first clock pulse.*

Note 8.11 *Counters initialize with Control Data after POR.*

Each TMR has a configuration bit that can be enabled to force OSC by the TMR when it is required to perform its function.

Table 8.26. 3-bit LUT Truth Table of Standard Logic Gates

Function	MSB							LSB
AND-3	1	0	0	0	0	0	0	0
NAND-3	0	1	1	1	1	1	1	1
OR-3	1	1	1	1	1	1	1	0
NOR-3	0	0	0	0	0	0	0	1
XOR-3	1	0	0	1	0	1	1	0
XNOR-3	0	1	1	0	1	0	0	1

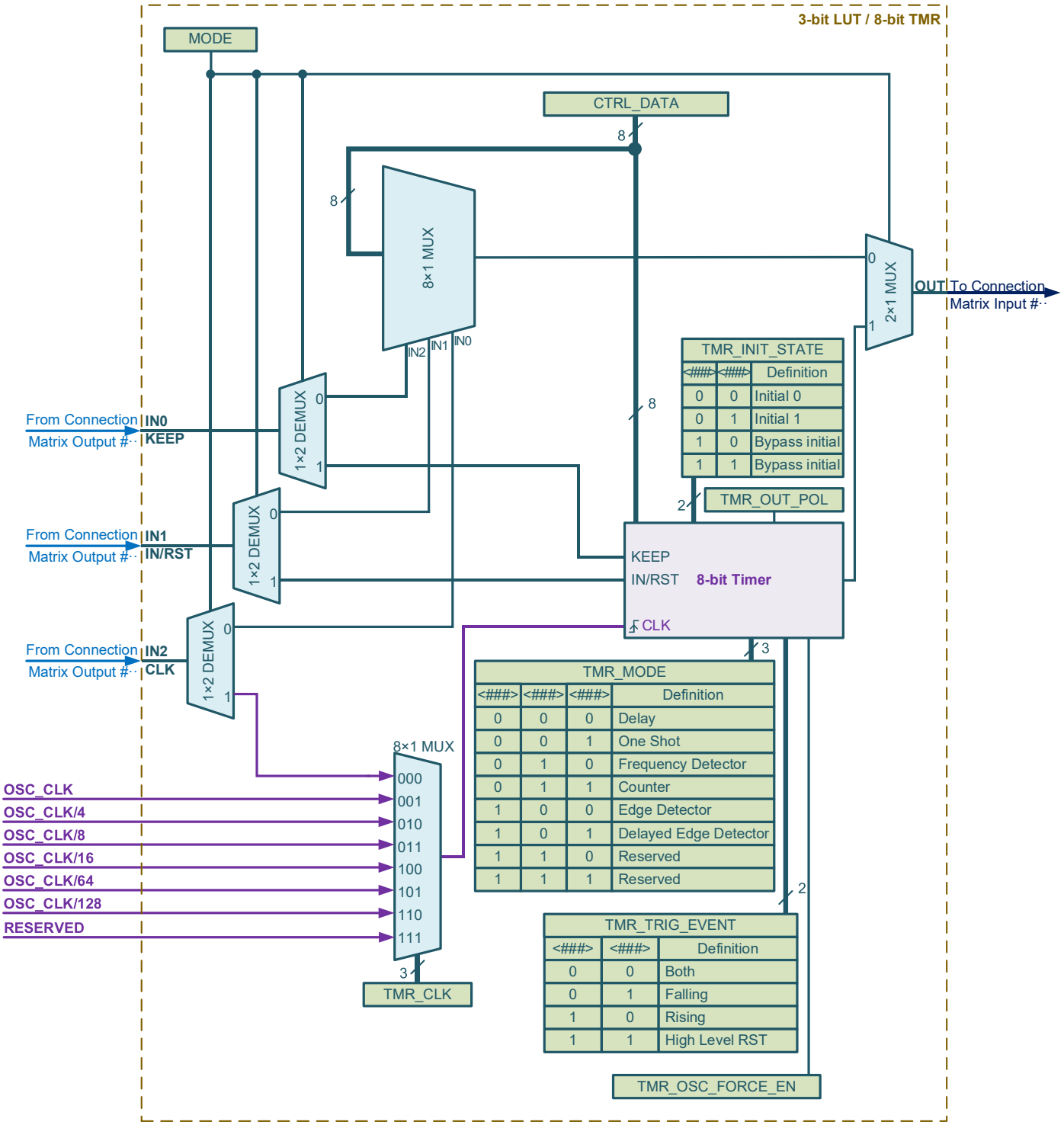
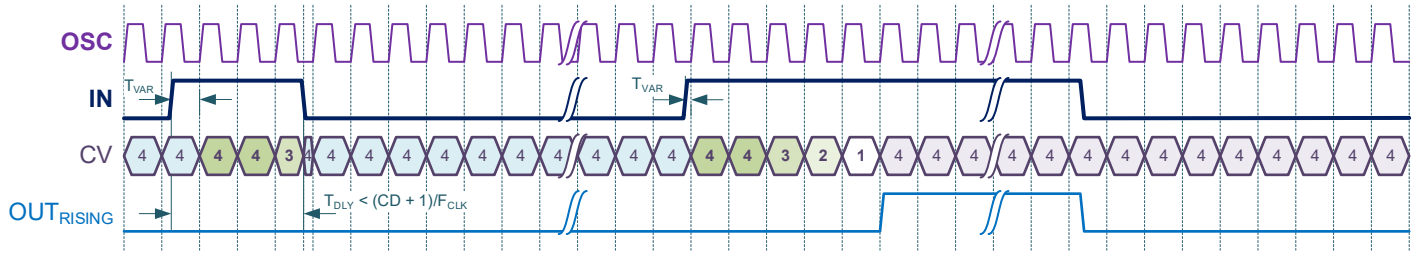
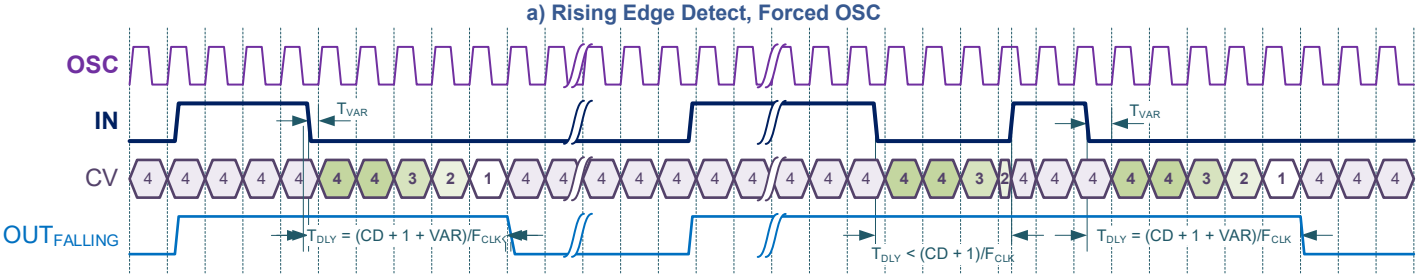


Figure 8.4. MF (3-bit LUT/8-bit TMR)

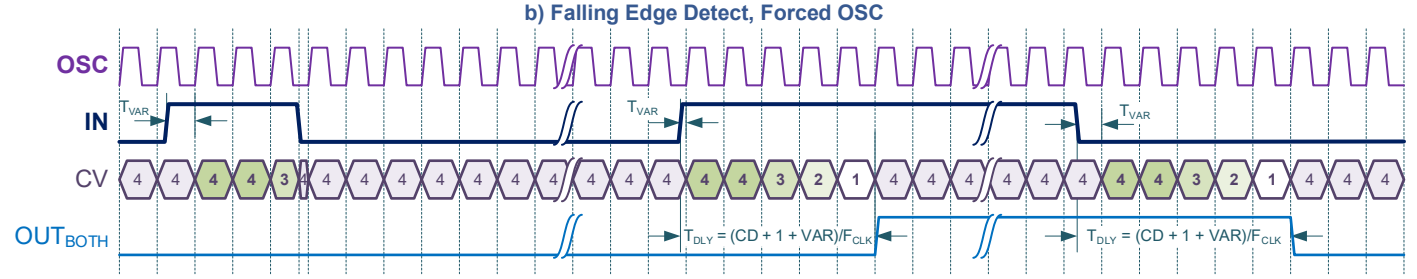
8.4.1. TMR Timing Diagrams



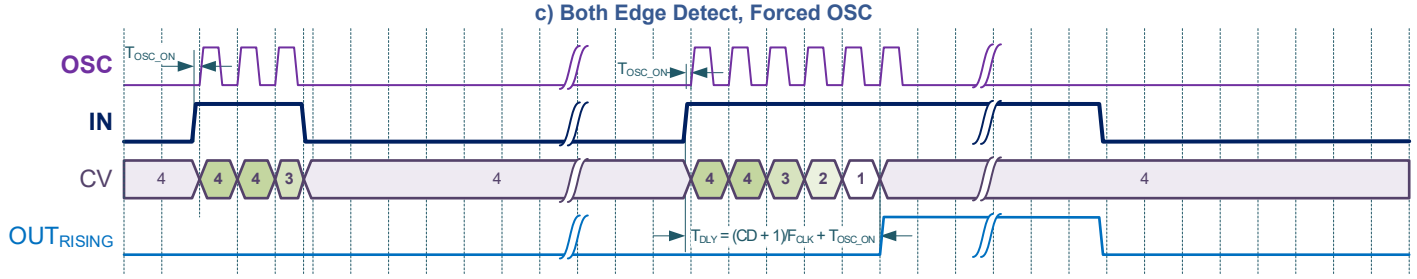
a) Rising Edge Detect, Forced OSC



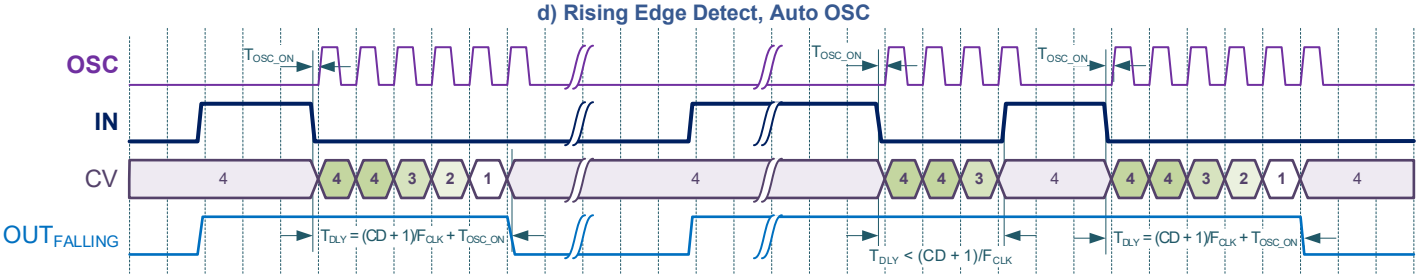
b) Falling Edge Detect, Forced OSC



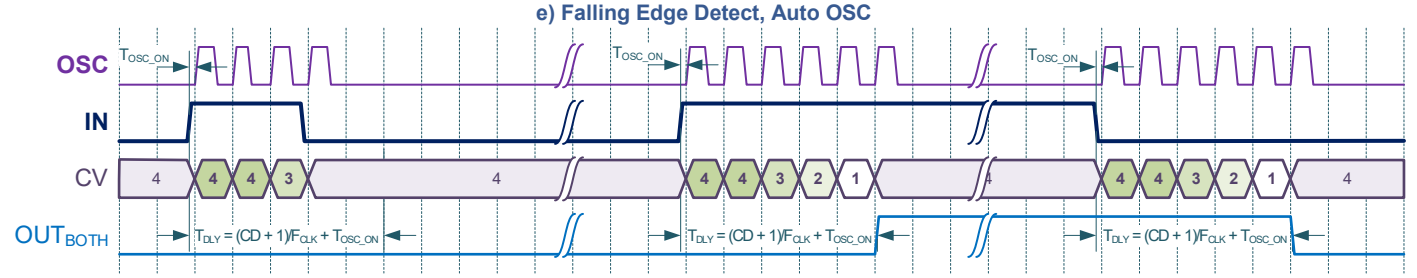
c) Both Edge Detect, Forced OSC



d) Rising Edge Detect, Auto OSC

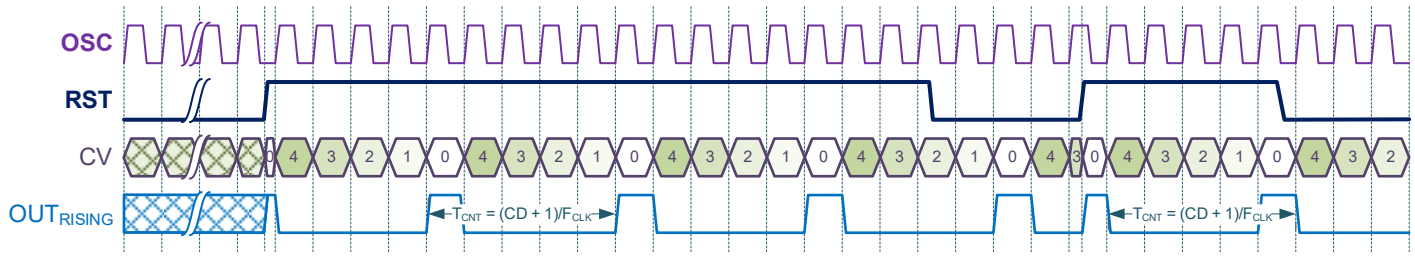


e) Falling Edge Detect, Auto OSC

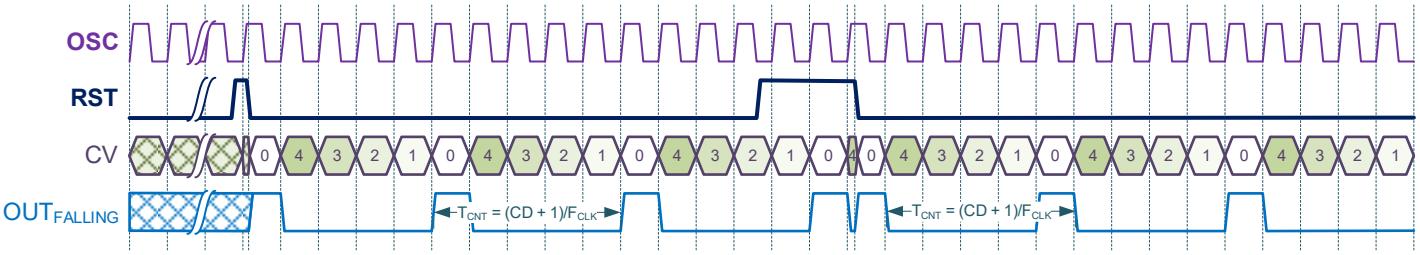


f) Both Edge Detect, Auto OSC

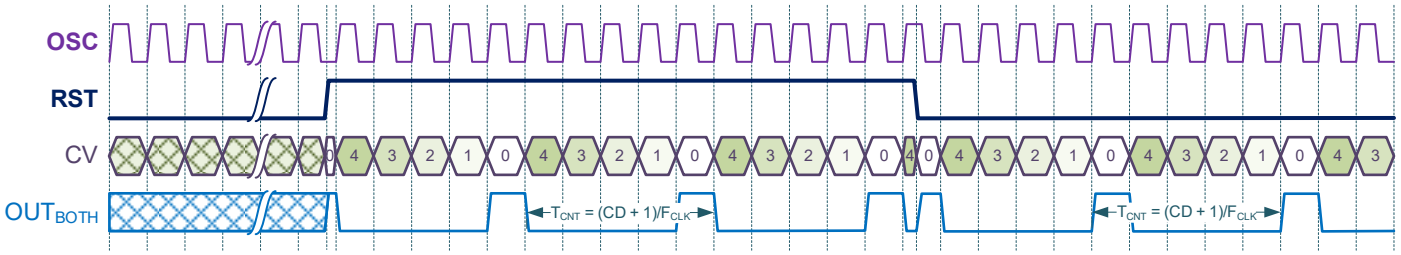
Figure 8.5. Delay Mode (Control Data: 4)



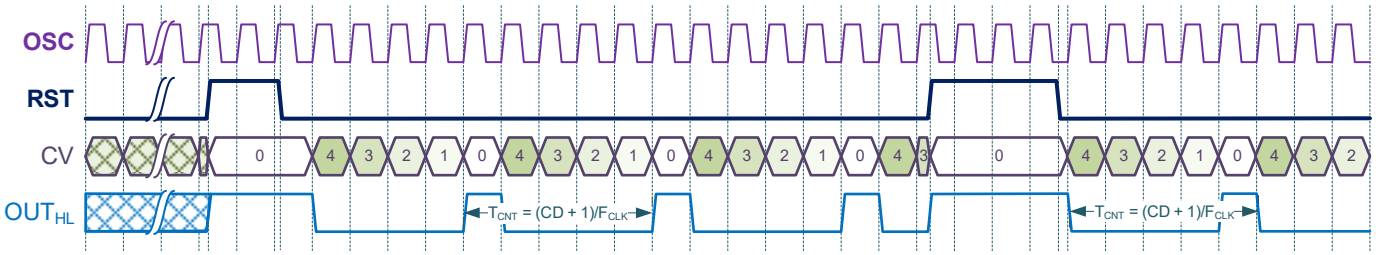
a) Rising Reset



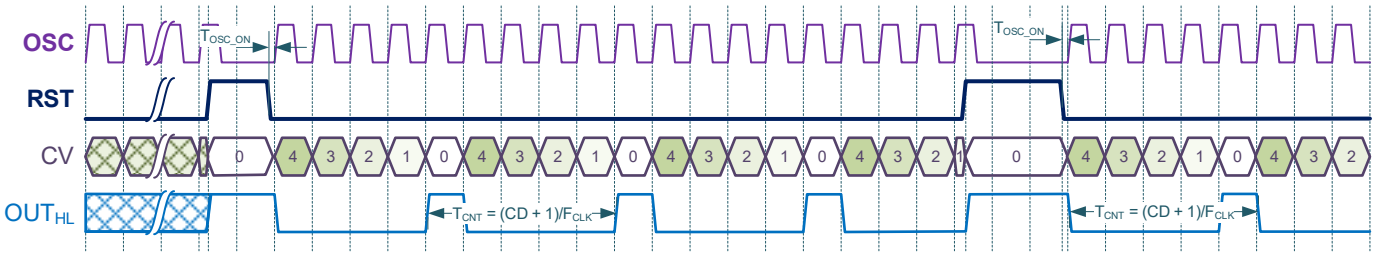
b) Falling Reset



c) Both Edge Reset



d) High Level Reset, Forced OSC



e) High Level Reset, Auto OSC

Figure 8.6. Counter Mode (Control Data: 4)

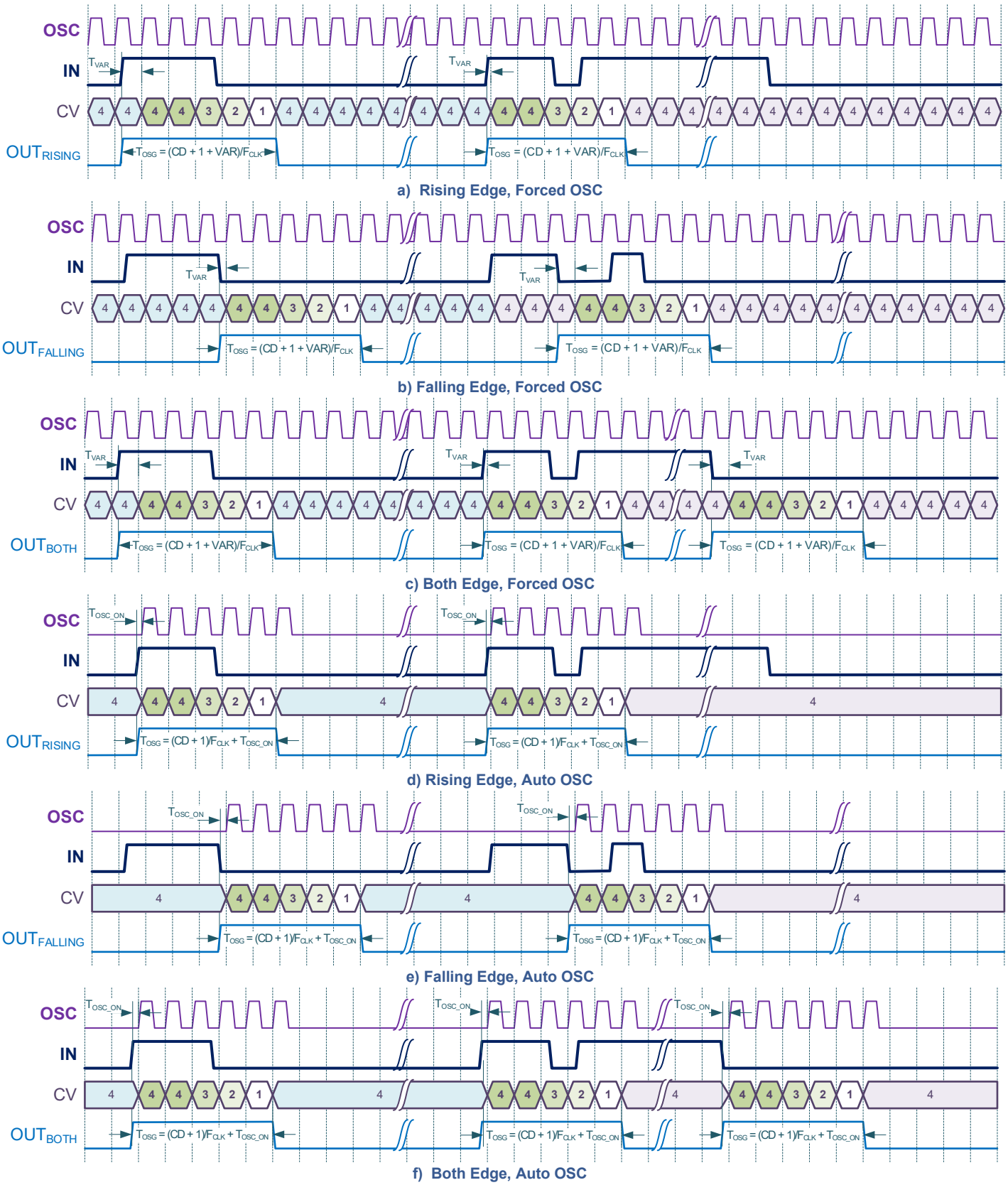
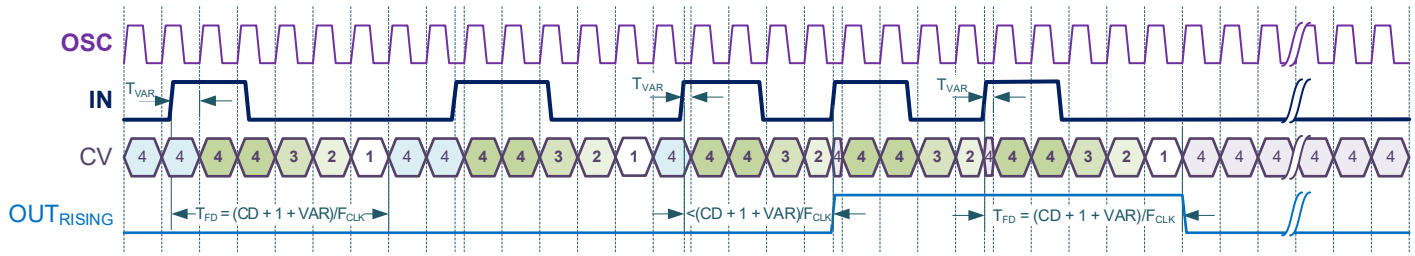
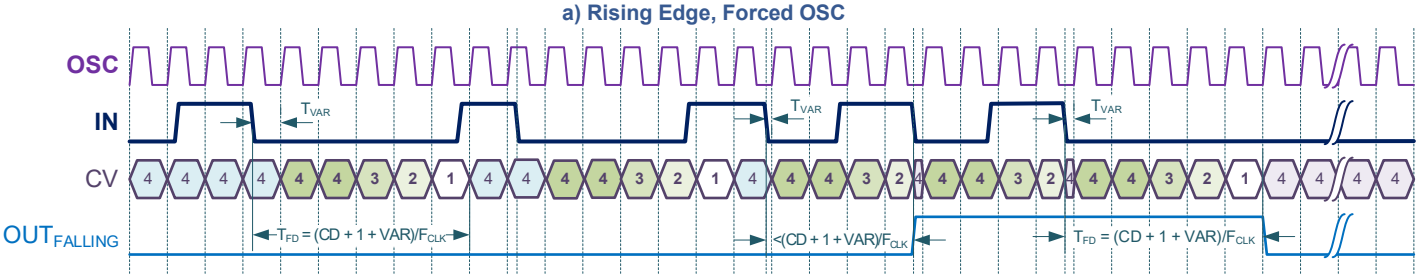


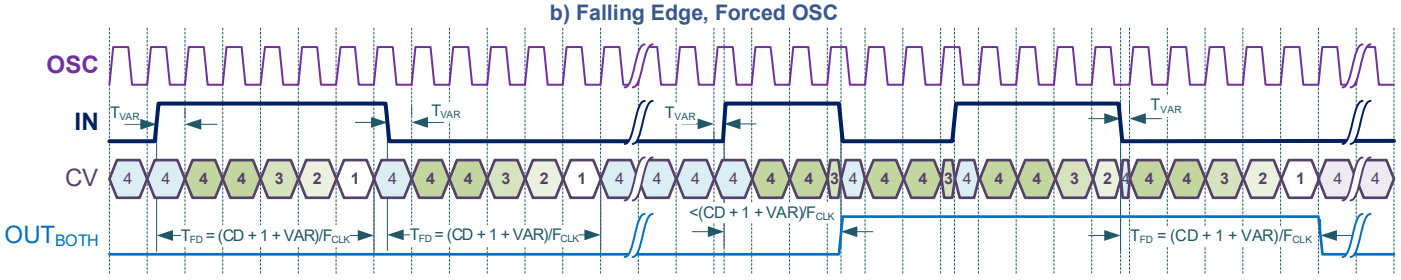
Figure 8.7. One-Shot Generator Mode (Control Data: 4)



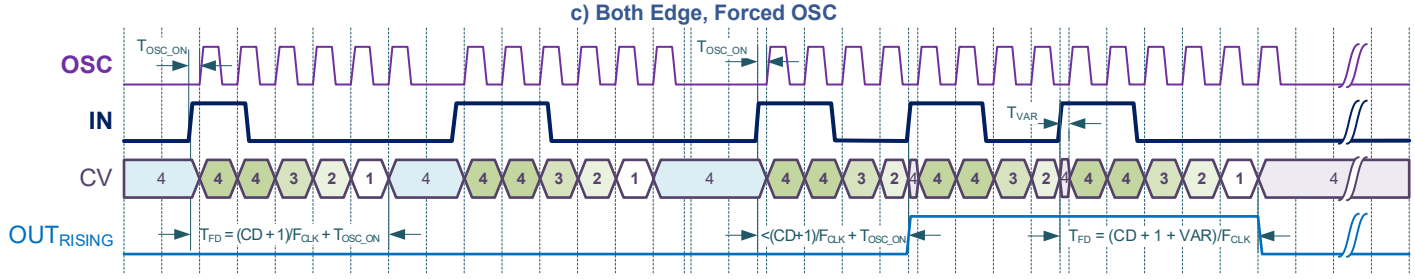
a) Rising Edge, Forced OSC



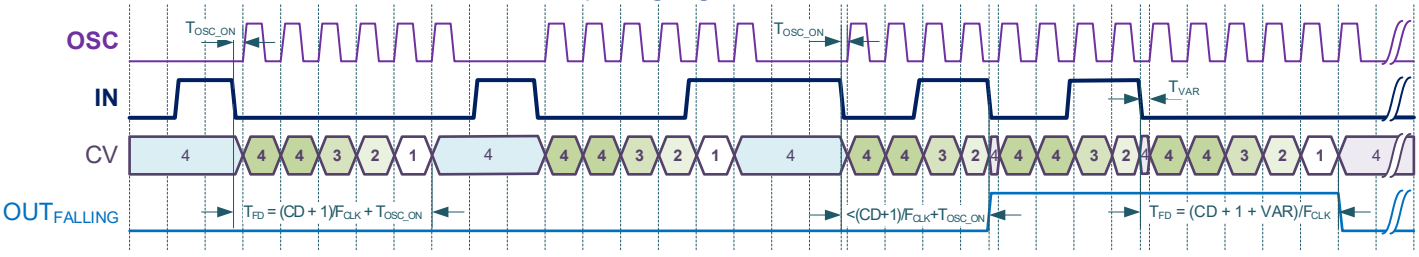
b) Falling Edge, Forced OSC



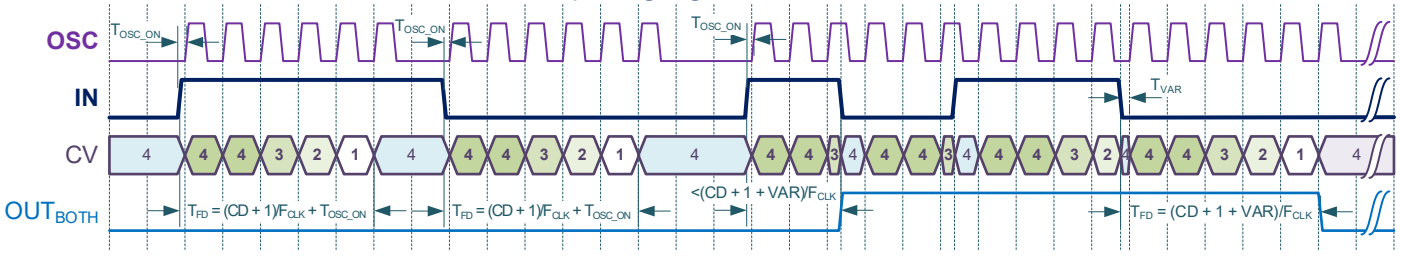
c) Both Edge, Forced OSC



d) Rising Edge, Auto OSC



e) Falling Edge, Auto OSC



f) Both Edge, Auto OSC

Figure 8.8. Frequency Detector Mode (Control Data: 4)

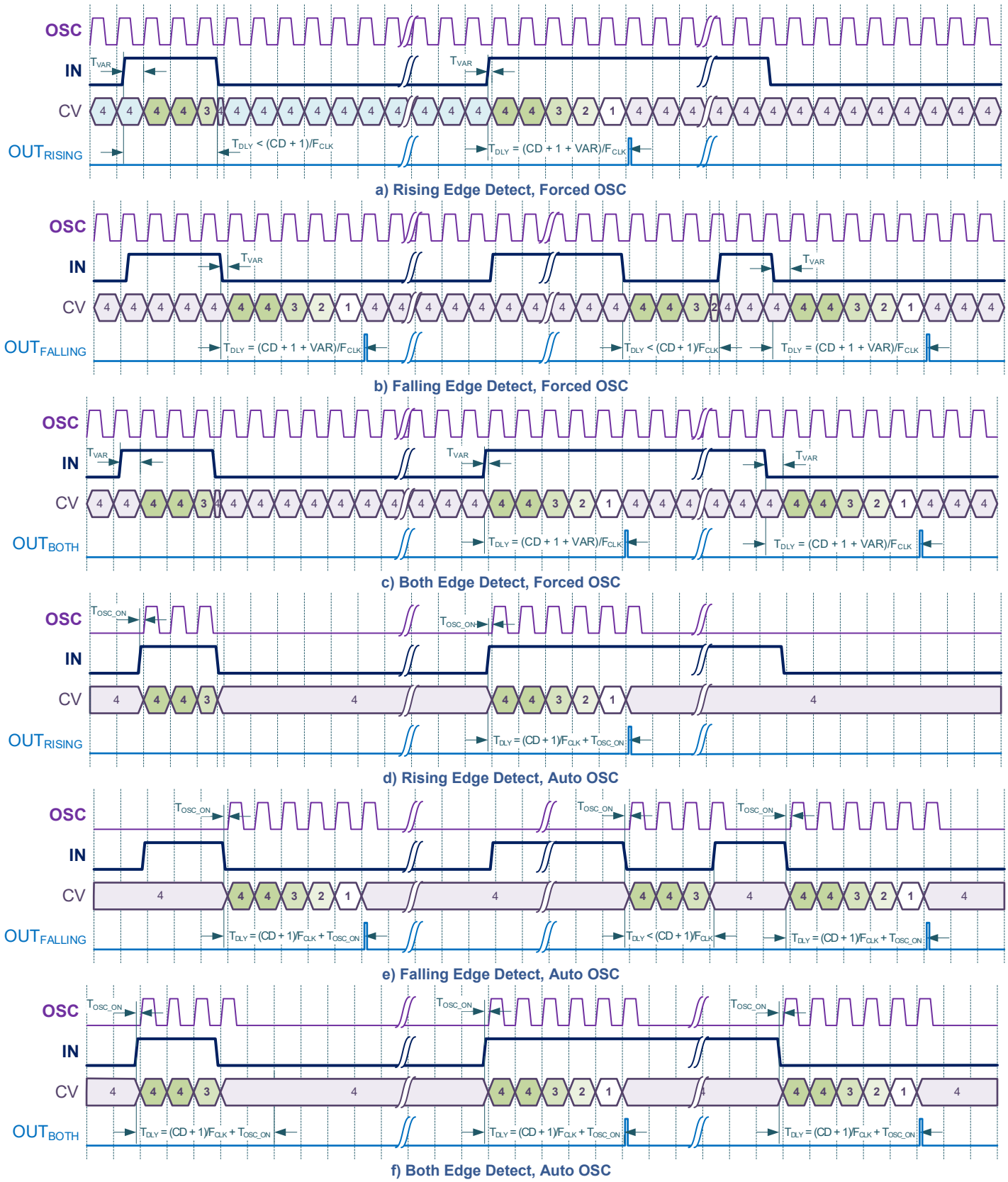


Figure 8.9. Delay Edge Detect Mode (Control Data: 4)

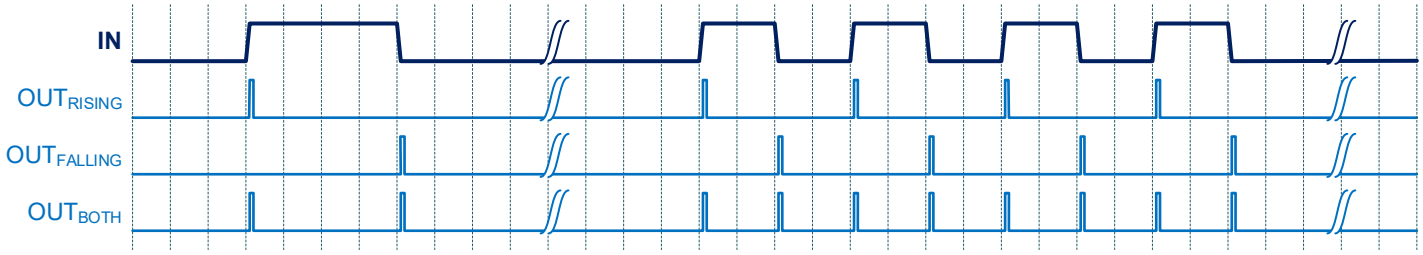
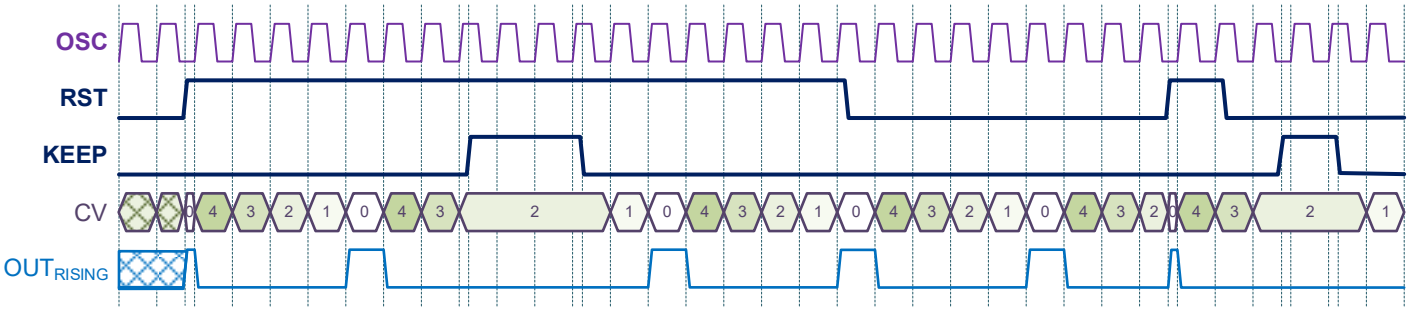
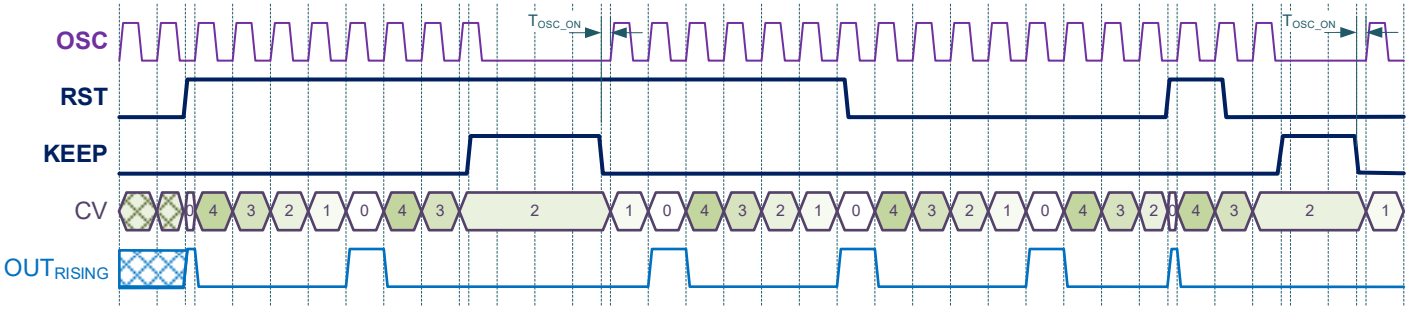


Figure 8.10. Edge Detector Mode



a) Rising Edge, Forced OSC



b) Rising Edge, Auto OSC

Figure 8.11. KEEP-functionality (Counter mode, Control Data: 4)

8.4.2. MF9 (3-bit LUT9/8-bit TMR1)

Settings of MF9 (3-bit LUT9/8-bit TMR1) are shown in Table 8.27.

Table 8.27. MF9 (3-bit LUT9/8-bit TMR1) Registers

Register Bit Address	Register Name	Register Definition
MF9 (3-bit LUT9/8-bit TMR1)		
<703>	MF9_MODE	MF mode: 0: LUT 1: Timer
<706:704>	MF9_TMR_MODE	Timer mode: 000: Delay 001: One shot 010: Frequency detector 011: Counter 100: Edge detector 101: Delayed edge detector 110: Reserved 111: Reserved
<708:707>	MF9_TMR_TRIG_EVENT	Timer trigger event: 00: On both falling and rising edges 01: On falling edge only 10: On rising edge only 11: High level reset (counter)
<711:709>	MF9_TMR_CLK	CLK source: 000: External CLK 001: OSC 010: OSC/4 011: OSC/8 100: OSC/16 101: OSC/64 110: OSC/128 111: Reserved
<712>	MF9_TMR_OSC_FORCE_EN	Force OSC by timer: 0: Disable 1: Enable
<714:713>	MF9_TMR_INIT_STATE	Timer initial state: 00: Initial 0 01: Initial 1 10: Bypass initial 11: Bypass initial
<715>	MF9_TMR_OUT_POL	Polarity of timer output: 0: OUT 1: nOUT
<723:716>	MF9_CTRL_DATA	MF control data

The 3-bit LUT9 uses an 8-bit register to define its output function (see Table 8.28).

Table 8.28. 3-bit LUT9 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	MF9_CTRL_DATA<0>	LSB
0	0	1	MF9_CTRL_DATA<1>	
0	1	0	MF9_CTRL_DATA<2>	
0	1	1	MF9_CTRL_DATA<3>	
1	0	0	MF9_CTRL_DATA<4>	
1	0	1	MF9_CTRL_DATA<5>	
1	1	0	MF9_CTRL_DATA<6>	
1	1	1	MF9_CTRL_DATA<7>	MSB

8.5. MF (4-bit LUT/8-bit TMR) Macrocells

Two macrocells have the capability to serve as 4-bit LUT or as 8-bit Timer (TMR). Schematic diagram of the macrocell is shown in Figure 8.12, Figure 8.13.

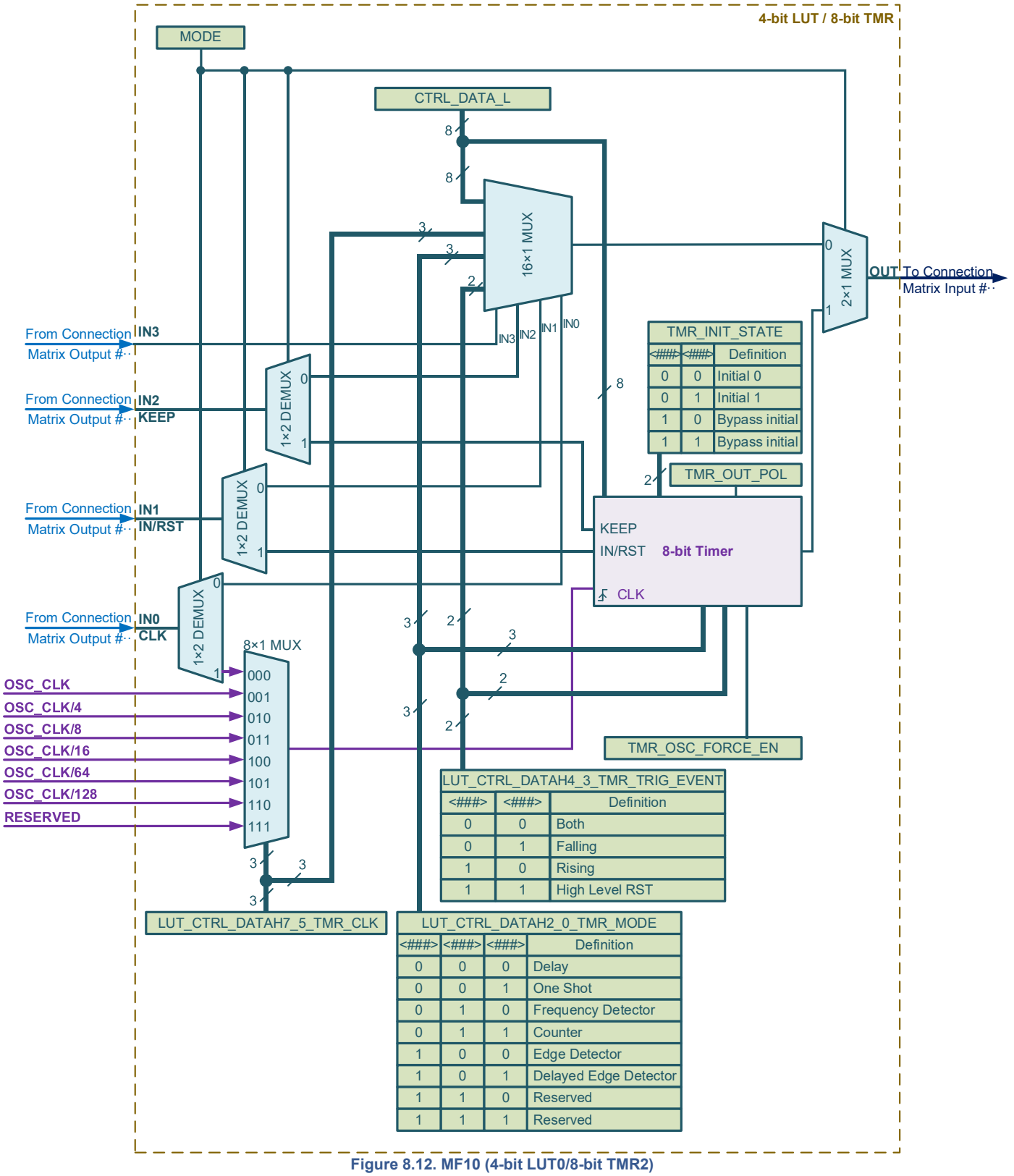
When the MF macrocells are used as LUT, the 4-bit LUT takes in four input signals from the connection matrix and produces a single output that goes back into the connection matrix. The LUT allows the user to implement used-defined combinatorial logic functions, including standard digital logic gates (AND, NAND, OR, NOR, XOR, XNOR). Standard logic gate configurations of the LUT are shown in Table 8.29.

When the macrocells are used to implement 8-bit TMR function, two input signals from the connection matrix go to the external clock (EXTCLK) and IN (RST for Counter) for the TMR, with the output going back to the connection matrix.

For description of Delay Mode, Counter Mode, One-Shot Mode, Frequency Mode, Edge Detect Mode, and Delayed Edge Detect Mode refer to section 8.4 and corresponding timing diagrams are shown in the section 8.4.1.

Table 8.29. 4-bit LUT Truth Table of Standard Logic Gates

Function	MSB															LSB
AND-4	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
NAND-4	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
OR-4	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
NOR-4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
XOR-4	0	1	1	0	1	0	0	1	1	0	0	1	0	1	1	0
XNOR-4	1	0	0	1	0	1	1	0	0	1	1	0	1	0	0	1



TMR_INIT_STATE

<###>	<###>	Definition
0	0	Initial 0
0	1	Initial 1
1	0	Bypass initial
1	1	Bypass initial

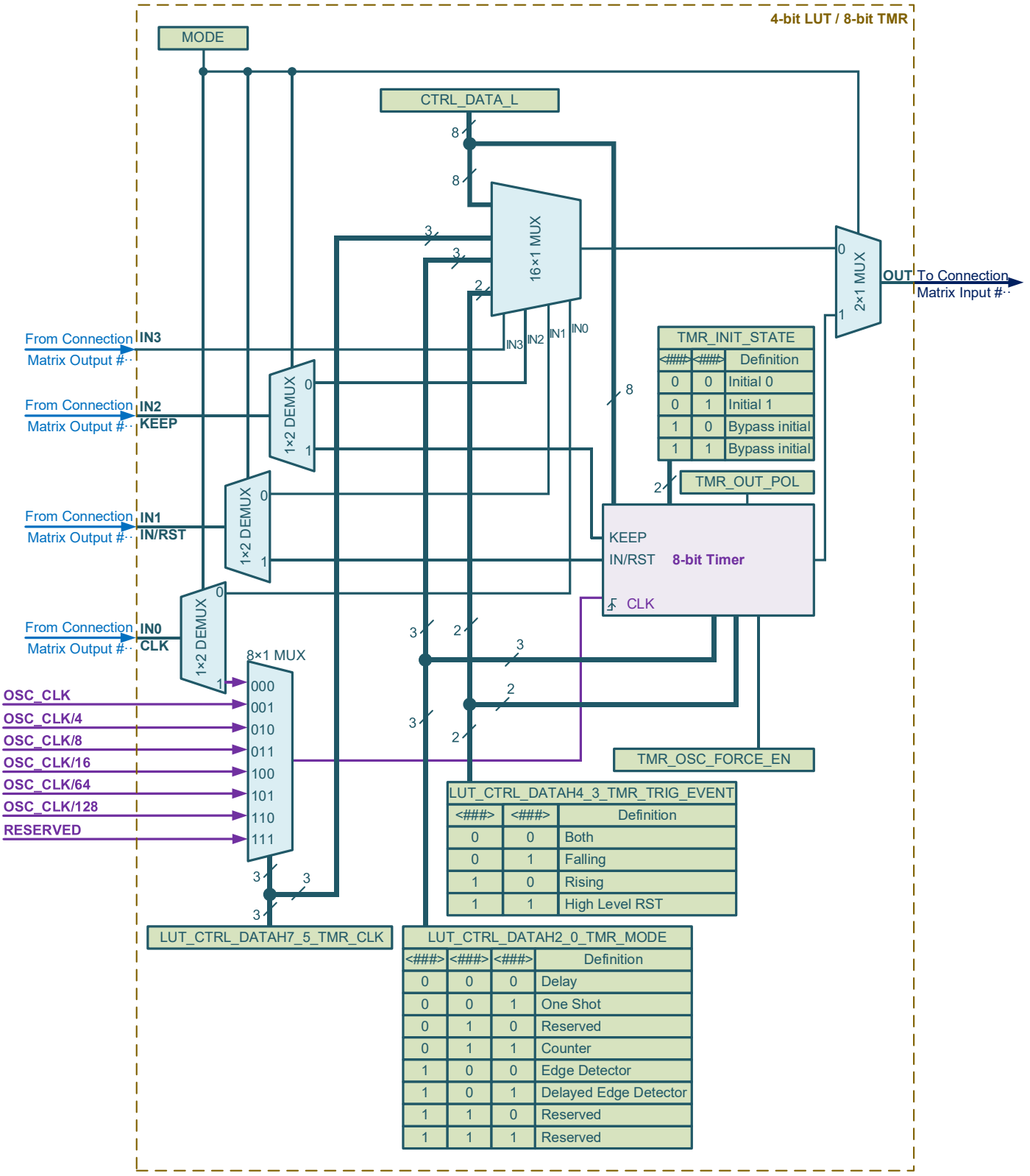
LUT_CTRL_DATAH4_3_TMR_TRIG_EVENT

<###>	<###>	Definition
0	0	Both
0	1	Falling
1	0	Rising
1	1	High Level RST

LUT_CTRL_DATAH2_0_TMR_MODE

<###>	<###>	<###>	Definition
0	0	0	Delay
0	0	1	One Shot
0	1	0	Frequency Detector
0	1	1	Counter
1	0	0	Edge Detector
1	0	1	Delayed Edge Detector
1	1	0	Reserved
1	1	1	Reserved

Figure 8.12. MF10 (4-bit LUT0/8-bit TMR2)



TMR_INIT_STATE		
<###>	<###>	Definition
0	0	Initial 0
0	1	Initial 1
1	0	Bypass initial
1	1	Bypass initial

LUT_CTRL_DATAH4_3_TMR_TRIG_EVENT		
<###>	<###>	Definition
0	0	Both
0	1	Falling
1	0	Rising
1	1	High Level RST

LUT_CTRL_DATAH2_0_TMR_MODE			
<###>	<###>	<###>	Definition
0	0	0	Delay
0	0	1	One Shot
0	1	0	Reserved
0	1	1	Counter
1	0	0	Edge Detector
1	0	1	Delayed Edge Detector
1	1	0	Reserved
1	1	1	Reserved

Figure 8.13. MF11 (4-bit LUT1/8-bit TMR3)

8.5.1. MF10 (4-bit LUT0/8-bit TMR2)

Settings of MF10 (4-bit LUT0/8-bit TMR2) are shown in Table 8.30.

Table 8.30. MF10 (4-bit LUT0/TMR2) Registers

Register Bit Address	Register Name	Register Definition
MF10 (4-bit LUT0/8-bit TMR2)		
<725>	MF10_MODE	MF mode: 0: LUT 1: Timer
<726>	MF10_TMR_OSC_FORCE_EN	Force OSC by timer: 0: Disable 1: Enable
<728:727>	MF10_TMR_INIT_STATE	Timer initial state: 00: Initial 0 01: Initial 1 10: Bypass initial 11: Bypass initial
<729>	MF10_TMR_OUT_POL	Polarity of timer output: 0: OUT 1: nOUT
<737:730>	MF10_CTRL_DATAL	MF low byte of control data
<740:738>	MF10_LUT_CTRL_DATAH2_0_TMR_MODE	<2:0> bits of LUT high byte control data or Timer mode: 000: Delay 001: One shot 010: Frequency detector 011: Counter 100: Edge detector 101: Delayed edge detector 110: Reserved 111: Reserved
<742:741>	MF10_LUT_CTRL_DATAH4_3_TMR_TRIG_EVENT	<4:3> bits of LUT high byte control data or Timer trigger event: 00: On both falling and rising edges 01: On falling edge only 10: On rising edge only 11: High level reset (counter)
<745:743>	MF10_LUT_CTRL_DATAH7_5_TMR_CLK	<7:5> bits of LUT high byte control data or CLK source: 000: External CLK 001: OSC 010: OSC/4 011: OSC/8 100: OSC/16 101: OSC/64 110: OSC/128 111: Reserved

The 4-bit LUT0 uses a 16-bit register to define its output function (see Table 8.31).

Table 8.31. 4-bit LUT0 Truth Table

IN3	IN2	IN1	IN0	OUT	
0	0	0	0	MF10_CTRL_DATAL<0>	LSB
0	0	0	1	MF10_CTRL_DATAL<1>	
0	0	1	0	MF10_CTRL_DATAL<2>	
0	0	1	1	MF10_CTRL_DATAL<3>	
0	1	0	0	MF10_CTRL_DATAL<4>	
0	1	0	1	MF10_CTRL_DATAL<5>	
0	1	1	0	MF10_CTRL_DATAL<6>	
0	1	1	1	MF10_CTRL_DATAL<7>	
1	0	0	0	MF10_LUT_CTRL_DATAH2_0_TMR_MODE<0>	
1	0	0	1	MF10_LUT_CTRL_DATAH2_0_TMR_MODE<1>	
1	0	1	0	MF10_LUT_CTRL_DATAH2_0_TMR_MODE<2>	
1	0	1	1	MF10_LUT_CTRL_DATAH4_3_TMR_TRIG_EVENT<0>	
1	1	0	0	MF10_LUT_CTRL_DATAH4_3_TMR_TRIG_EVENT<1>	
1	1	0	1	MF10_LUT_CTRL_DATAH7_5_TMR_CLK<0>	
1	1	1	0	MF10_LUT_CTRL_DATAH7_5_TMR_CLK<1>	
1	1	1	1	MF10_LUT_CTRL_DATAH7_5_TMR_CLK<2>	MSB

8.5.2. MF11 (4-bit LUT1/8-bit TMR3)

Settings of MF11 (4-bit LUT1/8-bit TMR3) are shown in Table 8.32.

Table 8.32. MF11 (4-bit LUT1/TMR3) Registers

Register Bit Address	Register Name	Register Definition
MF11 (4-bit LUT1/8-bit TMR3)		
<747>	MF11_MODE	MF mode: 0: LUT 1: Timer
<748>	MF11_TMR_OSC_FORCE_EN	Force OSC by timer: 0: Disable 1: Enable
<750:749>	MF11_TMR_INIT_STATE	Timer initial state: 00: Initial 0 01: Initial 1 10: Bypass initial 11: Bypass initial
<751>	MF11_TMR_OUT_POL	Polarity of timer output: 0: OUT 1: nOUT
<759:752>	MF11_CTRL_DATAL	MF low byte of control data
<762:760>	MF11_LUT_CTRL_DATAH2_0_TMR_MODE	<2:0> bits of LUT high byte control data or Timer mode: 000: Delay 001: One shot 010: Reserved 011: Counter 100: Edge detector 101: Delayed edge detector 110: Reserved 111: Reserved
<764:763>	MF11_LUT_CTRL_DATAH4_3_TMR_TRIG_EVENT	<4:3> bits of LUT high byte control data or Timer trigger event: 00: On both falling and rising edges 01: On falling edge only 10: On rising edge only 11: High level reset (counter)
<767:765>	MF11_LUT_CTRL_DATAH7_5_TMR_CLK	<7:5> bits of LUT high byte control data or CLK source: 000: External CLK 001: OSC 010: OSC/4 011: OSC/8 100: OSC/16 101: OSC/64 110: OSC/128 111: Reserved

The 4-bit LUT1 uses a 16-bit register to define its output function (see Table 8.33).

Table 8.33. 4-bit LUT1 Truth Table

IN3	IN2	IN1	IN0	OUT	
0	0	0	0	MF11_CTRL_DATAL<0>	LSB
0	0	0	1	MF11_CTRL_DATAL<1>	
0	0	1	0	MF11_CTRL_DATAL<2>	
0	0	1	1	MF11_CTRL_DATAL<3>	
0	1	0	0	MF11_CTRL_DATAL<4>	
0	1	0	1	MF11_CTRL_DATAL<5>	
0	1	1	0	MF11_CTRL_DATAL<6>	
0	1	1	1	MF11_CTRL_DATAL<7>	
1	0	0	0	MF11_LUT_CTRL_DATAH2_0_TMR_MODE<0>	
1	0	0	1	MF11_LUT_CTRL_DATAH2_0_TMR_MODE<1>	
1	0	1	0	MF11_LUT_CTRL_DATAH2_0_TMR_MODE<2>	
1	0	1	1	MF11_LUT_CTRL_DATAH4_3_TMR_TRIG_EVENT<0>	
1	1	0	0	MF11_LUT_CTRL_DATAH4_3_TMR_TRIG_EVENT<1>	
1	1	0	1	MF11_LUT_CTRL_DATAH7_5_TMR_CLK<0>	
1	1	1	0	MF11_LUT_CTRL_DATAH7_5_TMR_CLK<1>	
1	1	1	1	MF11_LUT_CTRL_DATAH7_5_TMR_CLK<2>	MSB

8.6. MF (PDLY/Edge Detector)

The ALM1412 has a macrocell that can serve as a programmable delay (PDLY) or as an edge detector (Figure 8.14).

In PDLY mode, the macrocell serves as both an edge delay with four selectable delay values: T_{ADJ}: 140 ns, 280 ns, 420 ns, 560 ns. If the input signal is shorter than the delay value, the signal does not propagate to the output and is filtered out.

In Edge Detector mode, the macrocell generates a high-level pulse (for non-inverted polarity) when detecting the respective selected edge event (rising edge, falling edge, both edges). The pulse width value (T_{WIDTH}) is configurable (140 ns, 280 ns, 420 ns, 560 ns).

See the timing diagrams below for further information (Figure 8.15).

The output polarity of the macrocell is configurable and can be selected as non-inverted or inverted.

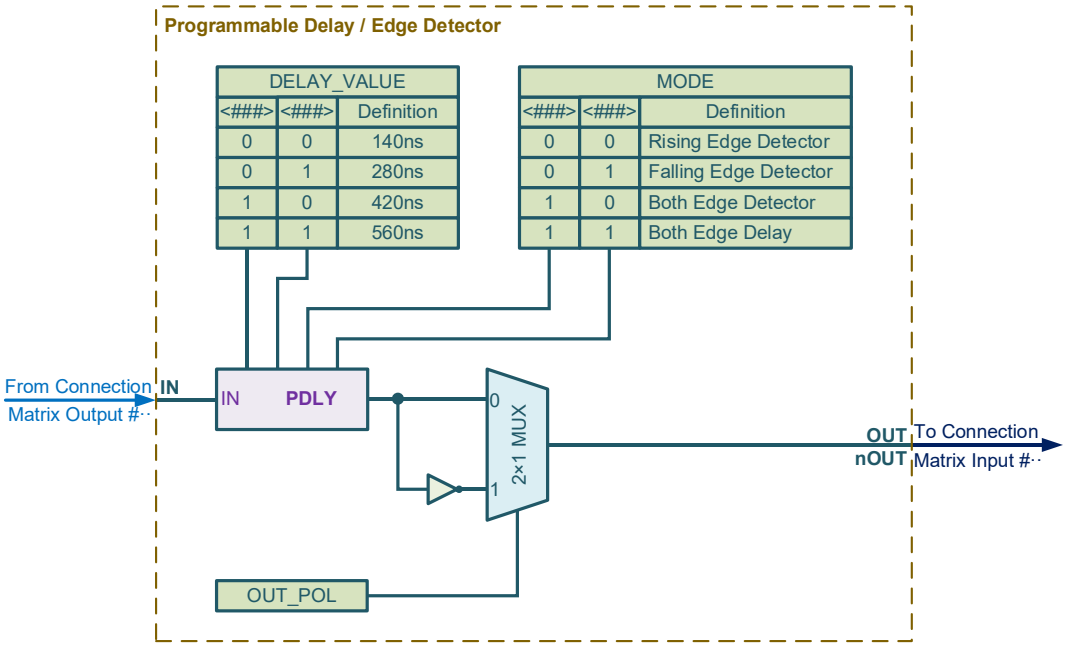


Figure 8.14. MF (PDLY/Edge Detector)

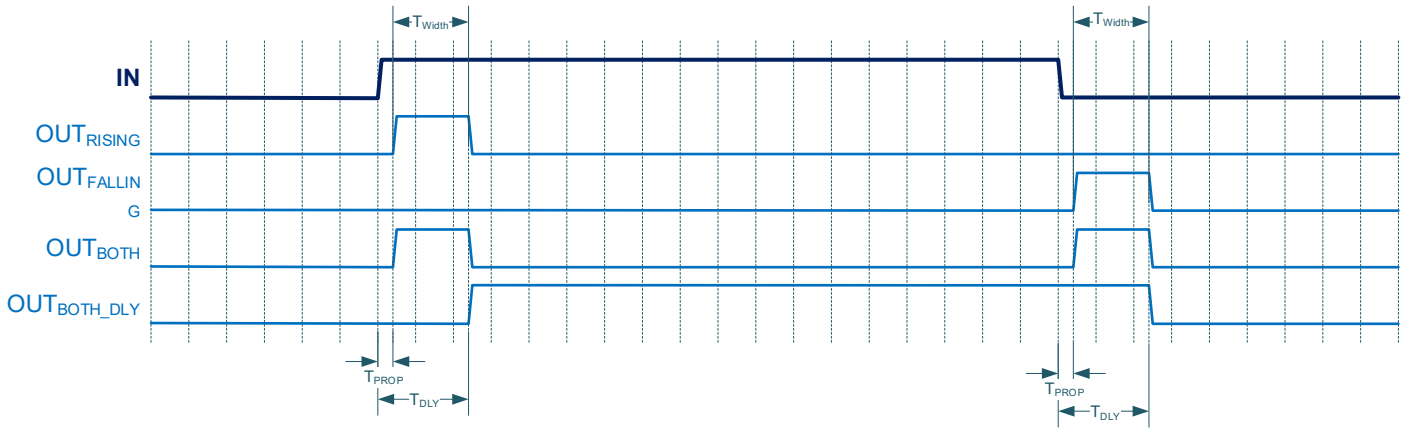


Figure 8.15. Edge Detector Output

8.6.1. MF12 (PDLY/Edge Detector)

Settings of MF12 (PDLY/Edge Detector) are shown in Table 8.34.

Table 8.34. MF12 (PDLY/Edge Detector) Registers

Register Bit Address	Register Name	Register Definition
MF12 (PDLY/Edge Detector)		
<770:769>	MF12_MODE	MF mode: 00: Rising edge detector 01: Falling edge detector 10: Both edge detector 11: Both edge delay
<771>	MF12_OUT_POL	Output polarity: 0: OUT 1: nOUT
<773:772>	MF12_DELAY_VAL	Delay value: 00: 140ns 01: 280ns 10: 420ns 11: 560ns

9. Timers

Four macrocells within the ALM1412 provide support for timer functionality. There is one 16-bit TMR, and three Multifunctional Macrocells that can be used as 8-bit timers (see Section 8.4. MF (3-bit LUT/8-bit TMR) Macrocell and 8.5. MF (4-bit LUT/8-bit TMR) Macrocells).

Two input signals from the connection matrix go to the external clock (CLK/KEEP) and IN (RST for Counter) for the TMR, with the output going back to the connection matrix. The mode of the CLK/KEEP can be determined by the CLK_KEEP_SEL register.

For a description of Delay Mode, Counter Mode, One-Shot Mode, Frequency Mode, Edge Detect Mode, and Delayed Edge Detect Mode, refer to section 8.4 and the corresponding timing diagrams, which are shown in section 8.4.1.

9.1. 16-bit timer

The schematic diagram of the macrocell is shown in Figure 9.1.

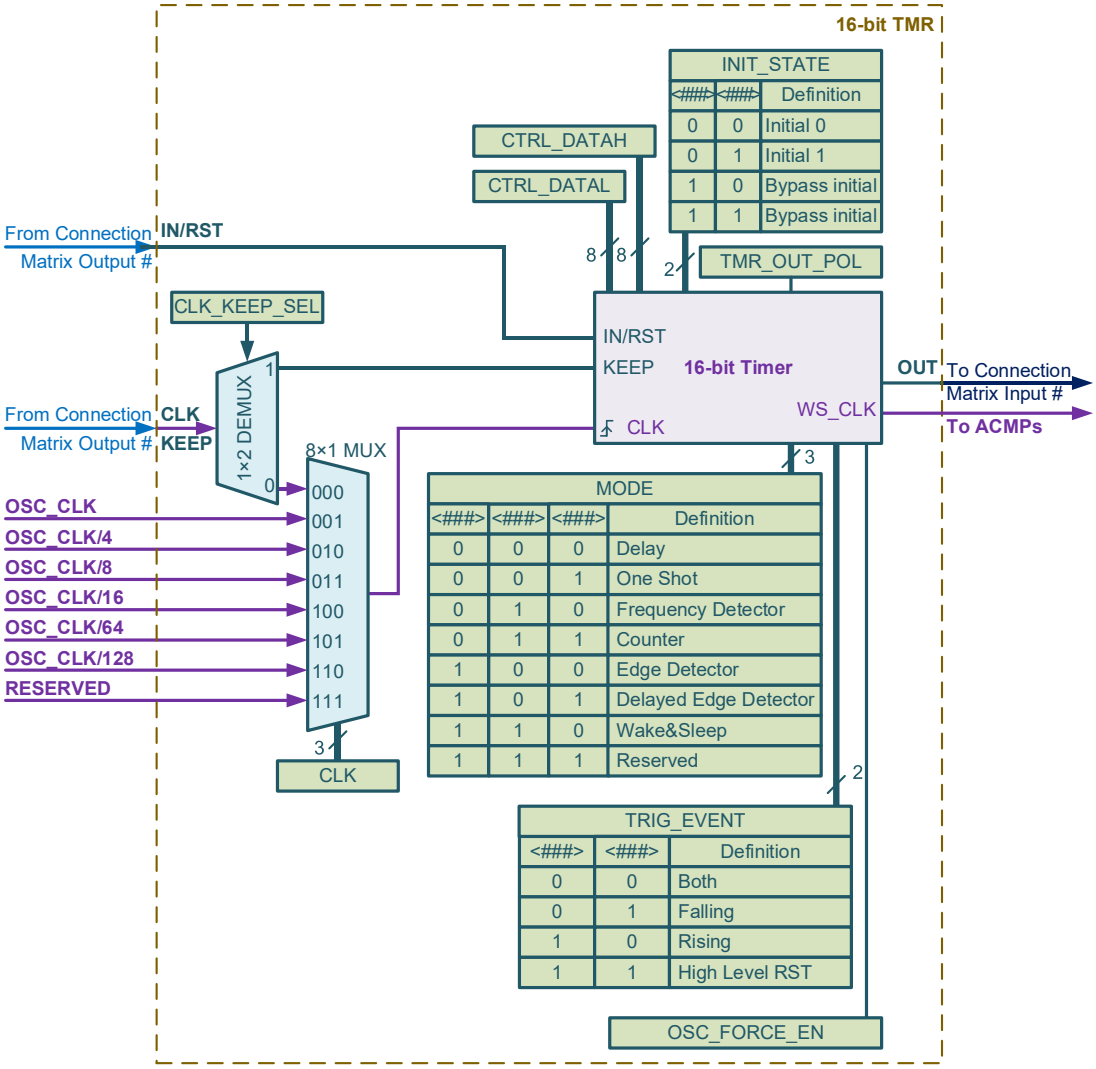


Figure 9.1. 16-bit TMR

9.1.1. 16-bit TMR0

The 16-bit TMR0 macrocell, in addition to the common operation modes, can be used as Wake&Sleep Controllers for the ACMPs, which allows the user reduce the ACMPs' power consumption by turning on the ACMP only for a short period of time.

To control the ACMPs with the WS macrocell, the following configuration should be performed:

- ACMP Power Up Input from matrix is HIGH (for desired ACMP);
- SET WS_EN register of desired ACMP;
- TMR0 should be set to WS function;
- RESET IN of WS is LOW in case TMR0_TRIG_EVENT set to High level reset.

The user selects a period of time while the ACMPs are sleeping with Control Data of the TMR0 (1…65535). The ACMP state (High or Low) can be updated during Wake Time and Latch for the sleeping time.

Note 9.1: For the WS function the period of the input clock should be selected greater than ACMP Power On Time (t_{START}).

Settings of 16-bit TMR0 are shown in Table 9.1.

Table 9.1. 16-bit TMR0 Registers

Register Bit Address	Register Name	Register Definition
16-bit TMR0		
<776:774>	TMR0_MODE	Timer mode: 000: Delay 001: One shot 010: Frequency detector 011: Counter 100: Edge detector 101: Delayed edge detector 110: Wake&Sleep 111: Reserved
<778:777>	TMR0_TRIG_EVENT	Timer trigger event: 00: On both falling and rising edges 01: On falling edge only 10: On rising edge only 11: High level reset (counter)
<781:779>	TMR0_CLK	CLK source: 000: External CLK 001: OSC 010: OSC/4 011: OSC/8 100: OSC/16 101: OSC/64 110: OSC/128 111: Reserved
<782>	TMR0_CLK_KEEP_SEL	Input mode selection: 0: CLK 1: KEEP
<783>	TMR0_OSC_FORCE_EN	Force OSC by timer: 0: Disable 1: Enable
<785:784>	TMR0_INIT_STATE	Timer initial state: 00: Initial 0 01: Initial 1 10: Bypass initial 11: Bypass initial
<786>	TMR0_OUT_POL	Polarity of timer output: 0: OUT 1: nOUT
<794:787>	TMR0_CTRL_DATAL	Low byte of control data
<802:795>	TMR0_CTRL_DATAH	High byte of control data

10. Memory Architecture

The memory of the µASIC consists of two main parts: non-volatile memory (NVM) and registers. The configuration of the µASIC is stored in the NVM and is loaded to the volatile registers during device power up. The register values define the macrocells' configuration, matrix connections setting (signal routing), IO configuration etc., that allows the user to retrieve the desired functionality for the end application (see Figure 10.1).

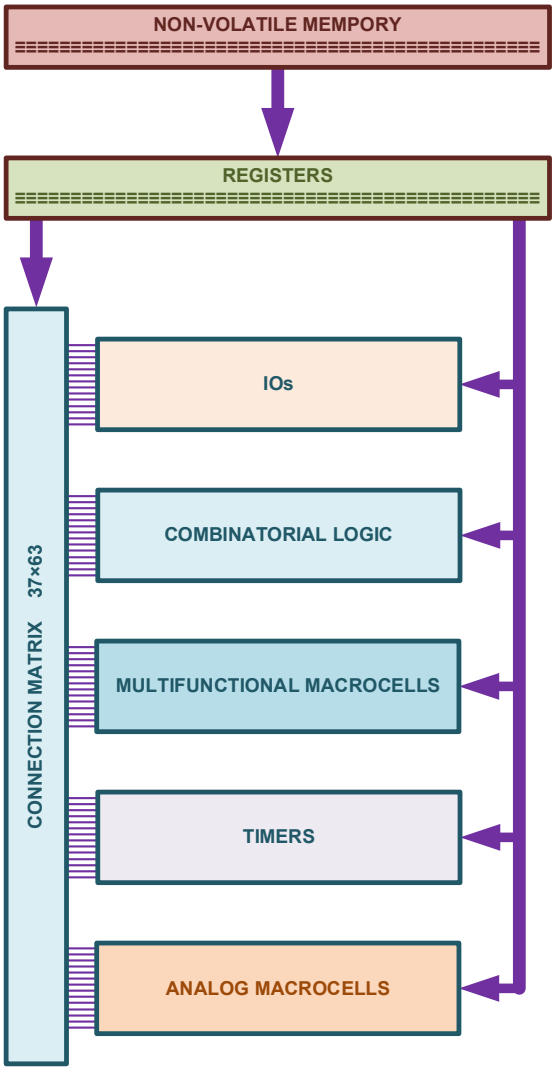


Figure 10.1. Memory Architecture

11. Data Protection

The ALM1412 has two data protection features, CRC-8 and CRV, that are enabled by SYS_SECURITY_CTRL (Table 11.1).

Table 11.1. Security Control Registers

Register Bit Address	Register Name	Register Definition
Security Control		
<60>	SYS_SECURITY_CRC_EN	CRC verification: 0: Disable 1: Enable
<68:61>	SYS_SECURITY_CRC	CRC ($x^8+x^6+x^3+1$)
<69>	SYS_SECURITY_CRV_EN	Continuous register verification: 0: Disable 1: Enable

11.1. CRC-8

Validity of correct NVM programming and NVM loading to the registers are checked by CRC-8. If the CRC-8 is Enabled and no errors are detected, the ALM1412 powers up. Otherwise, the chip will restart. CRC polynomial is $x^8 + x^6 + x^3 + 1$.

11.2. CRV

Continuous Registers Verification (CRV) is provided by a continuous comparison of the dedicated register bits spread all over the memory with hardcoded value 32'b 01010100111011001110111010111110. If the comparison shows a mismatch, the µASIC automatically restarts.

12. Analog Comparators (ACMP)

The µASIC has 2 Analog Comparator macrocells (ACMP) that can be used to compare the voltage of two analog inputs (IN+ and IN-), with a digital output going to the matrix connection indicating which input voltage is higher. When the voltage at IN+ input is higher than voltage at IN-, the digital output is HIGH and vice versa.

The ACMP also has PWR ON input, coming from the connection matrix, and is used to power on/off the ACMP. This allows the user to control the ACMP power on/off state from the connection matrix. The output of the ACMP is LOW when the ACMP PWR ON signal is LOW. Also, there is one more input, which comes from the TMR0 output when the ACMP is configured for Wake&Sleep (WS) mode. It allows the user to reduce the average current consumption of the part by periodically switching the ACMP on/off . In WS mode, the ACMP output will keep its previous value during power-off time.

PWR ON = 1 => ACMP is powered on.
PWR ON = 0 => ACMP is powered off.

The ACMP output remains low during ACMP start-up time (see Table 4.16) and then becomes valid.
For each ACMP that can be enabled, low-power mode reduces the total current consumption of the ACMP by reducing the bandwidth of the ACMP.

ACMP IN+ and IN- can be sourced with a variety of external and internal sources with a recommended voltage range IN+ = 0…VDD, IN- = 0…VDD-0.4V. Also, there is a selectable gain stage for the IN+ input that allows the user to select one of the following gains: 1.00×, 0.50×, 0.33×, 0.25×. Each ACMP has an optional input buffer on the IN+ input, which can be used along with the gain stage to increase IN+ input resistance (see Table 4.16 for R_{SIN}). However, the input buffer increases the input offset voltage and current consumption of the ACMP.

ACMP has three selectable hysteresis modes:

- No hysteresis;
- 25mV Hysteresis. This mode sets the hysteresis to 25mV, which can be used either for internal or external reference. The high threshold is VREF + hysteresis/2 and the low threshold is VREF – hysteresis/2;
- Custom Hysteresis. In this mode, there is a possibility to directly select low-to-high (VREFH) and high-to-low (VREFL) thresholds. This mode functions only when an internal VREF is used.

IO4 can be used as a common negative input for all ACMPs.

Configurations of ACMPs are shown in Table 12.1 and Table 12.2.

12.1. ACMP Block Diagram

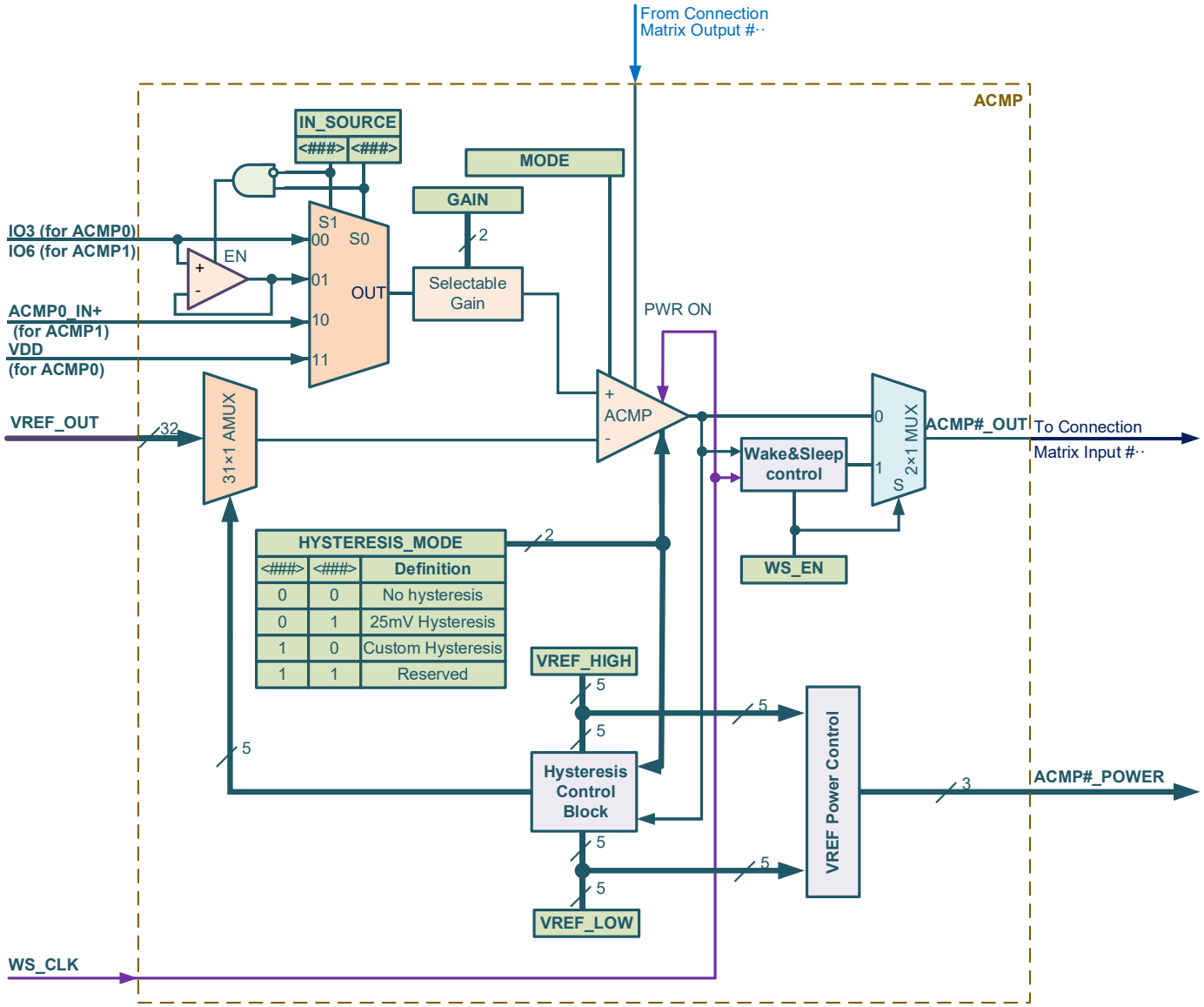


Figure 12.1. ACMP Block Diagram

12.2. ACMP0 Register Setting

Table 12.1 ACMP0 Register Setting

Register Bit Address	Register Name	Register Definition
ACMP0		
<831:830>	ACMP0_IN_SOURCE	IN+ source: 00: IO3 01: Buffered IO3 10: Reserved 11: VDD
<833:832>	ACMP0_GAIN	IN+ gain: 00: 1.00× 01: 0.50× 10: 0.33× 11: 0.25×
<835:834>	ACMP0_HYSTERESIS_MODE	Hysteresis mode: 00: No hysteresis (see Note 12.1) 01: 25mV (see Note 12.1) 10: Custom hysteresis 11: Reserved
<836>	ACMP0_MODE	Mode: 0: High speed 1: Low power (see Note 12.2)
<837>	ACMP0_WS_EN	Wake&Sleep: 0: Disable 1: Enable
<842:838>	ACMP0_VREFL	High to Low threshold: see Table 13.1
<847:843>	ACMP0_VREFH	Low to High threshold: see Table 13.1

Note 12.1 In this hysteresis mode, ACMP0_VREFH is used as voltage reference.

Note 12.2 With low current consumption, input noise suppression is also achieved by lowering the input bandwidth.

12.3. ACMP1 Register Setting

Table 12.2 ACMP1 Register Setting

Register Bit Address	Register Name	Register Definition
ACMP1		
<850:849>	ACMP1_IN_SOURCE	IN+ source: 00: IO6 01: Buffered IO6 10: ACMP0 IN+ 11: Reserved
<852:851>	ACMP1_GAIN	IN+ gain: 00: 1.00× 01: 0.50× 10: 0.33× 11: 0.25×
<854:853>	ACMP1_HYSTERESIS_MODE	Hysteresis mode: 00: No hysteresis (see Note 12.3) 01: 25mV (see Note 12.1) 10: Custom hysteresis 11: Reserved
<855>	ACMP1_MODE	Mode: 0: High speed 1: Low power (see Note 12.4)
<856>	ACMP1_WS_EN	Wake&Sleep: 0: Disable 1: Enable
<861:857>	ACMP1_VREFL	High to Low threshold: see Table 13.1
<866:862>	ACMP1_VREFH	Low to High threshold: see Table 13.1

Note 12.3 In this hysteresis mode, ACMP1_VREFH is used as voltage reference.

Note 12.4 With low current consumption, input noise suppression is also achieved by lowering the input bandwidth.

13. Voltage Reference (VREF)

The µASIC has a built-in Voltage Reference (VREF) Macrocell that provides a variety of selectable voltage levels to ACMPs (see Table 13.1). Also, the macrocell has an option to output a reference voltage on IO10 (Table 13.2, Figure 13.1). The VREF macrocell has a selection of internally generated voltage references, /2, /3 and /4 reference of V_{DD}, and externally supplied voltage reference from IO4, which can also be divided via a voltage divider. The input impedance of the divider can be found in Table 4.17 (RVDD_DIV, REXT_DIV).

Table 13.1. VREF Selection

Selection Registers <4:0>	VREF
00000	50mV
00001	100mV
00010	150mV
00011	200mV
00100	250mV
00101	300mV
00110	350mV
00111	400mV
01000	450mV
01001	500mV
01010	550mV
01011	600mV
01100	650mV
01101	700mV
01110	750mV
01111	800mV
10000	850mV
10001	900mV
10010	950mV
10011	1000mV
10100	1050mV
10101	1100mV
10110	1150mV
10111	1200mV
11000	VDD/2
11001	VDD/3
11010	VDD/4
11011	Reserved
11100	EXT_VREF (IO4)
11101	EXT_VREF (IO4)/2
11110	EXT_VREF (IO4)/3
11111	EXT_VREF (IO4)/4

Table 13.2 VREF Register Setting

Register Bit Address	Register Name	Register Definition
VREF		
<869:868>	VREF_PWR_ON	VREF output to IO10 power on: 00: Power Off 01: Power On 10: Controlled by Connection Matrix 11: Controlled by Connection Matrix
<874:870>	VREF_IO_VALUE	VREF IO value: see Table 13.1

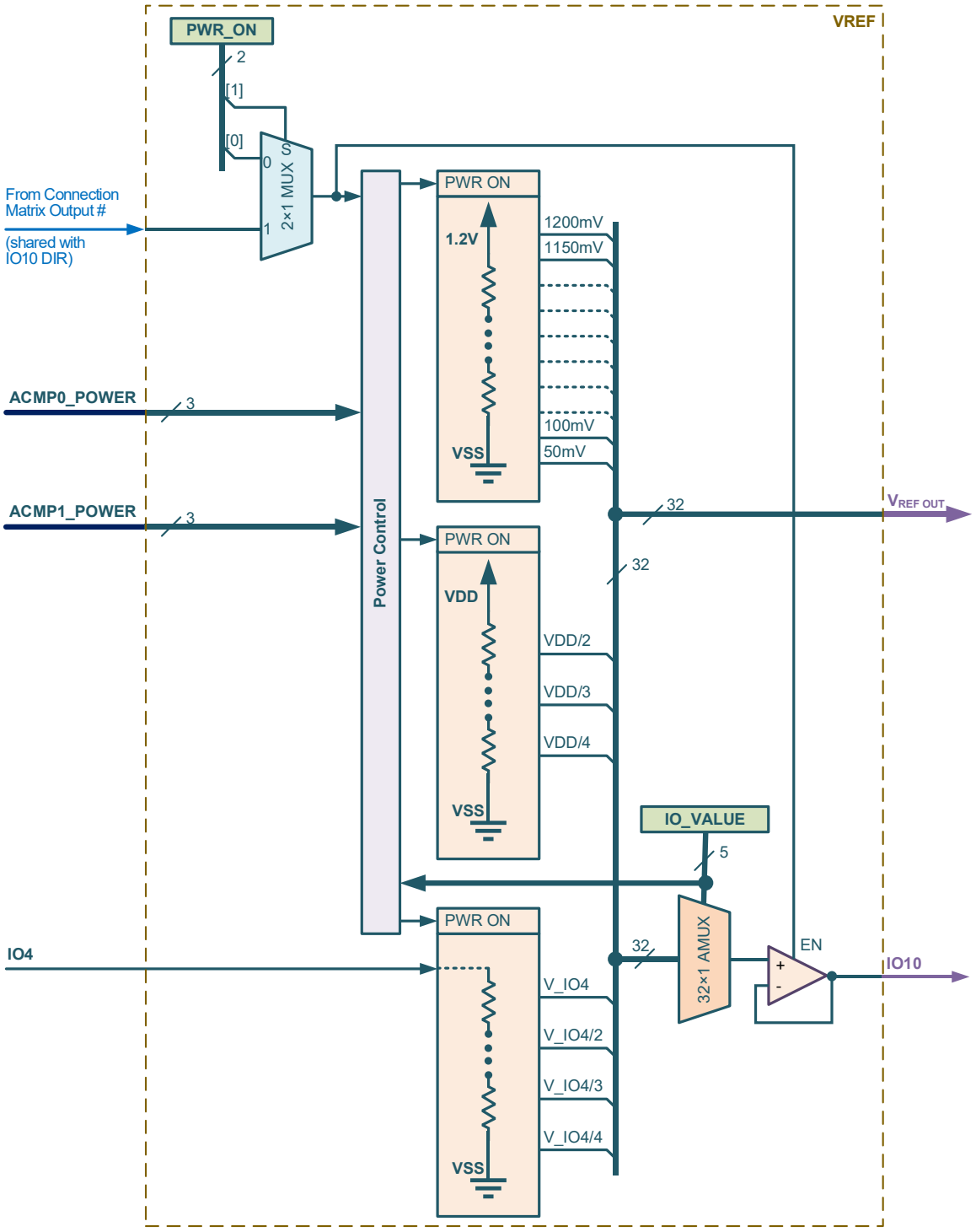


Figure 13.1. Voltage Reference Block Diagram

14. 100µA Current Source

The µASIC has a d100µA Current Source connected to IO3 (IN+ ACMP0) (Figure 14.1). The current source can be used either as a standalone or together with the ACMP0 for various purposes. The 100µA Current Source can be turned on by the corresponding register (Table 14.1).

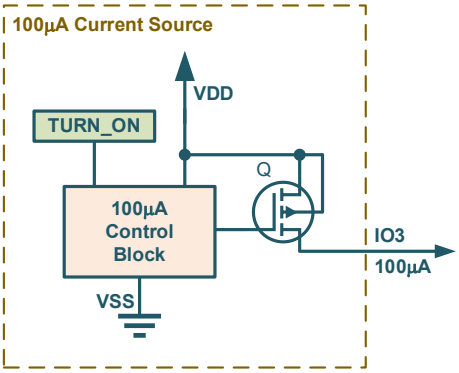


Figure 14.1. 100uA Current Source Block Diagram

Table 14.1 100µA Current Source Registers

Register Bit Address	Register Name	Register Definition
100µA Current Source		
<882>	CURR_SOURCE_TURN_ON	Turn on current source: 0: 100µA turn off 1: 100µA turn on

15. Oscillator (OSC)

The ALM1412 has an internal oscillator that allows the user to cover a variety of applications:

- OSC with two selectable output frequencies 25 kHz or 2 MHz.

The OSC macrocell can be sourced from either an internal oscillator or by an external frequency from IO12.

The OSC has two divider stages that give the user flexibility to introduce clock signals on the Connection Matrix Input lines. The first stage (prescaler) allows the user to divide the fundamental frequency by **/1**, **/2**, **/4** or **/8**. The two independent second stage dividers allow the user to divide the frequency from the first stage divider by **/1**, **/2** or **/4**, **/8**, **/16, /32, /64, /128** and outputs this frequency on the Connection Matrix Input #34 and #35 (See Figure 15.1 and Table 15.3 for more details).

Each oscillator has three power states of operation (see Table 15.1). The flow of turning on the oscillator starts from the OFF state, then goes to IDLE state, and lastly is in the ON state, in which the frequency appears on the oscillator output.

Table 15.1. Oscillator power states

State	Description
OFF state	The oscillator is fully shut down and consumes the minimum amount of current (less than 1nA). The power on time of the oscillator is longer compare to the power on from the IDLE state (see Table 4.10, Table 4.14). The oscillator stays in this state when it is not turned on by timers or control input, and Power On Time is selected as normal.
IDLE state	The power consumption is higher compared to the OFF state and depends on the type of oscillator (see Table 4.5). The oscillator is ready to operate and power on time is within 1 clock cycle of the oscillator.
ON state	The oscillator consumes its active current and frequency is generated on the oscillator output (see Table 4.5)

Each oscillator has three settings that allow the user to choose the appropriate mode of operation (see Table 15.2).

Table 15.2. Oscillator setting

Setting	Option	Description
Power On Time	Normal	The oscillator power on time is normal (see Table 4.10, Table 4.14). When the oscillator is turned off it stays in the OFF state.
	Fast	The oscillator power on time fast, within 1 clock cycle (see Table 4.10, Table 4.14). When the oscillator is turned off it stays in the IDLE state.
Control Input Mode	Power down	High level of CTRL IN turns off the oscillator. The low level of CTRL IN doesn't affect the operation of the oscillator.
	Force on	HIGH level of CTRL IN turns on the oscillator. The low level of CTRL IN doesn't affect the operation of the oscillator.
Power Mode	Auto power on	The oscillator is turned on when any of timers require it, or control input signal force it (Note 15.1).
	Forced power on	The oscillator is turned on when part is powered on and control input signal doesn't shut down it.

Note 15.1 Power control signal has the highest priority.

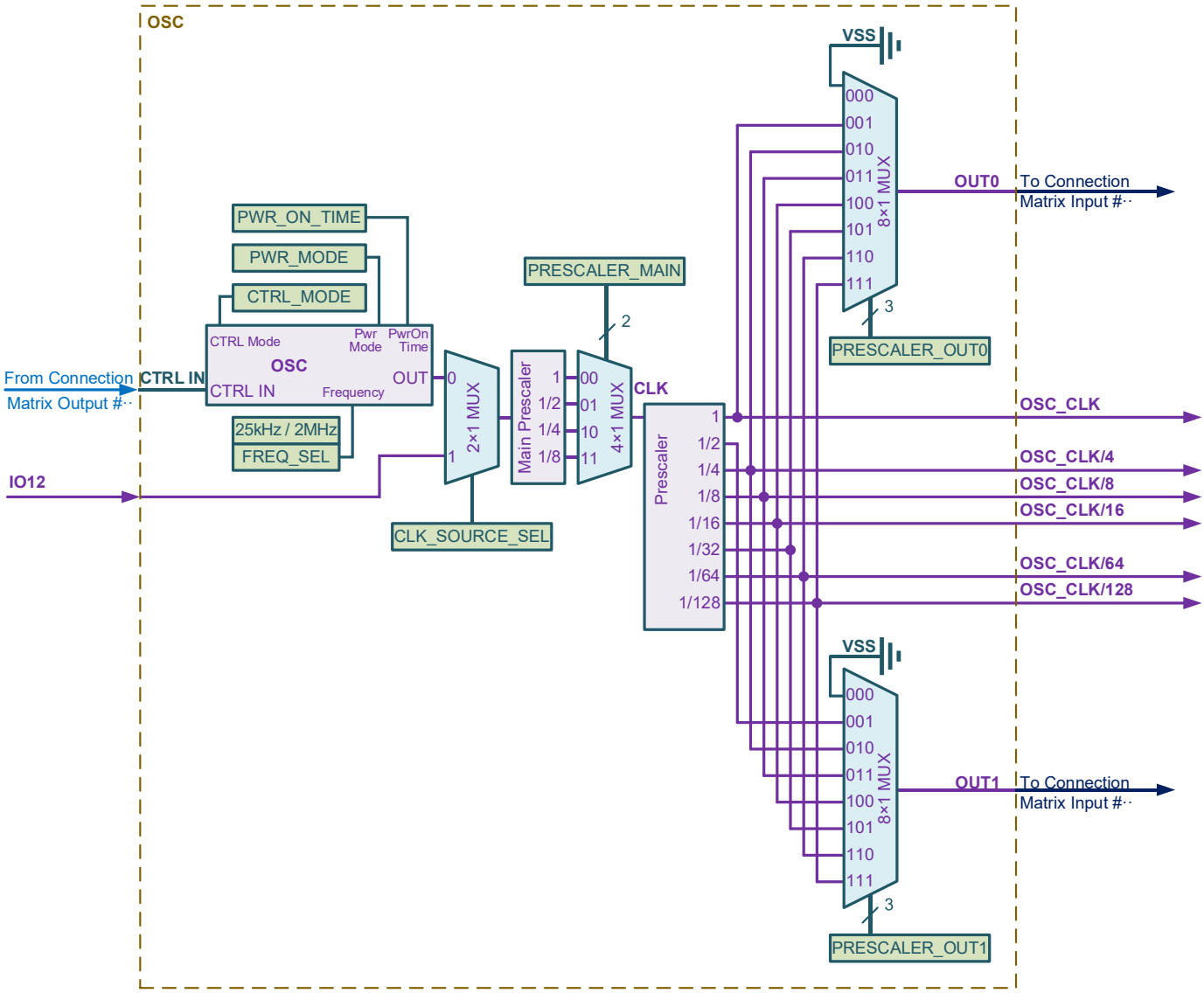


Figure 15.1. OSC0(25 kHz/2 MHz) Block Diagram

Table 15.3. OSC Registers

Register Bit Address	Register Name	Register Definition
OSC (25kHz/2MHz)		
<804>	OSC_FREQ_SEL	Frequency: 0: 25kHz 1: 2MHz
<805>	OSC_CTRL_MODE	Control Input mode control: 0: Power down 1: Force on
<806>	OSC_PWR_MODE	Power mode: 0: Auto power on 1: Forced power on
<807>	OSC_PWR_ON_TIME	Power on time: 0: Normal 1: Fast
<808>	OSC_CLK_SOURCE_SEL	Clock source: 0: Inner oscillator 1: External CLK

Register Bit Address	Register Name	Register Definition
OSC (25kHz/2MHz)		
<810:809>	OSC_PRESCALER_MAIN	Main prescaler: 00: 1 01: 1/2 10: 1/4 11: 1/8
<813:811>	OSC_PRESCALER_OUT0	OUT0 prescaler: 000: OUT0_DISABLE 001: OSC_CLK 010: OSC_CLK/4 011: OSC_CLK/8 100: OSC_CLK/16 101: OSC_CLK/32 110: OSC_CLK/64 111: OSC_CLK/128
<816:814>	OSC_PRESCALER_OUT1	OUT1 prescaler: 000: OUT1_DISABLE 001: OSC_CLK/2 010: OSC_CLK/4 011: OSC_CLK/8 100: OSC_CLK/16 101: OSC_CLK/32 110: OSC_CLK/64 111: OSC_CLK/128

16. POR

To ensure correct device initialization and operation of all macrocells in the device, the µASIC has a Power-On Reset (POR) circuit. The POR circuit achieves consistent behavior and predictable results during VDD power ramp-up and power-down. To accomplish this goal, the POR circuit releases a defined Power-Up sequence of internal events that initializes different macrocells inside the device.

16.1. POR General Operation

To start the Power-Up sequence, the voltage applied on the VDD should be higher than the POWER ON threshold (which can vary by PVT, but typically is 1.5 V). The operational V_{DD} range for the ALM1412 is 1.71V…5.50V. Therefore, the Power-Up sequence will start earlier, as soon as the V_{DD} rises to the POWER ON threshold, but the VDD voltage itself must continue to ramp up to the operational voltage value. After the POR sequence starts, the ALM1412 will have a period of time to go through all the steps in the sequence and will be ready and completely operational after the Power-Up sequence is completed.

The ALM1412 is powered down and non-operational when the VDD voltage is between 0.6 V and -0.6 V. Another essential condition for the chip to be powered down is that no voltage higher than the VDD voltage is applied to any other pin (although there is a 0.5 V margin due to forward drop voltage of the ESD protection diodes).

All pins are in HIGH IMPEDANCE state while the Power-Up sequence is taking place and when the chip is powered down. The last step in the Power-Up sequence releases the IO structures from the HIGH IMPEDANCE state making the device operational. The design programmed into the chip defines the pin configuration of the device when operational. (The voltage on the pins can not be higher than the VDD, and this rule does apply to when the chip is powered on).

16.2. Power-Up Sequence

The Power-Up sequence of signals is shown in Figure 16.1.

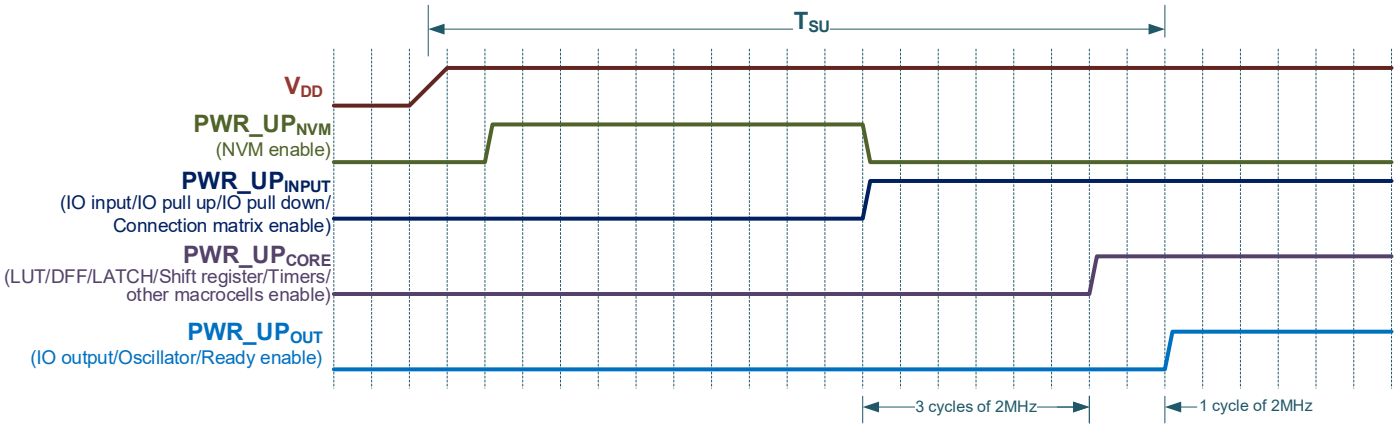


Figure 16.1. Power-Up sequence

As demonstrated by Figure 16.1 after the V_{DD} starts ramping up and crosses the POWER ON threshold, the on-chip NVM memory is enabled. After that, the Input pins and Connection Matrix are enabled and all traces between all macrocells are routed. The macrocells like LUT, DFF, LATCH, Shift Register, Timers, and others are initialized and stabilized for the next 3 cycles of the 2MHz oscillator. After another one cycle, the READY signal and OSC outputs are enabled, and the outputs start to run. The output pins transition from HIGH IMPEDANCE to active at this point.

The completion time for the Power Up sequence varies by device type in the µASIC family. The completion time also depends on many environmental factors such as: slew rate, V_{DD} value, temperature to a degree that the times will even vary from chip to chip due to process influence.

16.3. Macrocells Output States During Power-Up Sequence

First, all macrocells have their output set to logic LOW, except the output pins which are in HIGH IMPEDANCE state, before the NVM is enabled. Then until the NVM is ready, all macrocell outputs states are unpredictable except the IOs. On the next step Input pins determined by external signals, LOGIC 1 is high, LOGIC 0 is low, LUTs and PDLY macrocell configured as edge detector work according to their inputs. All other macrocells are initialized in the next step. Lastly, READY signal, oscillator, and the output pins become active as determined by the input signals. (Figure 16.2 describes the macrocell output signal states during the Power-Up sequence).

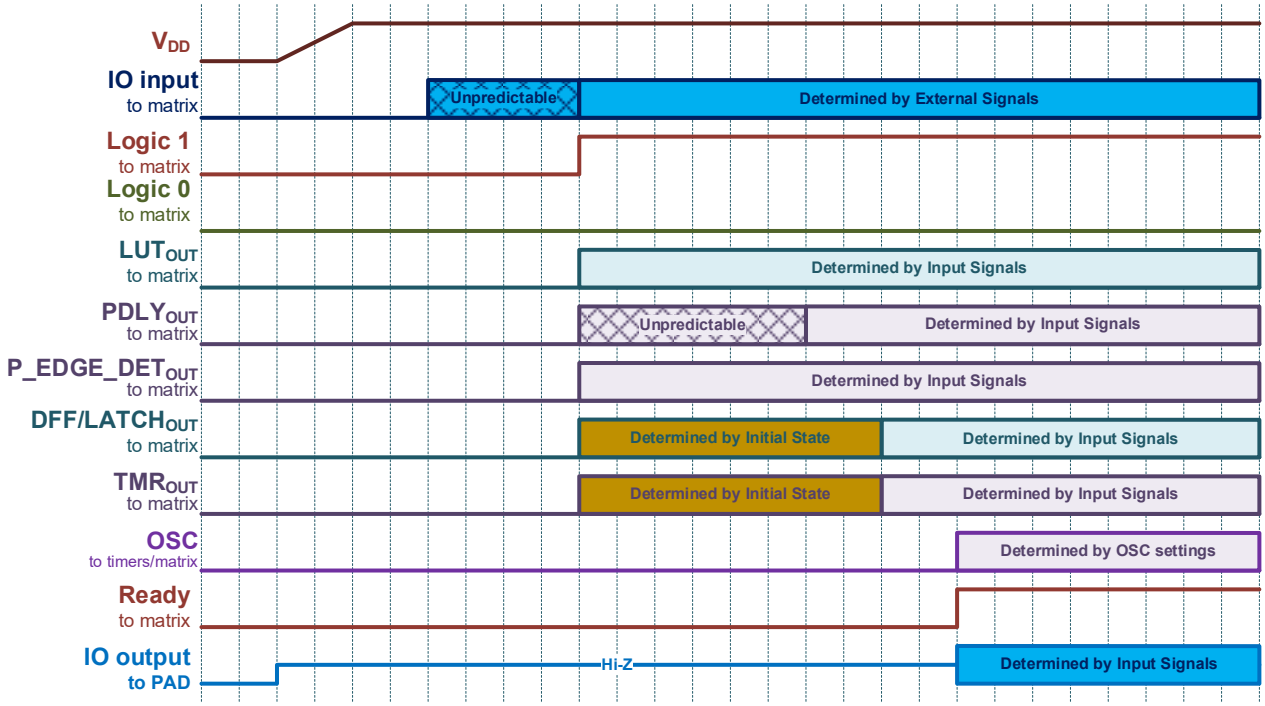


Figure 16.2. Internal Macrocell States during Power-Up sequence

16.4. Reset Events

There are number of reset events for ALM1412:

- POR;
- CRC-8;
- CRV;
- IO2 Reset.

The CRC-8 (see section 11.1), CRV (see section 11.2), and IO2 Reset can be enabled or disabled by the register bits (Table 16.1). Keep in mind that IO2 should be configured as a Digital Input (any of the input modes) as long as IO2 Reset is enabled.

Table 16.1 IO2 Reset Register Settings

Register Bit Address	Register Name	Register Definition
IO2 Reset		
<70>	IO2_RESET_EN	IO2 Reset: 0: Disable 1: Enable
<72:71>	IO2_RESET_TRIG	IO2 Reset Trigger Event: 00: Rising Edge 01: Falling Edge 10: High Level 11: Reserved

17. Abbreviations

ACMP	Analog Comparator
ADJ	Adjustable
AI	Analog Input
AIO	Analog Input/Output
AO	Analog Output
ASIC	Application-Specific Integrated Circuit
CLK	Clock
CLK/L	Clock/Latch
CRC	Cyclic Redundancy Code
CRV	Continuous Registers Verification
CM	Connection Matrix
CMI	Connection Matrix Inputs
CMO	Connection Matrix Outputs
CV	Counted Value
D	Data
DC	Direct Current
DFF	D Flip-Flop
DI	Digital Input
DIR	Direction
DILV	Digital Input Low Voltage
DIO	Digital Input/Output
ED	Edge Detector
ESD	Electrostatic Discharge
EXTCLK	External Clock
GND	Ground
IC	Integrated Circuit
IMC	Input Mode Control
IN	Input
IO	Input/Output
Logic 0	Low Logic Level
Logic 1	High Logic Level
LSB	Least Significant Bit
LUT	Look Up Table
LV	Low Voltage
MF	Multi-Functional
MSB	Most Significant Bit
MUX	Multiplexer
N/A	Not Applicable
N/C	Not Connected
NMOS	N channel Metal Oxide Semiconductor
NVM	Non-Volatile Memory
OD	Open Drain
OSC	Oscillator
OSG	One Shot Generator
OUT	Output
PDLY	Programmable Delay
PMOS	P channel Metal Oxide Semiconductor
POR	Power On Reset
PP	Push Pull
PROP	Propagation
PW	Pulse Width
PWRDWN	Power Down
REG	Register
RST	Reset
SHR	Shift Register
ST	Schmitt Trigger
TMR	Timer
TQFN	Thin Quad Flat No Leads
VDD	Voltage Drain-Drain
VSS	Voltage Source-Source
w/	With
w/o	Without

18. Appendix A – ALM1412 Register Definition

Register Bit Address	Register Name	Register Definition
System		
<15:0>		Reserved
<23:16>	SYS_PART_NUMBER_LSB	Project part number
<31:24>	SYS_PART_NUMBER_MSB	Project part number
<39:32>	SYS_SPARE_BYTE0	Spare byte
<47:40>	SYS_SPARE_BYTE1	Spare byte
<55:48>	SYS_PATTERN_ID	Project pattern ID
<59:56>		Reserved
Security Control		
<60>	SYS_SECURITY_CRC_EN	CRC verification: 0: Disable 1: Enable
<68:61>	SYS_SECURITY_CRC	CRC ($x^8+x^6+x^3+1$)
<69>	SYS_SECURITY_CRV_EN	Continuous register verification: 0: Disable 1: Enable
IO2 Reset		
<70>	IO2_RESET_EN	IO2 Reset: 0: Disable 1: Enable
<72:71>	IO2_RESET_TRIG	IO2 Reset Trigger Event: 00: Rising Edge 01: Falling Edge 10: High Level 11: Reserved
Reserved		
<73>		Reserved
CRV		
<74>	CRV_B0	CRV bit. If CRV is enabled, please make sure to keep the bit LOW
Reserved		
<78:75>		Reserved
Connection matrix outputs		
<84:79>	CMO0_IO3_DIN	IO3 DIN
<90:85>	CMO1_IO4_DIN	IO4 DIN
<96:91>	CMO2_IO5_DIN	IO5 DIN
<102:97>	CMO3_IO6_DIN	IO6 DIN
<108:103>	CMO4_IO8_DIN	IO8 DIN
<114:109>	CMO5_IO9_DIN	IO9 DIN
<120:115>	CMO6_IO10_DIN	IO10 DIN
<126:121>	CMO7_IO11_DIN	IO11 DIN
<132:127>	CMO8_IO12_DIN	IO12 DIN
<138:133>	CMO9_IO6_DIR	IO6 DIR
<144:139>	CMO10_IO10_DIR_VREF_PWR_ON	IO10 DIR shared with PWR_ON of VREF
<145>	CRV_B1	CRV bit. If CRV is enabled, please make sure to keep the bit HIGH
<151:146>	CMO11_OSC_CTRL_IN	OSC CTRL IN
<157:152>	CMO12_3BLUT0_IN0	3-bit LUT0 IN0
<163:158>	CMO13_3BLUT0_IN1	3-bit LUT0 IN1
<169:164>	CMO14_3BLUT0_IN2	3-bit LUT0 IN2
<175:170>	CMO15_3BLUT1_IN0	3-bit LUT1 IN0
<181:176>	CMO16_3BLUT1_IN1	3-bit LUT1 IN1
<187:182>	CMO17_3BLUT1_IN2	3-bit LUT1 IN2
<193:188>	CMO18_3BLUT2_IN0	3-bit LUT2 IN0
<199:194>	CMO19_3BLUT2_IN1	3-bit LUT2 IN1
<205:200>	CMO20_3BLUT2_IN2	3-bit LUT2 IN2
<211:206>	CMO21_3BLUT3_IN0	3-bit LUT3 IN0
<217:212>	CMO22_3BLUT3_IN1	3-bit LUT3 IN1
<223:218>	CMO23_3BLUT3_IN2	3-bit LUT3 IN2
<224>	CRV_B2	CRV bit. If CRV is enabled, please make sure to keep the bit HIGH
<230:225>	CMO24_MF0_2BLUT0_DFF0_IN0_CLK	MF0(2-bit LUT0/DFF0/LATCH0) IN0/CLK/nL
<236:231>	CMO25_MF0_2BLUT0_DFF0_IN1_D	MF0(2-bit LUT0/DFF0/LATCH0) IN1/D
<242:237>	CMO26_MF1_2BLUT1_DFF1_IN0_CLK	MF1(2-bit LUT1/DFF1/LATCH1) IN0/CLK/nL

Register Bit Address	Register Name	Register Definition
<248:243>	CMO27_MF1_2BLUT1_DFF1_IN1_D	MF1(2-bit LUT1/DFF1/LATCH1) IN1/D
<254:249>	CMO28_MF2_2BLUT2_DFF2_IN0_CLK	MF2(2-bit LUT2/DFF2/LATCH2) IN0/CLK/nL
<260:255>	CMO29_MF2_2BLUT2_DFF2_IN1_D	MF2(2-bit LUT2/DFF2/LATCH2) IN1/D
<266:261>	CMO30_MF3_2BLUT3_DFF3_IN0_CLK	MF3(2-bit LUT3/DFF3/LATCH3) IN0/CLK/nL
<272:267>	CMO31_MF3_2BLUT3_DFF3_IN1_D	MF3(2-bit LUT3/DFF3/LATCH3) IN1/D
<273>	CRV_B3	CRV bit. If CRV is enabled, please make sure to keep the bit HIGH
<279:274>	CMO32_MF4_3BLUT4_DFF4_IN0_CLK	MF4(3-bit LUT4/DFF4/LATCH4) IN0/CLK/nL
<285:280>	CMO33_MF4_3BLUT4_DFF4_IN1_D	MF4(3-bit LUT4/DFF4/LATCH4) IN1/D
<291:286>	CMO34_MF4_3BLUT4_DFF4_IN2_RST	MF4(3-bit LUT4/DFF4/LATCH4) IN2/(n)RST/(n)SET
<297:292>	CMO35_MF5_3BLUT5_DFF5_IN0_CLK	MF5(3-bit LUT5/DFF5/LATCH5) IN0/CLK/nL
<303:298>	CMO36_MF5_3BLUT5_DFF5_IN1_D	MF5(3-bit LUT5/DFF5/LATCH5) IN1/D
<309:304>	CMO37_MF5_3BLUT5_DFF5_IN2_RST	MF5(3-bit LUT5/DFF5/LATCH5) IN2/(n)RST/(n)SET
<315:310>	CMO38_MF6_3BLUT6_DFF6_IN0_CLK	MF6(3-bit LUT6/DFF6/LATCH6) IN0/CLK/nL
<321:316>	CMO39_MF6_3BLUT6_DFF6_IN1_D	MF6(3-bit LUT6/DFF6/LATCH6) IN1/D
<327:322>	CMO40_MF6_3BLUT6_DFF6_IN2_RST	MF6(3-bit LUT6/DFF6/LATCH6) IN2/(n)RST/(n)SET
<333:328>	CMO41_MF7_3BLUT7_DFF7_IN0_CLK	MF7(3-bit LUT7/DFF7/LATCH7) IN0/CLK/nL
<339:334>	CMO42_MF7_3BLUT7_DFF7_IN1_D	MF7(3-bit LUT7/DFF7/LATCH7) IN1/D
<345:340>	CMO43_MF7_3BLUT7_DFF7_IN2_RST	MF7(3-bit LUT7/DFF7/LATCH7) IN2/(n)RST/(n)SET
<346>	CRV_B4	CRV bit. If CRV is enabled, please make sure to keep the bit HIGH
<352:347>	CMO44_MF8_3BLUT8_SH_REG_IN0_CLK	MF8(3-bit LUT8/Shift Register) IN0/CLK
<358:353>	CMO45_MF8_3BLUT8_SH_REG_IN1_D	MF8(3-bit LUT8/Shift Register) IN1/D
<364:359>	CMO46_MF8_3BLUT8_SH_REG_IN2_nRST	MF8(3-bit LUT8/Shift Register) IN2/nRST
<370:365>	CMO47_MF9_3BLUT9_8BTMR1_IN2_CLK	MF9(3-bit LUT9/8-bit TMR1) IN0/CLK
<376:371>	CMO48_MF9_3BLUT9_8BTMR1_IN1_RST	MF9(3-bit LUT9/8-bit TMR1) IN1/IN/RST
<382:377>	CMO49_MF9_3BLUT9_8BTMR1_IN0_KEEP	MF9(3-bit LUT9/8-bit TMR1) IN2/KEEP
<383>	CRV_B5	CRV bit. If CRV is enabled, please make sure to keep the bit HIGH
<389:384>	CMO50_MF10_4BLUT0_8BTMR2_IN0_CLK	MF10(4-bit LUT0/8-bit TMR2) IN0/CLK
<395:390>	CMO51_MF10_4BLUT0_8BTMR2_IN1_RST	MF10(4-bit LUT0/8-bit TMR2) IN1/IN/RST
<401:396>	CMO52_MF10_4BLUT0_8BTMR2_IN2_KEEP	MF10(4-bit LUT0/8-bit TMR2) IN2/KEEP
<407:402>	CMO53_MF10_4BLUT0_8BTMR2_IN3	MF10(4-bit LUT0/8-bit TMR2) IN3
<413:408>	CMO54_MF11_4BLUT1_8BTMR3_IN0_CLK	MF11(4-bit LUT1/8-bit TMR3) IN0/CLK
<419:414>	CMO55_MF11_4BLUT1_8BTMR3_IN1_RST	MF11(4-bit LUT1/8-bit TMR3) IN1/IN/RST
<425:420>	CMO56_MF11_4BLUT1_8BTMR3_IN2_KEEP	MF11(4-bit LUT1/8-bit TMR3) IN2/KEEP
<431:426>	CMO57_MF11_4BLUT1_8BTMR3_IN3	MF11(4-bit LUT1/8-bit TMR3) IN3
<432>	CRV_B6	CRV bit. If CRV is enabled, please make sure to keep the bit LOW
<438:433>	CMO58_MF12_PDLY_ED_IN	MF12(PDLY/Edge Detector) IN
<444:439>	CMO59_16BTMR0_CLK_KEEP	16-bit TMR0 CLK/KEEP
<450:445>	CMO60_16BTMR0_IN_RST	16-bit TMR0 IN/RST
<456:451>	CMO61_ACMP0_PWR_ON	ACMP0 PWR ON
<462:457>	CMO62_ACMP1_PWR_ON	ACMP1 PWR ON
Reserved		
<470:463>		Reserved
IO2		
<472:471>	IO2_IMC	Input mode control: 00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Digital Input Low Voltage 11: Reserved
<473>	IO2_PULL_R_DOWN_UP_SEL	Pull resistor: 0: Down 1: Up
<475:474>	IO2_PULL_R_VAL	Pulled resistor value: 00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
CRV		
<476>	CRV_B7	CRV bit. If CRV is enabled, please make sure to keep the bit HIGH
IO3		

Register Bit Address	Register Name	Register Definition
<477>	IO3_DIR	Direction: 0: Input 1: Output
<478>	IO3_FORCE_IN_EN	Force input: 0: Disable 1: Enable (Input is always ON)
<480:479>	IO3_IMC	Input mode control: 00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Digital Input Low Voltage 11: Analog IO
<482:481>	IO3_OMC	Output mode control: 00: Push Pull 01: Open Drain NMOS 10: Open Drain PMOS 11: Reserved
<483>	IO3_DRIVE_STRENGTH	Drive strength: 0: ×1 1: ×2
<484>	IO3_PULL_R_DOWN_UP_SEL	Pull resistor: 0: Down 1: Up
<486:485>	IO3_PULL_R_VAL	Pulled resistor value: 00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
CRV		
<487>	CRV_B8	CRV bit. If CRV is enabled, please make sure to keep the bit LOW
IO4		
<488>	IO4_DIR	Direction: 0: Input 1: Output
<489>	IO4_FORCE_IN_EN	Force input: 0: Disable 1: Enable (Input is always ON)
<491:490>	IO4_IMC	Input mode control: 00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Digital Input Low Voltage 11: Analog IO
<493:492>	IO4_OMC	Output mode control: 00: Push Pull 01: Open Drain NMOS 10: Open Drain PMOS 11: Reserved
<494>	IO4_DRIVE_STRENGTH	Drive strength: 0: ×1 1: ×2
<495>	IO4_PULL_R_DOWN_UP_SEL	Pull resistor: 0: Down 1: Up
<497:496>	IO4_PULL_R_VAL	Pulled resistor value: 00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
CRV		
<498>	CRV_B9	CRV bit. If CRV is enabled, please make sure to keep the bit HIGH
IO5		
<499>	IO5_DIR	Direction: 0: Input 1: Output
<500>	IO5_FORCE_IN_EN	Force input: 0: Disable 1: Enable (Input is always ON)

Register Bit Address	Register Name	Register Definition
<502:501>	IO5_IMC	Input mode control: 00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Digital Input Low Voltage 11: Reserved
<504:503>	IO5_OMC	Output mode control: 00: Push Pull 01: Open Drain NMOS 10: Open Drain PMOS 11: Reserved
<505>	IO5_DRIVE_STRENGTH	Driver strength: 0: ×1 1: ×2
<506>	IO5_PULL_R_DOWN_UP_SEL	Pull resistor: 0: Down 1: Up
<508:507>	IO5_PULL_R_VAL	Pulled resistor value: 00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
CRV		
<509>	CRV_B10	CRV bit. If CRV is enabled, please make sure to keep the bit HIGH
IO6		
<510>	IO6_FORCE_IN_EN	Force input: 0: Disable 1: Enable (Input is always ON)
<512:511>	IO6_IMC	Input mode control: 00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Digital Input Low Voltage 11: Analog IO
<514:513>	IO6_OMC	Output mode control: 00: Push Pull 01: Open Drain NMOS 10: Open Drain PMOS 11: Reserved
<515>	IO6_DRIVE_STRENGTH	Drive strength: 0: ×1 1: ×2
<516>	IO6_PULL_R_DOWN_UP_SEL	Pull resistor: 0: Down 1: Up
<518:517>	IO6_PULL_R_VAL	Pulled resistor value: 00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
IO8		
<519>	IO8_DIR	Direction: 0: Input 1: Output
<520>	IO8_FORCE_IN_EN	Force input: 0: Disable 1: Enable (Input is always ON)
<522:521>	IO8_IMC	Input mode control: 00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Digital Input Low Voltage 11: Reserved
<524:523>	IO8_OMC	Output mode control: 00: Push Pull 01: Open Drain NMOS 10: Open Drain PMOS 11: Reserved
<525>	IO8_DRIVE_STRENGTH	Drive strength: 0: ×1 1: ×2

Register Bit Address	Register Name	Register Definition
<526>	IO8_PULL_R_DOWN_UP_SEL	Pull resistor: 0: Down 1: Up
<528:527>	IO8_PULL_R_VAL	Pulled resistor value: 00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
CRV		
<529>	CRV_B11	CRV bit. If CRV is enabled, please make sure to keep the bit HIGH
IO9		
<530>	IO9_DIR	Direction: 0: Input 1: Output
<531>	IO9_FORCE_IN_EN	Force input: 0: Disable 1: Enable (Input is always ON)
<533:532>	IO9_IMC	Input mode control: 00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Digital Input Low Voltage 11: Reserved
<535:534>	IO9_OMC	Output mode control: 00: Push Pull 01: Open Drain NMOS 10: Open Drain PMOS 11: Reserved
<536>	IO9_DRIVE_STRENGTH	Drive strength: 0: ×1 1: ×2
<537>	IO9_PULL_R_DOWN_UP_SEL	Pull resistor: 0: Down 1: Up
<539:538>	IO9_PULL_R_VAL	Pulled resistor value: 00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
CRV		
<540>	CRV_B12	CRV bit. If CRV is enabled, please make sure to keep the bit LOW
IO10		
<541>	IO10_DIR	Direction: 0: Input 1: Output
<542>	IO10_FORCE_IN_EN	Force input: 0: Disable 1: Enable (Input is always ON)
<544:543>	IO10_IMC	Input mode control: 00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Digital Input Low Voltage 11: Analog IO
<546:545>	IO10_OMC	Output mode control: 00: Push Pull 01: Open Drain NMOS 10: Open Drain PMOS 11: Reserved
<547>	IO10_DRIVE_STRENGTH	Drive strength: 0: ×1 1: ×2
<548>	IO10_PULL_R_DOWN_UP_SEL	Pull resistor: 0: Down 1: Up

Register Bit Address	Register Name	Register Definition
<550:549>	IO10_PULL_R_VAL	Pulled resistor value: 00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
<551>	IO10_DIR_SOURCE_SEL	Direction source selection: 0: Register IO10_DIR 1: Connection matrix CMO10
CRV		
<552>	CRV_B13	CRV bit. If CRV is enabled, please make sure to keep the bit HIGH
IO11		
<553>	IO11_DIR	Direction: 0: Input 1: Output
<554>	IO11_FORCE_IN_EN	Force input: 0: Disable 1: Enable (Input is always ON)
<556:555>	IO11_IMC	Input mode control: 00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Digital Input Low Voltage 11: Reserved
<558:557>	IO11_OMC	Output mode control: 00: Push Pull 01: Open Drain NMOS 10: Open Drain PMOS 11: Reserved
<559>	IO11_DRIVE_STRENGTH	Drive strength: 0: ×1 1: ×2
<560>	IO11_PULL_R_DOWN_UP_SEL	Pull resistor: 0: Down 1: Up
<562:561>	IO11_PULL_R_VAL	Pulled resistor value: 00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
CRV		
<563>	CRV_B14	CRV bit. If CRV is enabled, please make sure to keep the bit HIGH
IO12		
<564>	IO12_DIR	Direction: 0: Input 1: Output
<565>	IO12_FORCE_IN_EN	Force input: 0: Disable 1: Enable (Input is always ON)
<567:566>	IO12_IMC	Input mode control: 00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Digital Input Low Voltage 11: Reserved
<569:568>	IO12_OMC	Output mode control: 00: Push Pull 01: Open Drain NMOS 10: Open Drain PMOS 11: Reserved
<570>	IO12_DRIVE_STRENGTH	Drive strength: 0: ×1 1: ×2
<571>	IO12_PULL_R_DOWN_UP_SEL	Pull resistor: 0: Down 1: Up

Register Bit Address	Register Name	Register Definition
<573:572>	IO12_PULL_R_VAL	Pulled resistor value: 00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
CRV		
<574>	CRV_B15	CRV bit. If CRV is enabled, please make sure to keep the bit HIGH
3-bit LUT0		
<582:575>	3BLUT0_CTRL_DATA	OUT LUT control data
3-bit LUT1		
<590:583>	3BLUT1_CTRL_DATA	OUT LUT control data
3-bit LUT2		
<598:591>	3BLUT2_CTRL_DATA	OUT LUT control data
3-bit LUT3		
<606:599>	3BLUT3_CTRL_DATA	OUT LUT control data
Reserved		
<612:607>		Reserved
MF0 (2-bit LUT0/DFF0/LATCH0)		
<613>	MF0_MODE	MF mode: 0: LUT 1: DFF/LATCH
<614>	MF0_LUT_CTRL_DATA0_DFF_LATCH_SEL	0th bit of LUT control data: 0: LOW 1: HIGH or DFF/LATCH selection: 0: DFF 1: LATCH
<615>	MF0_LUT_CTRL_DATA1_DFF_LATCH_Q_POL	1st bit of LUT control data: 0: LOW 1: HIGH or Q polarity of DFF/LATCH: 0: Q 1: nQ
<616>	MF0_LUT_CTRL_DATA2_DFF_LATCH_INIT_STATE	2nd bit of LUT control data: 0: LOW 1: HIGH or Initial state of DFF/LATCH: 0: LOW 1: HIGH
<617>	MF0_LUT_CTRL_DATA3	3rd bit of LUT control data: 0: LOW 1: HIGH
CRV		
<618>	CRV_B16	CRV bit. If CRV is enabled, please make sure to keep the bit LOW
MF1 (2-bit LUT1/DFF1/LATCH1)		
<619>	MF1_MODE	MF mode: 0: LUT 1: DFF/LATCH
<620>	MF1_LUT_CTRL_DATA0_DFF_LATCH_SEL	0th bit of LUT control data: 0: LOW 1: HIGH or DFF/LATCH selection: 0: DFF 1: LATCH
<621>	MF1_LUT_CTRL_DATA1_DFF_LATCH_Q_POL	1st bit of LUT control data: 0: LOW 1: HIGH or Q polarity of DFF/LATCH: 0: Q 1: nQ

Register Bit Address	Register Name	Register Definition
<622>	MF1_LUT_CTRL_DATA2_DFF_LATCH_INIT_STATE	2nd bit of LUT control data: 0: LOW 1: HIGH or Initial state of DFF/LATCH: 0: LOW 1: HIGH
<623>	MF1_LUT_CTRL_DATA3	3rd bit of LUT control data: 0: LOW 1: HIGH
MF2 (2-bit LUT2/DFF2/LATCH2)		
<624>	MF2_MODE	MF mode: 0: LUT 1: DFF/LATCH
<625>	MF2_LUT_CTRL_DATA0_DFF_LATCH_SEL	0th bit of LUT control data: 0: LOW 1: HIGH or DFF/LATCH selection: 0: DFF 1: LATCH
<626>	MF2_LUT_CTRL_DATA1_DFF_LATCH_Q_POL	1st bit of LUT control data: 0: LOW 1: HIGH or Q polarity of DFF/LATCH: 0: Q 1: nQ
<627>	MF2_LUT_CTRL_DATA2_DFF_LATCH_INIT_STATE	2nd bit of LUT control data: 0: LOW 1: HIGH or Initial state of DFF/LATCH: 0: LOW 1: HIGH
<628>	MF2_LUT_CTRL_DATA3	3rd bit of LUT control data: 0: LOW 1: HIGH
CRV		
<629>	CRV_B17	CRV bit. If CRV is enabled, please make sure to keep the bit LOW
MF3 (2-bit LUT3/DFF3/LATCH3)		
<630>	MF3_MODE	MF mode: 0: LUT 1: DFF/LATCH
<631>	MF3_LUT_CTRL_DATA0_DFF_LATCH_SEL	0th bit of LUT control data: 0: LOW 1: HIGH or DFF/LATCH selection: 0: DFF 1: LATCH
<632>	MF3_LUT_CTRL_DATA1_DFF_LATCH_Q_POL	1st bit of LUT control data: 0: LOW 1: HIGH or Q polarity of DFF/LATCH: 0: Q 1: nQ
<633>	MF3_LUT_CTRL_DATA2_DFF_LATCH_INIT_STATE	2nd bit of LUT control data: 0: LOW 1: HIGH or Initial state of DFF/LATCH: 0: LOW 1: HIGH
<634>	MF3_LUT_CTRL_DATA3	3rd bit of LUT control data: 0: LOW 1: HIGH
CRV		

Register Bit Address	Register Name	Register Definition
<635>	CRV_B18	CRV bit. If CRV is enabled, please make sure to keep the bit HIGH
MF4 (3-bit LUT4/DFF4/LATCH4)		
<636>	MF4_MODE	MF mode: 0: LUT 1: DFF/LATCH
<637>	MF4_LUT_CTRL_DATA0_DFF_LATCH_SEL	0th bit of LUT control data: 0: LOW 1: HIGH or DFF/LATCH selection: 0: DFF 1: LATCH
<638>	MF4_LUT_CTRL_DATA1_DFF_LATCH_Q_POL	1st bit of LUT control data: 0: LOW 1: HIGH or Q polarity of DFF/LATCH: 0: Q 1: nQ
<639>	MF4_LUT_CTRL_DATA2_DFF_LATCH_RST_SET_SEL	2nd bit of LUT control data: 0: LOW 1: HIGH or reset/set selection: 0: (n)RST 1: (n)SET
<640>	MF4_LUT_CTRL_DATA3_DFF_LATCH_RST_SET_POL	3rd bit of LUT control data: 0: LOW 1: HIGH or reset/set polarity: 0: nRST(nSET) 1: RST(SET)
<641>	MF4_LUT_CTRL_DATA4_DFF_LATCH_INIT_STATE	4th bit of LUT control data: 0: LOW 1: HIGH or Initial state of DFF/LATCH: 0: LOW 1: HIGH
<642>	MF4_LUT_CTRL_DATA_5	5th bit of LUT control data: 0: LOW 1: HIGH
<643>	MF4_LUT_CTRL_DATA_6	6th bit of LUT control data: 0: LOW 1: HIGH
<644>	MF4_LUT_CTRL_DATA_7	7th bit of LUT control data: 0: LOW 1: HIGH
CRV		
<645>	CRV_B19	CRV bit. If CRV is enabled, please make sure to keep the bit HIGH
MF5 (3-bit LUT5/DFF5/LATCH5)		
<646>	MF5_MODE	MF mode: 0: LUT 1: DFF/LATCH
<647>	MF5_LUT_CTRL_DATA0_DFF_LATCH_SEL	0th bit of LUT control data: 0: LOW 1: HIGH or DFF/LATCH selection: 0: DFF 1: LATCH

Register Bit Address	Register Name	Register Definition
<648>	MF5_LUT_CTRL_DATA1_DFF_LATCH_Q_POL	1st bit of LUT control data: 0: LOW 1: HIGH or Q polarity of DFF/LATCH: 0: Q 1: nQ
<649>	MF5_LUT_CTRL_DATA2_DFF_LATCH_RST_SET_SEL	2nd bit of LUT control data: 0: LOW 1: HIGH or reset/set selection: 0: (n)RST 1: (n)SET
<650>	MF5_LUT_CTRL_DATA3_DFF_LATCH_RST_SET_POL	3rd bit of LUT control data: 0: LOW 1: HIGH or reset/set polarity: 0: nRST(nSET) 1: RST(SET)
<651>	MF5_LUT_CTRL_DATA4_DFF_LATCH_INIT_STATE	4th bit of LUT control data: 0: LOW 1: HIGH or Initial state of DFF/LATCH: 0: LOW 1: HIGH
<652>	MF5_LUT_CTRL_DATA_5	5th bit of LUT control data: 0: LOW 1: HIGH
<653>	MF5_LUT_CTRL_DATA_6	6th bit of LUT control data: 0: LOW 1: HIGH
<654>	MF5_LUT_CTRL_DATA_7	7th bit of LUT control data: 0: LOW 1: HIGH
CRV		
<655>	CRV_B20	CRV bit. If CRV is enabled, please make sure to keep the bit LOW
MF6 (3-bit LUT6/DFF6/LATCH6)		
<656>	MF6_MODE	MF mode: 0: LUT 1: DFF/LATCH
<657>	MF6_LUT_CTRL_DATA0_DFF_LATCH_SEL	0th bit of LUT control data: 0: LOW 1: HIGH or DFF/LATCH selection: 0: DFF 1: LATCH
<658>	MF6_LUT_CTRL_DATA1_DFF_LATCH_Q_POL	1st bit of LUT control data: 0: LOW 1: HIGH or Q polarity of DFF/LATCH: 0: Q 1: nQ
<659>	MF6_LUT_CTRL_DATA2_DFF_LATCH_RST_SET_SEL	2nd bit of LUT control data: 0: LOW 1: HIGH or reset/set selection: 0: (n)RST 1: (n)SET

Register Bit Address	Register Name	Register Definition
<660>	MF6_LUT_CTRL_DATA3_DFF_LATCH_RST_SET_POL	3rd bit of LUT control data: 0: LOW 1: HIGH or reset/set polarity: 0: nRST(nSET) 1: RST(SET)
<661>	MF6_LUT_CTRL_DATA4_DFF_LATCH_INIT_STATE	4th bit of LUT control data: 0: LOW 1: HIGH or Initial state of DFF/LATCH: 0: LOW 1: HIGH
<662>	MF6_LUT_CTRL_DATA_5	5th bit of LUT control data: 0: LOW 1: HIGH
<663>	MF6_LUT_CTRL_DATA_6	6th bit of LUT control data: 0: LOW 1: HIGH
<664>	MF6_LUT_CTRL_DATA_7	7th bit of LUT control data: 0: LOW 1: HIGH
CRV		
<665>	CRV_B21	CRV bit. If CRV is enabled, please make sure to keep the bit HIGH
MF7 (3-bit LUT7/DFF7/LATCH7)		
<666>	MF7_MODE	MF mode: 0: LUT 1: DFF/LATCH
<667>	MF7_LUT_CTRL_DATA0_DFF_LATCH_SEL	0th bit of LUT control data: 0: LOW 1: HIGH or DFF/LATCH selection: 0: DFF 1: LATCH
<668>	MF7_LUT_CTRL_DATA1_DFF_LATCH_Q_POL	1st bit of LUT control data: 0: LOW 1: HIGH or Q polarity of DFF/LATCH: 0: Q 1: nQ
<669>	MF7_LUT_CTRL_DATA2_DFF_LATCH_RST_SET_SEL	2nd bit of LUT control data: 0: LOW 1: HIGH or reset/set selection: 0: (n)RST 1: (n)SET
<670>	MF7_LUT_CTRL_DATA3_DFF_LATCH_RST_SET_POL	3rd bit of LUT control data: 0: LOW 1: HIGH or reset/set polarity: 0: nRST(nSET) 1: RST(SET)
<671>	MF7_LUT_CTRL_DATA4_DFF_LATCH_INIT_STATE	4th bit of LUT control data: 0: LOW 1: HIGH or Initial state of DFF/LATCH: 0: LOW 1: HIGH
<672>	MF7_LUT_CTRL_DATA_5	5th bit of LUT control data: 0: LOW 1: HIGH

Register Bit Address	Register Name	Register Definition
<673>	MF7_LUT_CTRL_DATA_6	6th bit of LUT control data: 0: LOW 1: HIGH
<674>	MF7_LUT_CTRL_DATA_7	7th bit of LUT control data: 0: LOW 1: HIGH
CRV		
<675>	CRV_B22	CRV bit. If CRV is enabled, please make sure to keep the bit HIGH
MF8 (3-bit LUT8/Shift Register)		
<676>	MF8_MODE	MF mode: 0: LUT 1: Shift register
<677>	MF8_SHIFT_REG_OUT1_POL	Shift register OUT1 polarity: 0: OUT1 1: nOUT1
<681:678>	MF8_LUT_CTRL_DATA3_0_SHIFT_REG_STAGE_OUT0	Low tetrad of OUT0 LUT control data or stage of OUT0 shift register
<685:682>	MF8_LUT_CTRL_DATA7_4_SHIFT_REG_STAGE_OUT1	High tetrad of OUT0 LUT control data or stage of OUT1 shift register
<693:686>	MF8_CTRL_DATA1	OUT1 LUT control data
<701:694>	MF8_CTRL_DATA2	OUT2 LUT control data
CRV		
<702>	CRV_B23	CRV bit. If CRV is enabled, please make sure to keep the bit HIGH
MF9 (3-bit LUT9/8-bit TMR1)		
<703>	MF9_MODE	MF mode: 0: LUT 1: Timer
<706:704>	MF9_TMR_MODE	Timer mode: 000: Delay 001: One shot 010: Frequency detector 011: Counter 100: Edge detector 101: Delayed edge detector 110: Reserved 111: Reserved
<708:707>	MF9_TMR_TRIG_EVENT	Timer trigger event: 00: On both falling and rising edges 01: On falling edge only 10: On rising edge only 11: High level reset (counter)
<711:709>	MF9_TMR_CLK	CLK source: 000: External CLK 001: OSC 010: OSC/4 011: OSC/8 100: OSC/16 101: OSC/64 110: OSC/128 111: Reserved
<712>	MF9_TMR_OSC_FORCE_EN	Force OSC by timer: 0: Disable 1: Enable
<714:713>	MF9_TMR_INIT_STATE	Timer initial state: 00: Initial 0 01: Initial 1 10: Bypass initial 11: Bypass initial
<715>	MF9_TMR_OUT_POL	Polarity of timer output: 0: OUT 1: nOUT
<723:716>	MF9_CTRL_DATA	MF control data
CRV		
<724>	CRV_B24	CRV bit. If CRV is enabled, please make sure to keep the bit LOW
MF10 (4-bit LUT0/8-bit TMR2)		

Register Bit Address	Register Name	Register Definition
<725>	MF10_MODE	MF mode: 0: LUT 1: Timer
<726>	MF10_TMR_OSC_FORCE_EN	Force OSC by timer: 0: Disable 1: Enable
<728:727>	MF10_TMR_INIT_STATE	Timer initial state: 00: Initial 0 01: Initial 1 10: Bypass initial 11: Bypass initial
<729>	MF10_TMR_OUT_POL	Polarity of timer output: 0: OUT 1: nOUT
<737:730>	MF10_CTRL_DATAL	MF low byte of control data
<740:738>	MF10_LUT_CTRL_DATAH2_0_TMR_MODE	<2:0> bits of LUT high byte control data or Timer mode: 000: Delay 001: One shot 010: Frequency detector 011: Counter 100: Edge detector 101: Delayed edge detector 110: Reserved 111: Reserved
<742:741>	MF10_LUT_CTRL_DATAH4_3_TMR_TRIG_EVENT	<4:3> bits of LUT high byte control data or Timer trigger event: 00: On both falling and rising edges 01: On falling edge only 10: On rising edge only 11: High level reset (counter)
<745:743>	MF10_LUT_CTRL_DATAH7_5_TMR_CLK	<7:5> bits of LUT high byte control data or CLK source: 000: External CLK 001: OSC 010: OSC/4 011: OSC/8 100: OSC/16 101: OSC/64 110: OSC/128 111: Reserved
CRV		
<746>	CRV_B25	CRV bit. If CRV is enabled, please make sure to keep the bit LOW
MF11 (4-bit LUT1/8-bit TMR3)		
<747>	MF11_MODE	MF mode: 0: LUT 1: Timer
<748>	MF11_TMR_OSC_FORCE_EN	Force OSC by timer: 0: Disable 1: Enable
<750:749>	MF11_TMR_INIT_STATE	Timer initial state: 00: Initial 0 01: Initial 1 10: Bypass initial 11: Bypass initial
<751>	MF11_TMR_OUT_POL	Polarity of timer output: 0: OUT 1: nOUT
<759:752>	MF11_CTRL_DATAL	MF low byte of control data

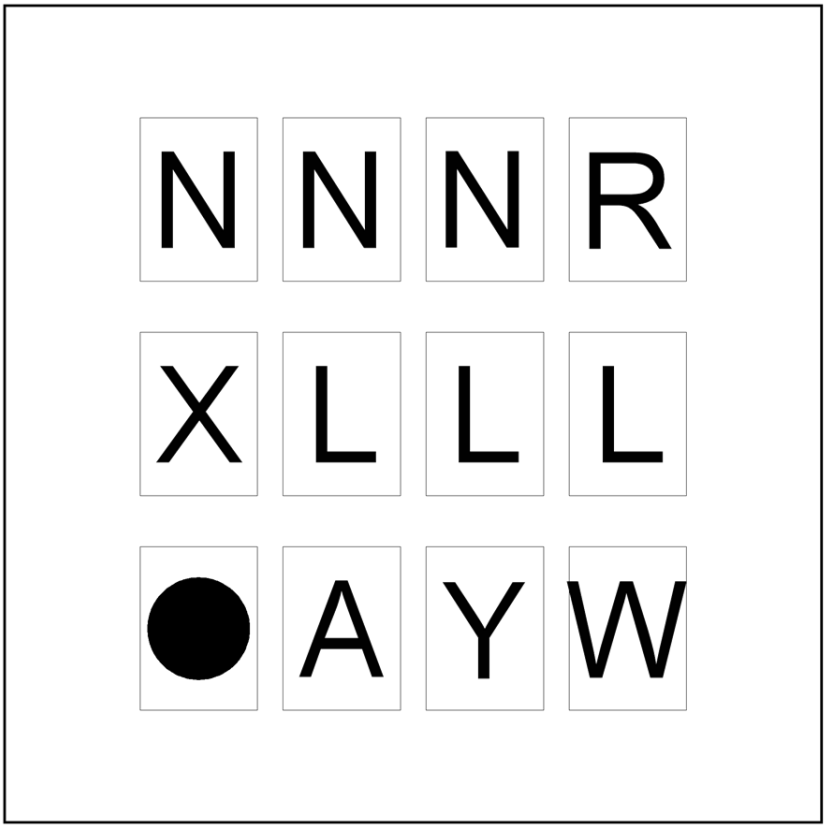
Register Bit Address	Register Name	Register Definition
<762:760>	MF11_LUT_CTRL_DATAH2_0_TMR_MODE	<2:0> bits of LUT high byte control data or Timer mode: 000: Delay 001: One shot 010: Reserved 011: Counter 100: Edge detector 101: Delayed edge detector 110: Reserved 111: Reserved
<764:763>	MF11_LUT_CTRL_DATAH4_3_TMR_TRIG_EVENT	<4:3> bits of LUT high byte control data or Timer trigger event: 00: On both falling and rising edges 01: On falling edge only 10: On rising edge only 11: High level reset (counter)
<767:765>	MF11_LUT_CTRL_DATAH7_5_TMR_CLK	<7:5> bits of LUT high byte control data or CLK source: 000: External CLK 001: OSC 010: OSC/4 011: OSC/8 100: OSC/16 101: OSC/64 110: OSC/128 111: Reserved
CRV		
<768>	CRV_B26	CRV bit. If CRV is enabled, please make sure to keep the bit HIGH
MF12 (PDLY/Edge Detector)		
<770:769>	MF12_MODE	MF mode: 00: Rising edge detector 01: Falling edge detector 10: Both edge detector 11: Both edge delay
<771>	MF12_OUT_POL	Output polarity: 0: OUT 1: nOUT
<773:772>	MF12_DELAY_VAL	Delay value: 00: 140ns 01: 280ns 10: 420ns 11: 560ns
16-bit TMR0		
<776:774>	TMR0_MODE	Timer mode: 000: Delay 001: One shot 010: Frequency detector 011: Counter 100: Edge detector 101: Delayed edge detector 110: Wake&Sleep 111: Reserved
<778:777>	TMR0_TRIG_EVENT	Timer trigger event: 00: On both falling and rising edges 01: On falling edge only 10: On rising edge only 11: High level reset (counter)
<781:779>	TMR0_CLK	CLK source: 000: External CLK 001: OSC 010: OSC/4 011: OSC/8 100: OSC/16 101: OSC/64 110: OSC/128 111: Reserved

Register Bit Address	Register Name	Register Definition
<782>	TMR0_CLK_KEEP_SEL	Input mode selection: 0: CLK 1: KEEP
<783>	TMR0_OSC_FORCE_EN	Force OSC by timer: 0: Disable 1: Enable
<785:784>	TMR0_INIT_STATE	Timer initial state: 00: Initial 0 01: Initial 1 10: Bypass initial 11: Bypass initial
<786>	TMR0_OUT_POL	Polarity of timer output: 0: OUT 1: nOUT
<794:787>	TMR0_CTRL_DATAL	Low byte of control data
<802:795>	TMR0_CTRL_DATAH	High byte of control data
CRV		
<803>	CRV_B27	CRV bit. If CRV is enabled, please make sure to keep the bit LOW
OSC (25kHz/2MHz)		
<804>	OSC_FREQ_SEL	Frequency: 0: 25kHz 1: 2MHz
<805>	OSC_CTRL_MODE	Control Input mode control: 0: Power down 1: Force on
<806>	OSC_PWR_MODE	Power mode: 0: Auto power on 1: Forced power on
<807>	OSC_PWR_ON_TIME	Power on time: 0: Normal 1: Fast
<808>	OSC_CLK_SOURCE_SEL	Clock source: 0: Inner oscillator 1: External CLK
<810:809>	OSC_PRESCALER_MAIN	Main prescaler: 00: 1 01: 1/2 10: 1/4 11: 1/8
<813:811>	OSC_PRESCALER_OUT0	OUT0 prescaler: 000: OUT0_DISABLE 001: OSC_CLK 010: OSC_CLK/4 011: OSC_CLK/8 100: OSC_CLK/16 101: OSC_CLK/32 110: OSC_CLK/64 111: OSC_CLK/128
<816:814>	OSC_PRESCALER_OUT1	OUT1 prescaler: 000: OUT1_DISABLE 001: OSC_CLK/2 010: OSC_CLK/4 011: OSC_CLK/8 100: OSC_CLK/16 101: OSC_CLK/32 110: OSC_CLK/64 111: OSC_CLK/128
<828:817>		Reserved
CRV		
<829>	CRV_B28	CRV bit. If CRV is enabled, please make sure to keep the bit HIGH
ACMP0		
<831:830>	ACMP0_IN_SOURCE	IN+ source: 00: IO3 01: Buffered IO3 10: Reserved 11: VDD

Register Bit Address	Register Name	Register Definition
<833:832>	ACMP0_GAIN	IN+ gain: 00: 1.00× 01: 0.50× 10: 0.33× 11: 0.25×
<835:834>	ACMP0_HYSTERESIS_MODE	Hysteresis mode: 00: No hysteresis (see Note 12.1) 01: 25mV 10: Custom hysteresis 11: Reserved
<836>	ACMP0_MODE	Mode: 0: High speed 1: Low power (see Note 12.2)
<837>	ACMP0_WS_EN	Wake&Sleep: 0: Disable 1: Enable
<842:838>	ACMP0_VREFL	High to Low threshold: see Table 13.1
<847:843>	ACMP0_VREFH	Low to High threshold: see Table 13.1
CRV		
<848>	CRV_B29	CRV bit. If CRV is enabled, please make sure to keep the bit LOW
ACMP1		
<850:849>	ACMP1_IN_SOURCE	IN+ source: 00: IO8 01: Buffered IO8 10: ACMP0 IN+ 11: Reserved
<852:851>	ACMP1_GAIN	IN+ gain: 00: 1.00× 01: 0.50× 10: 0.33× 11: 0.25×
<854:853>	ACMP1_HYSTERESIS_MODE	Hysteresis mode: 00: No hysteresis (see Note 12.3) 01: 25mV 10: Custom hysteresis 11: Reserved
<855>	ACMP1_MODE	Mode: 0: High speed 1: Low power (see Note 12.4)
<856>	ACMP1_WS_EN	Wake&Sleep: 0: Disable 1: Enable
<861:857>	ACMP1_VREFL	High to Low threshold: see Table 13.1
<866:862>	ACMP1_VREFH	Low to High threshold: see Table 13.1
CRV		
<867>	CRV_B30	CRV bit. If CRV is enabled, please make sure to keep the bit HIGH
VREF		
<869:868>	VREF_PWR_ON	VREF output to IO10 power on: 00: Power Off 01: Power On 10: Controlled by Connection Matrix 11: Controlled by Connection Matrix
<874:870>	VREF_IO_VALUE	VREF IO value: see Table 13.1
Reserved		
<880:875>		Reserved
CRV		
<881>	CRV_B31	CRV bit. If CRV is enabled, please make sure to keep the bit LOW
100µA Current Source		
<882>	CURR_SOURCE_TURN_ON	Turn on current source: 0: 100µA turn off 1: 100µA turn on

Register Bit Address	Register Name	Register Definition
Reserved		
<1023:883>		Reserved

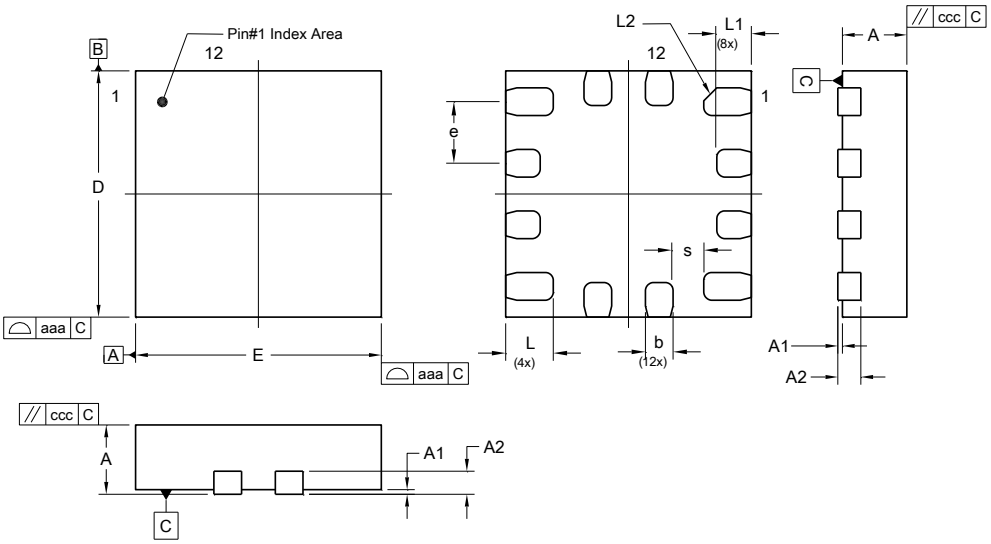
19. Package Top Marking System Definition



N - Identification Code
R - Project Revision
X - Internal Code
L - Lot ID
A - Assembly site ID
Y - Assembly Year
W - Assembly Week

20. Package Drawing and Dimensions

X1-QFN1616-12 (Type AX)



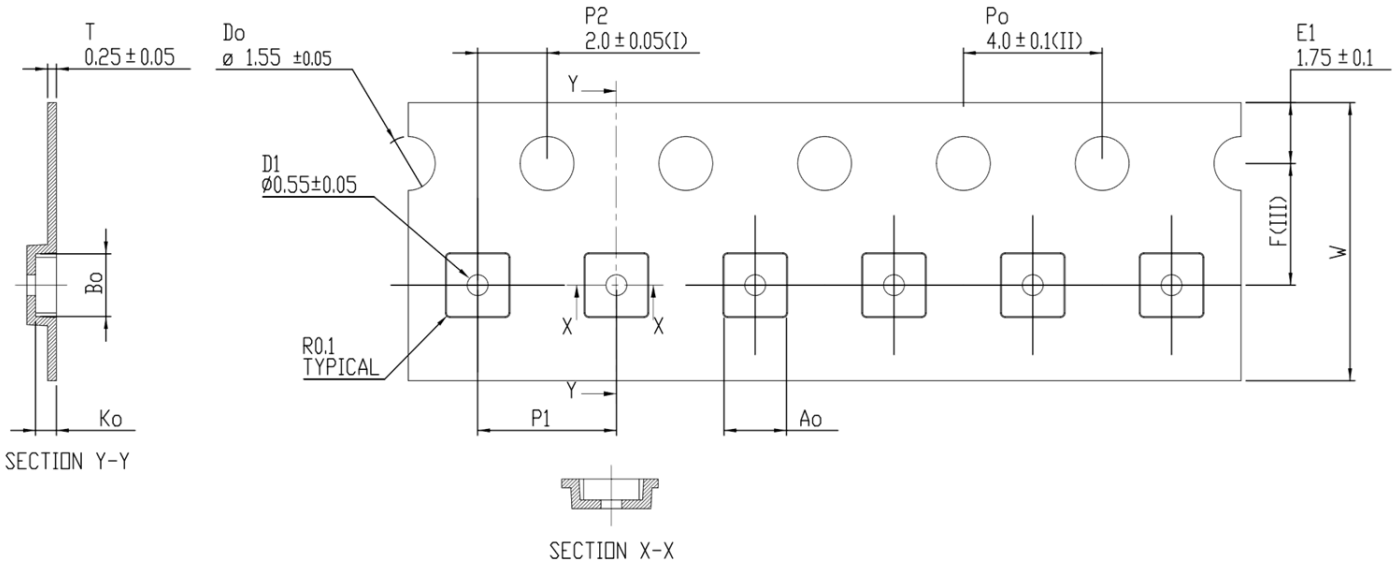
X1-QFN1616-12 (Type AX)			
Dim	**Min**	**Max**	**Typ**
A	0.370	0.470	0.420
A1	-0.005	0.030	--
A2	0.100	0.150	0.120
b	0.130	0.230	0.180
D	1.55	1.65	1.60
E	1.55	1.65	1.60
e	0.40 BSC		
L	0.260	0.360	0.310
L1	0.175	0.275	0.225
L2	0.100	0.120	0.1196
s	--	--	0.20
aaa	0.05		
ccc	0.05		
All Dimensions in mm			

21. Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size, mm	Max Units		per Reel & Hub Size, mm	Leader (min)		Trailer (min)		Tape Width, mm	Part Pitch, mm
			per Reel	per Box		Pockets	Length, mm	Pockets	Length, mm		
X1-QFN1616-12 (Type AX)	12	**Error! Bookmark not defined. × Error! Bookmark not defined. × Error! Bookmark not defined.**	3000	3000	178/54	100	400	100	400	8	4

21.1. Carrier Tape Drawing and Dimensions

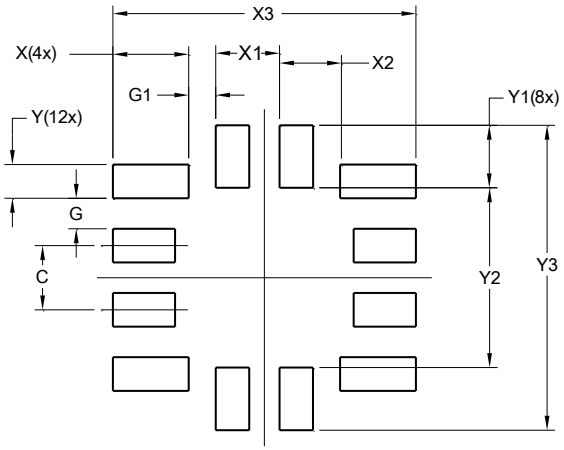
Package Type	Ao	Bo	Do	D1	E1	F	Po	P1	P2	R	T	W
BD0160X0160D	1.80	1.80	Ø1.55	Ø0.55	1.75	3.50	4.0	4.00	2.0	0.1	0.25	8.00



Note 21.1 All dimensions in millimeters unless otherwise stated.

22. Recommended Land Pattern

X1-QFN1616-12 (Type AX)



Dimensions	Value (in mm)
C	0.400
G	0.190
G1	0.170
X	0.475
X1	0.400
X2	0.380
X3	1.900
Y	0.210
Y1	0.390
Y2	1.120
Y3	1.900

23. Mechanical Data

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – NiPdAu. Solderable per MIL-STD-202, Method 208 e4
- Weight: 0.0028 grams (Approximate)

24. Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 1.0752 mm^3 (nominal). More information can be found at www.jedec.org.

25. Revision History

Date	Version	Change
July 04,2023	Rev.001	Initial version.
January 26, 2024	Rev.002	Updated diagrams, figures, and register names. Fixed typos.
September 2, 2025	Rev.003	Updated sections: 4. Electrical Specifications, 19. Package Top Marking System Definition, 20. Package Drawing and Dimensions, 21. Tape and Reel Specifications. Added a section 23. Mechanical Data. Updated figures: Figure 1.5, Figure 8.1, Figure 8.2, Figure 8.11, Figure 16.1. Added Figure 8.13. Updated Table 8.3, Table 8.14. Updated Registers: <370:365>, <382:377>.

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