



# ZXCT211 PSpice Model Validation Report

15/03/2024



## ZXCT211

Version	Details	Author	Date	REMARKS
1.0	PSpice Results	Sankalp	15MAR2024	Initial Release

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# Spec Compliance Matrix

PARAMETER	SYMBOL	TEST CONDITION	DATASHEET VALUE			PSPICE VALUE	UNIT
			Min	Typ	Max		
Common-Mode Input	VCM	TA = -40°C to +125°C	-0.3	--	26	(-0.3)-26	V
Common – Mode Rejection	CMRR	VIN+ = 0V to 26V, VSENSE = 0mV, TA = -40°C to +125°C	100	120	--	126	dB
Offset voltage	VOS	VSENSE = 0mV	--	+0.55	+35	+35	uA
Vos vs Temperature	dVos/dT	TA = -40°C to +125°C	--	0.1	--	0.1	uV/°C
Power supply rejection	PSRR	VS = 2.7V to 18V, VIN+ = 18V, VSENSE = 0mV	--	+0.1	+10	+0.1	uV/V
Input bias current	IB	VSENSE = 0mV	--	28	35	28	uA
Gain	G	--	--	500	--	500	V/V

# Spec Compliance Matrix

PARAMETER	SYMBOL	TEST CONDITION	DATASHEET VALUE			PSPICE VALUE	UNIT
			Min	Typ	Max		
Gain Error	EG	A and B Version, VSENSE = -5mV to 5mV, TA = -40°C to +125°C	--	+0.03	+0.8	+0.5482	%
		C Version, VSENSE = -5mV to 5mV, TA = -40°C to +125°C	--	+0.03	+0.8	+0.5482	
Swing to V+ Power-supply Rail	V <sub>OH</sub>	RL = 10kΩ to GND, TA = -40°C to +125°C	--	(V+)-0.05	(V+)-0.2	(V+)-0.05	V
Swing to GND	V <sub>OL</sub>	RL = 10kΩ to GND, TA = -40°C to +125°C	--	(VGND)+0.005	(VGND)+0.05	(VGND)+0.005	V
Operating voltage range	V <sub>S</sub>	TA = -40°C to +125°C	2.7	--	26	2.7-26	V
Quiescent Current	I <sub>Q</sub>	VSENSE = 0mV	--	65	100	65	uA

# Analysis Parameter

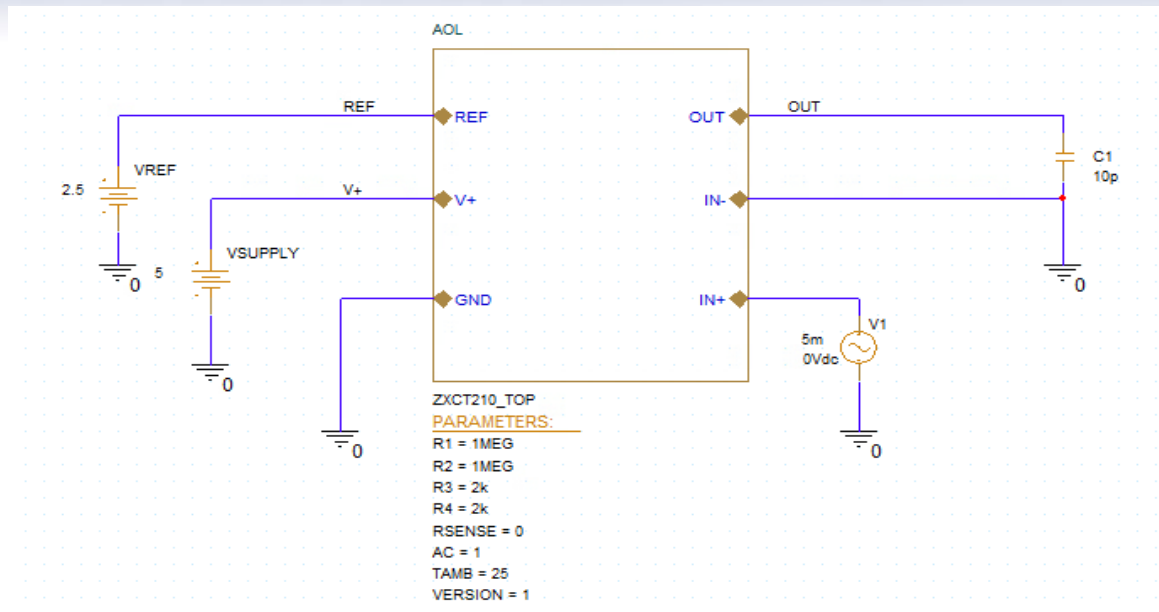
Parameter	Value
VNTOL	5u
ABSTOL	1n
CHGTOL	1p
ITL4	40
TIME STEP	10n

Note: Remaining parameters are set to the default values of Allegro Pspice 17.4.

# AC Analysis

# Frequency Response Test Setup and Condition

Test Condition: VSUPPLY=5V, VREF=2.5V, FREQ=10Hz – 10MHz



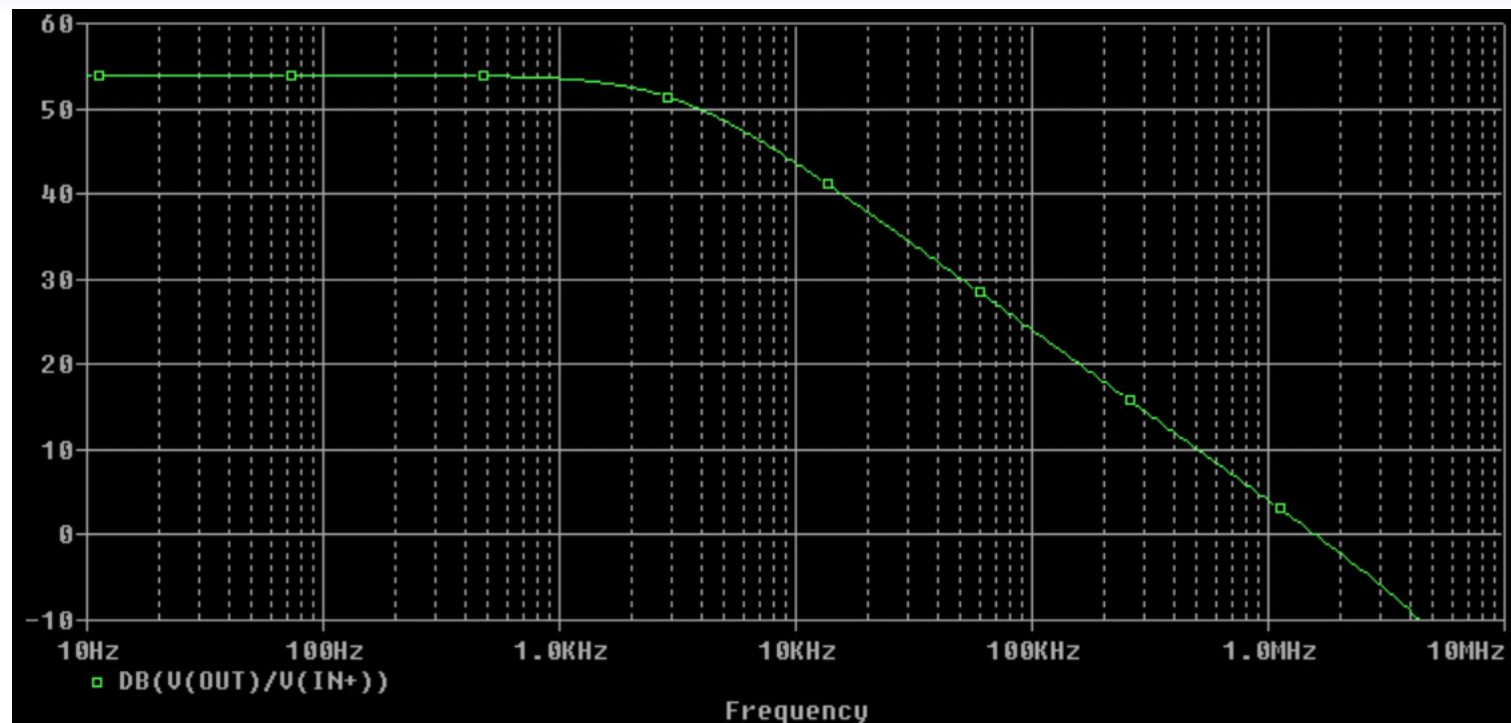
## Testbench Description

- The above testbench has been set-up to observe the frequency response of the device.
- Keep AC=1 : For AC analysis; Keep AC=0 : For transient analysis.
- Time taken for the simulation to complete which runs for the frequency range of 10Hz to 10MHz = Few seconds.



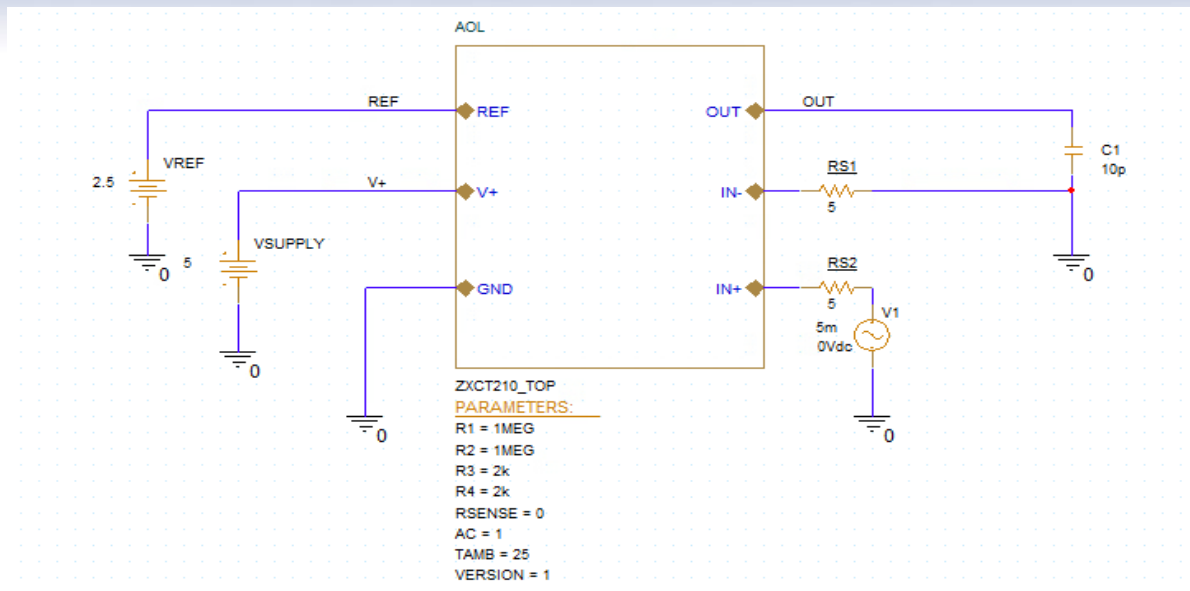
# PSpice Simulation Result / Datasheet

P-Spice Result



# Gain Error Test Setup and Condition

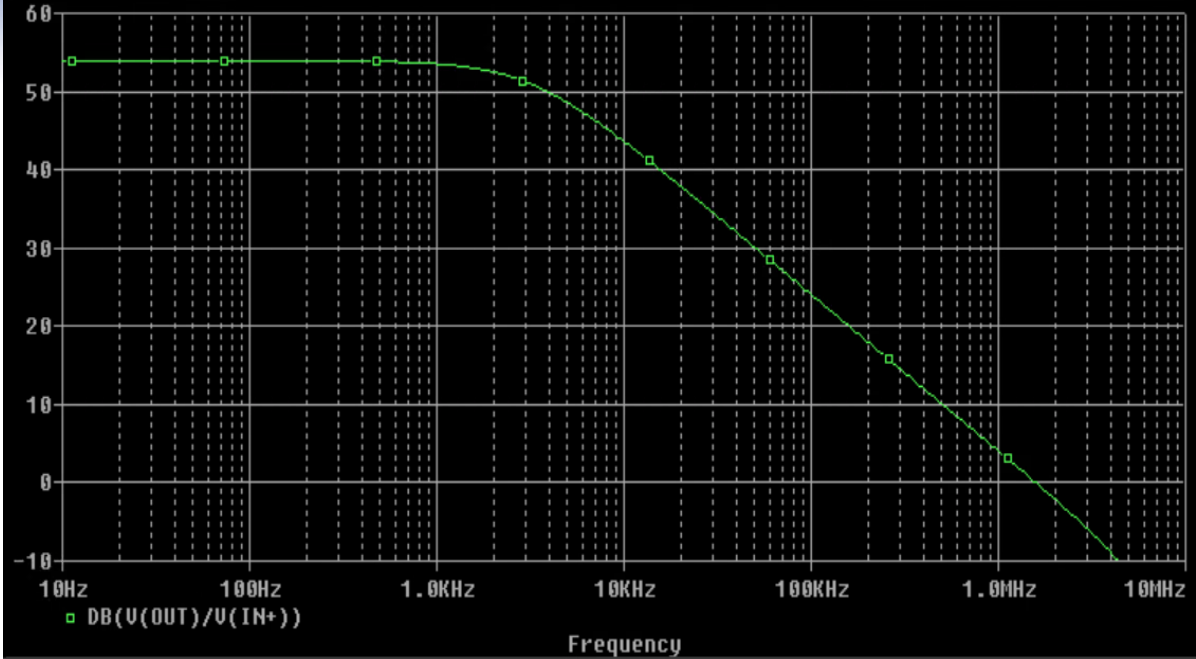
Test Condition: VSUPPLY=5V, VREF=2.5V, FREQ=10Hz – 10MHz



## Testbench Description

- The above testbench has been set-up to observe the frequency response of the device. The Error is inducted in the device by changing the values of the source resistors, RS1 & RS2
- Keep AC=1 : For AC analysis; Keep AC=0 : For transient analysis.
- Time taken for the simulation to complete which runs for the frequency range of 10Hz to 10MHz = Few seconds.

# PSPice Simulation Result



When  $R_s (=5\Omega)$  is connected,  
Gain = 53.936 dB = 498 V/V

When  $R_s (=5\Omega)$  is not connected,  
Gain = 53.897 dB = 495.27 V/V

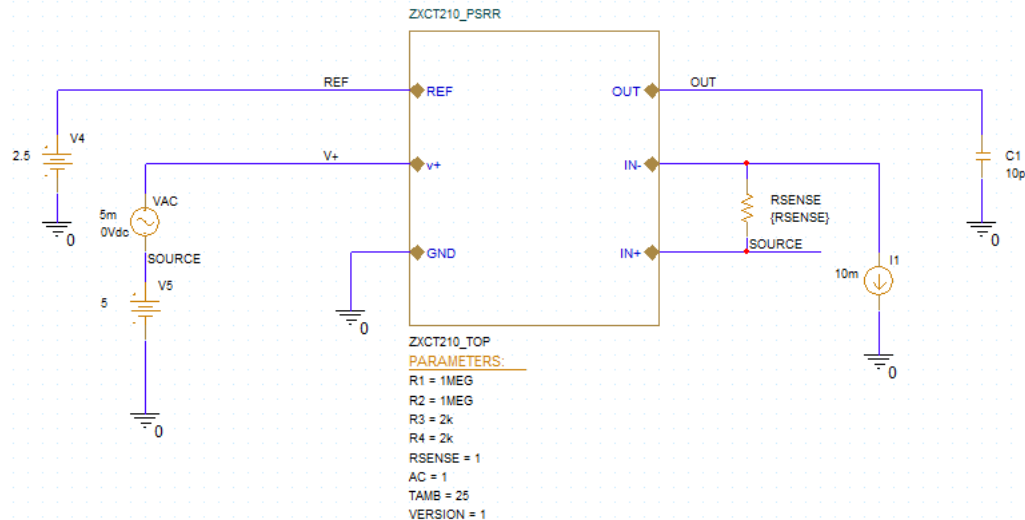
Therefore, the Gain Error =

$$\{(498 - 495.27)/498\} \times 100 = 0.5482\%$$

Part Number	Gain	R <sub>INT</sub> R3 and R4	Gain Error Factor Equations	Gain Error % *
				R <sub>s</sub> = 5Ω
ZXCT211	500	2kΩ	$\frac{10000}{13 * R_s + 10000}$	0.6458%

# PSRR Test Setup and Condition

Test Condition: VSUPPLY=5V, VREF=2.5V, FREQ=10Hz – 100kHz

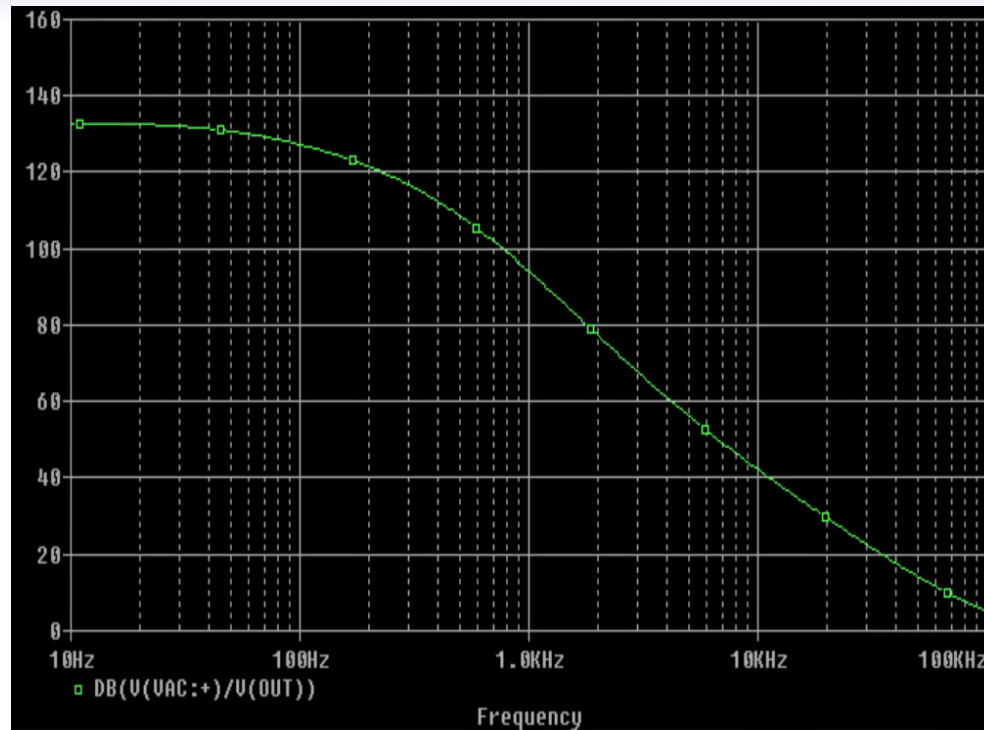


## Testbench Description

- The above testbench has been set-up to observe the PSRR characteristics of the device.
- Keep AC=1 : For AC analysis; Keep AC=0 : For transient analysis.
- Time taken for the simulation to complete which runs for the frequency range of 10Hz to 100KHz = Few seconds.

# PSpice Simulation Result / Datasheet

P-Spice Result



Datasheet

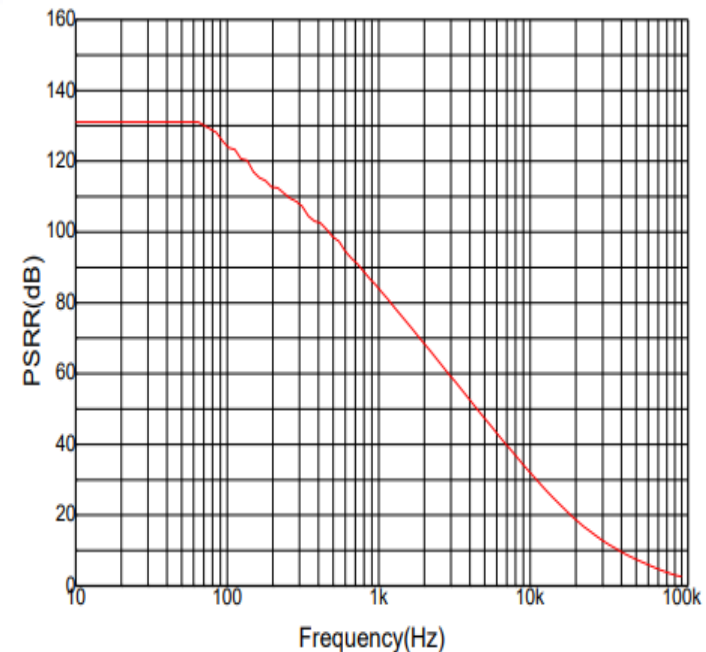
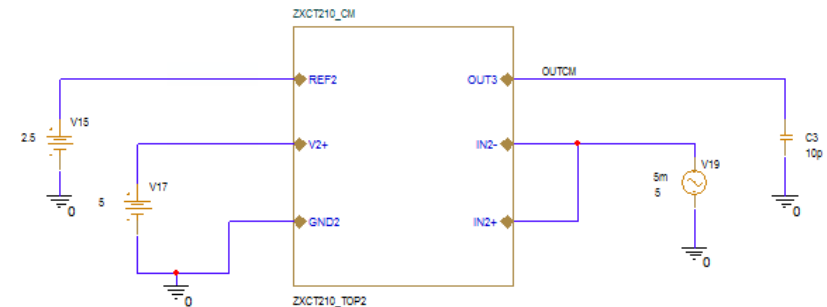
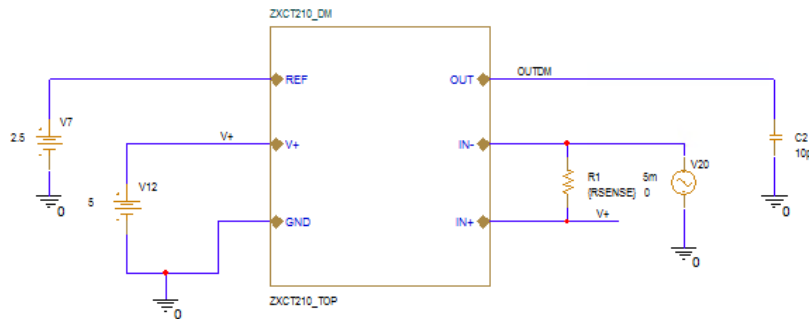


Figure 4. Power-Supply Rejection Ratio vs. Frequency

# CMRR Test Setup and Condition

Test Condition:  $V_{SUPPLY}=5V$ ,  $V_{REF}=2.5V$ ,  $FREQ=10Hz - 1MHz$



## PARAMETERS:

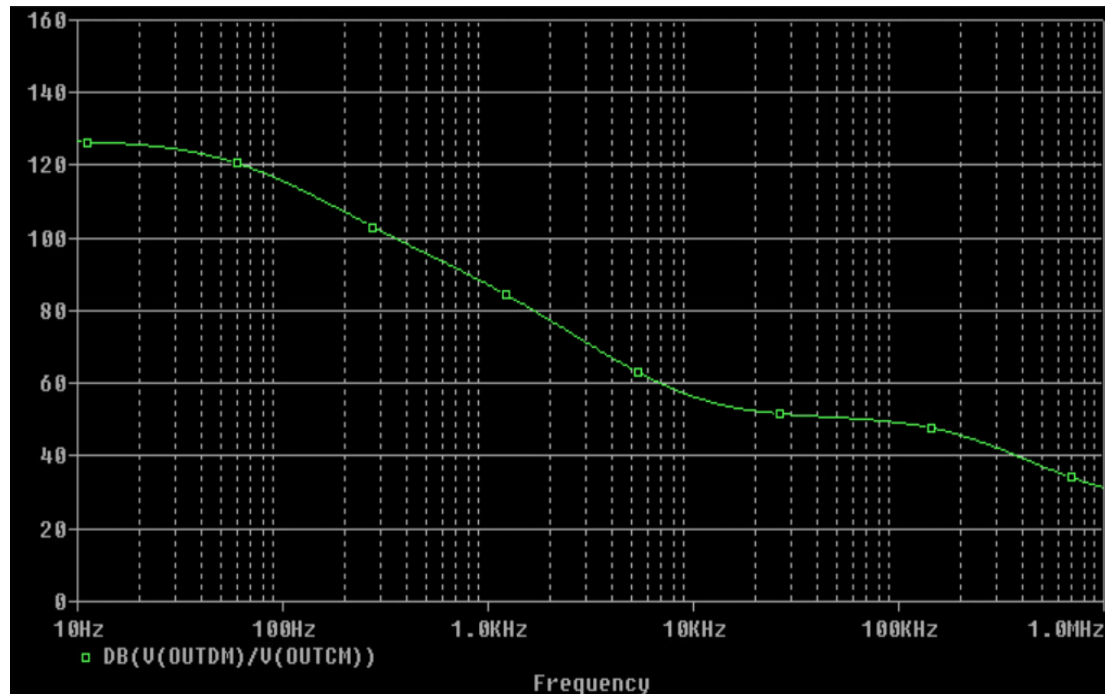
R1 = 1M $\Omega$   
R2 = 1M $\Omega$   
R3 = 2k  
R4 = 2k  
RSENSE = 1  
AC = 1  
TAMBS = 25  
VERSION = 1

## Testbench Description

- The above testbench has been set-up to observe the CMRR vs frequency response of the device.
- Keep AC=1 : For AC analysis; Keep AC=0 : For transient analysis.
- Time taken for the simulation to complete which runs for the frequency range of 10Hz to 1MHz = Few seconds.

# PSpice Simulation Result / Datasheet

## P-Spice Result



## Datasheet

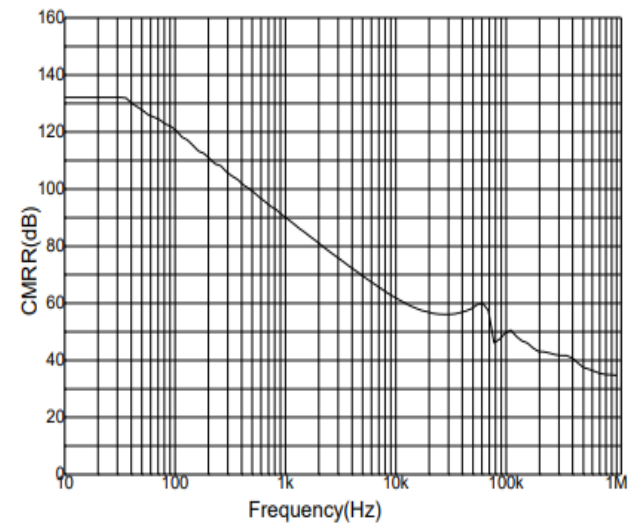


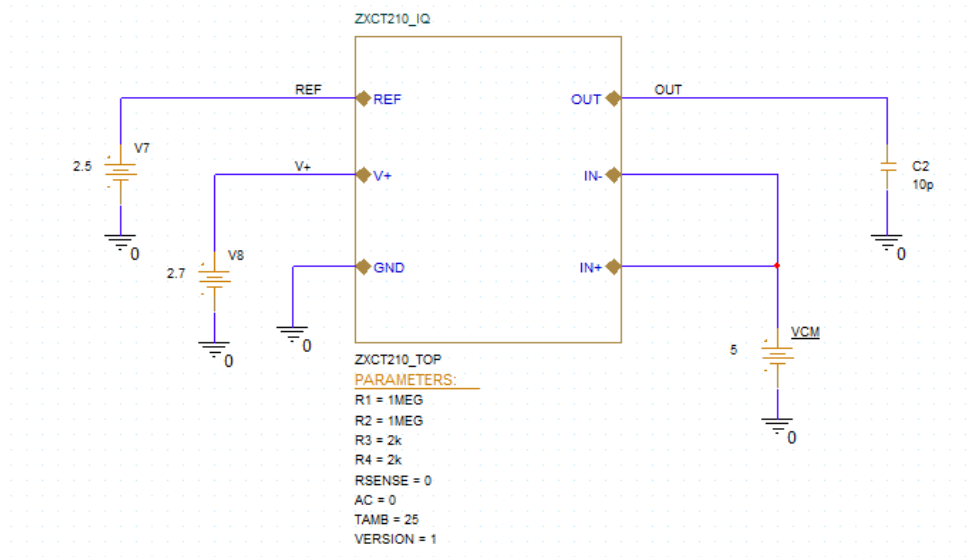
Figure 5. Common-Mode Rejection Ratio vs. Frequency

## Temperature variation



# Quiescent current vs Temperature

Test Condition: VSUPPLY=2.7V, VREF=2.5V, COMMON MODE VOLTAGE (V\_CM)=5V

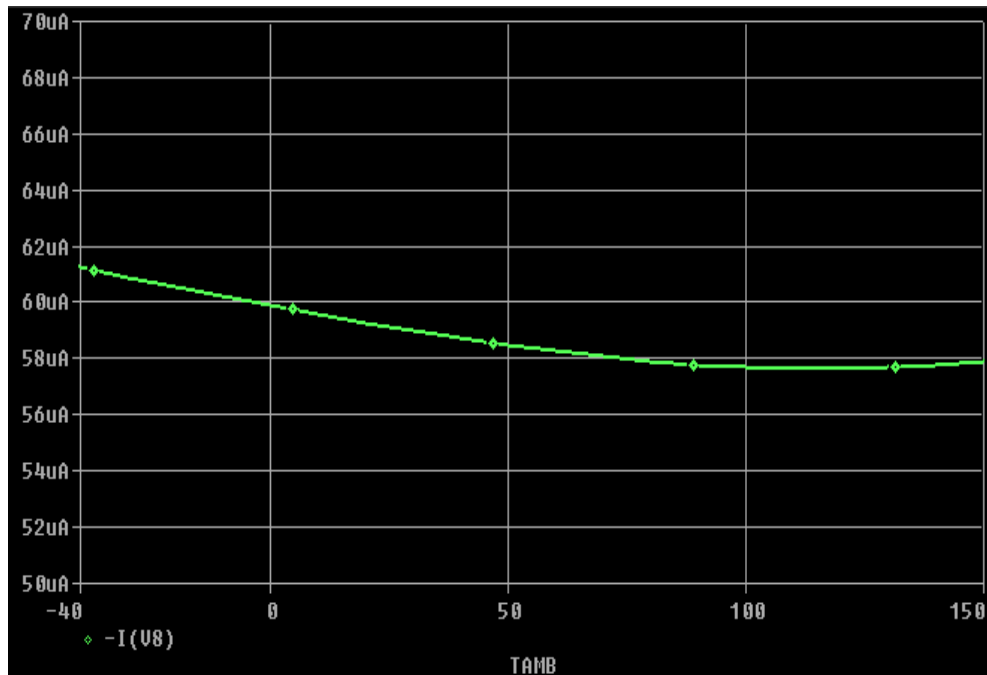


## Testbench Description

- The above testbench has been set-up to observe the variation of the Quiescent current with respect to temperature variation.
- Time taken for the simulation to complete = Few seconds.

# PSpice Simulation Result / Datasheet

P-Spice Result



Datasheet

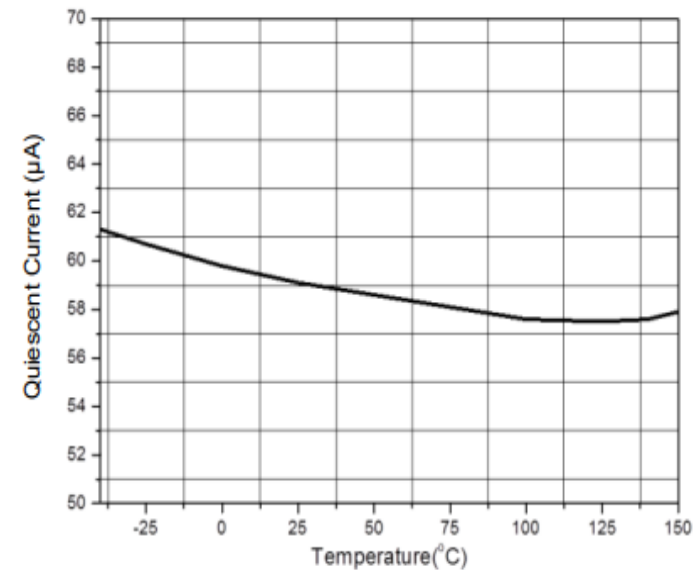
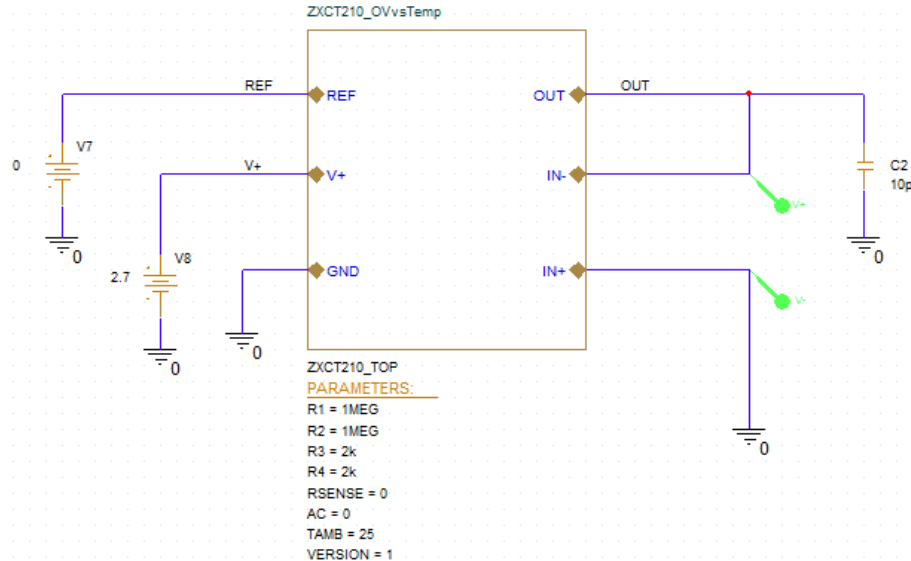


Figure 11. Quiescent Current vs. Temperature

# Offset voltage vs Temperature

Test Condition:  $V_{SUPPLY}=2.7V$ ,  $V_{REF}=0$ ,  $V_{(IN+)}=0$

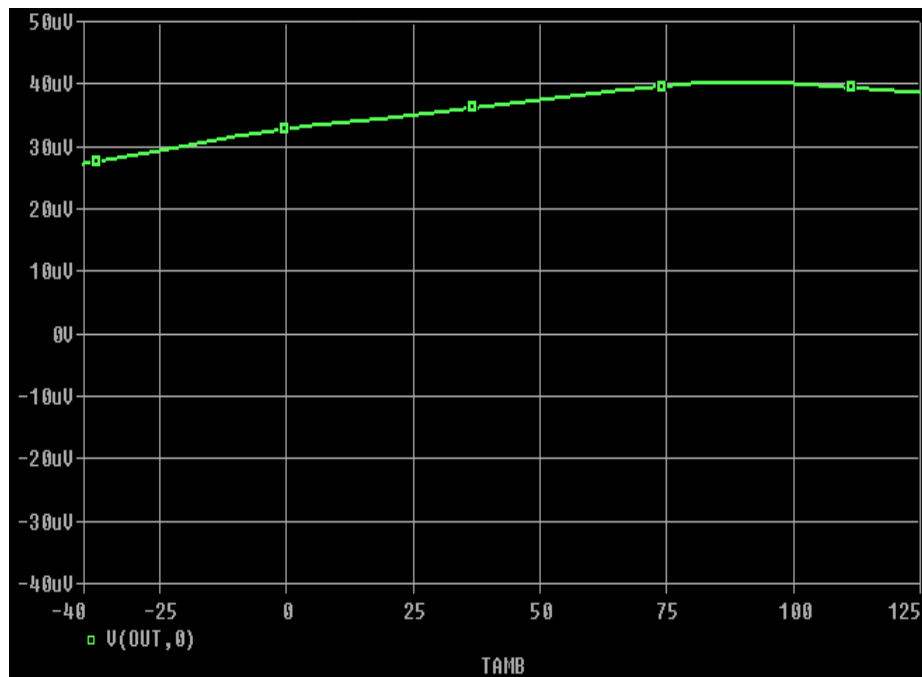


## Testbench Description

- The above testbench has been set-up to observe the variation of the Offset voltage with respect to temperature.
- Time taken for the simulation to complete = Few seconds.

# PSpice Simulation Result / Datasheet

P-Spice Result



Datasheet

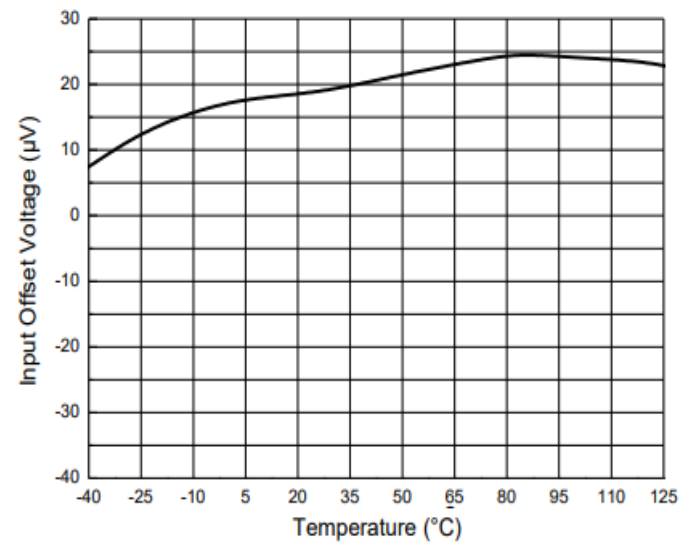
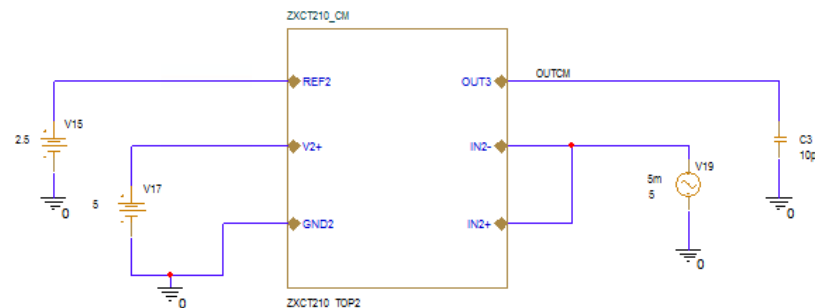
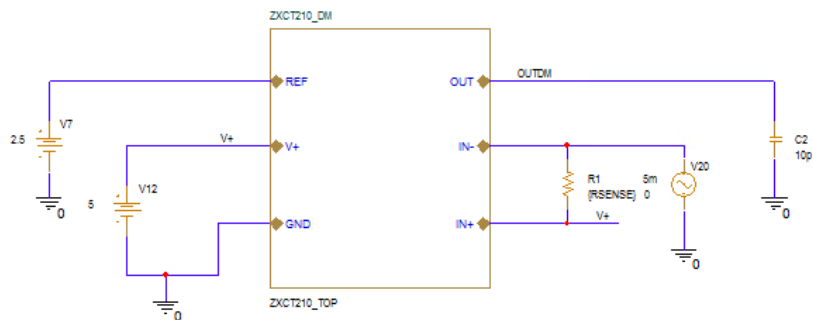


Figure 1. Offset Voltage vs. Temperature

# CMRR vs Temperature

Test Condition:  $V_{SUPPLY}=5V$ ,  $V_{REF}=2.5$ ,  $V(IN+)=12V$



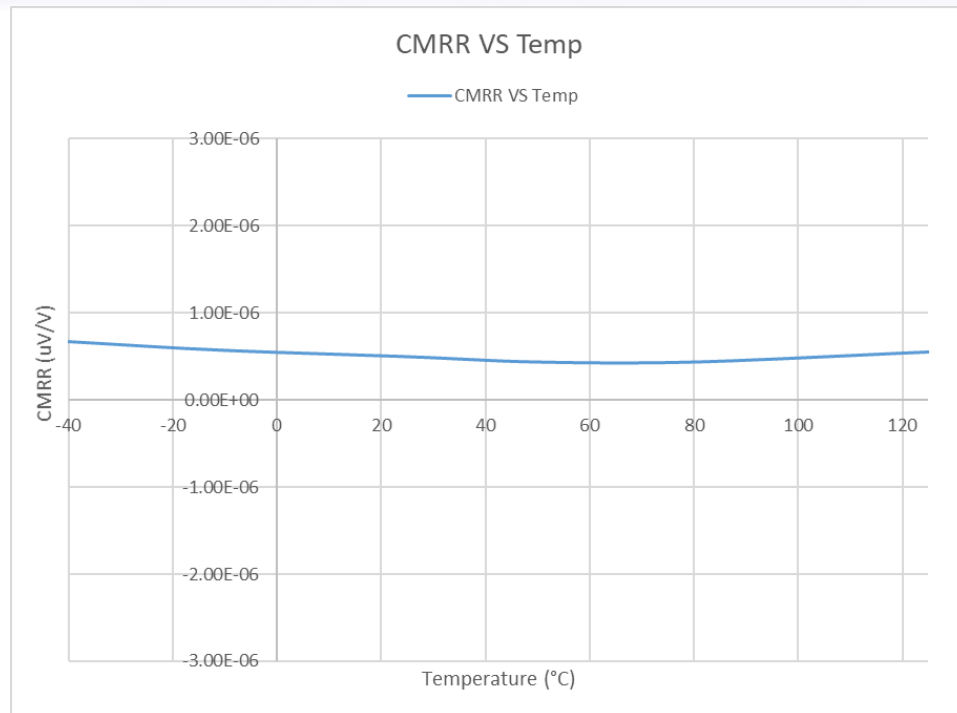
## PARAMETERS:

R1 = 1M Ω  
R2 = 1M Ω  
R3 = 2k  
R4 = 2k  
RSENSE = 1  
AC = 1  
TAMIB = 25  
VERSION = 1

## Testbench Description

- The above testbench has been set-up to observe the variation of CMRR with respect to temperature.
- Keep AC=1 : For AC analysis; Keep AC=0 : For transient analysis.
- Time taken for the simulation to complete = Few seconds.

# PSpice Simulation Result / Datasheet



## Datasheet

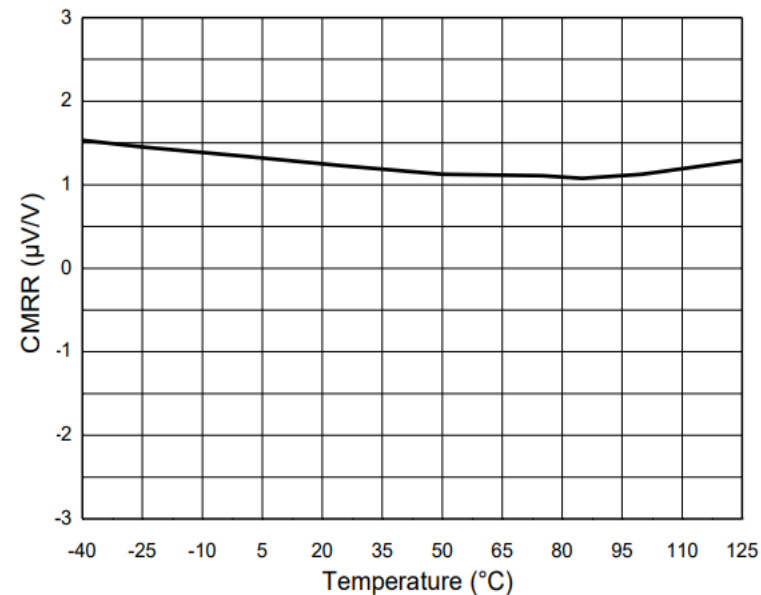
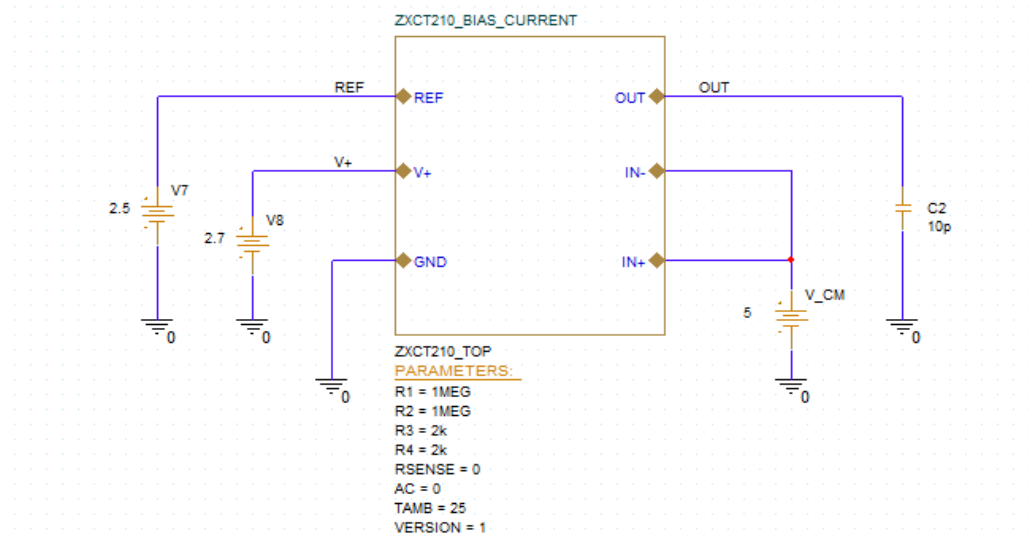


Figure 2. Common-Mode Rejection Ratio vs. Temperature

## DC Analysis

# Bias Current Test Setup 1 and Condition

Test Condition:  $V_{SUPPLY}=2.7V$ ,  $V_{REF}=2.5V$ , COMMON MODE VOLTAGE ( $V_{CM}$ )=5V



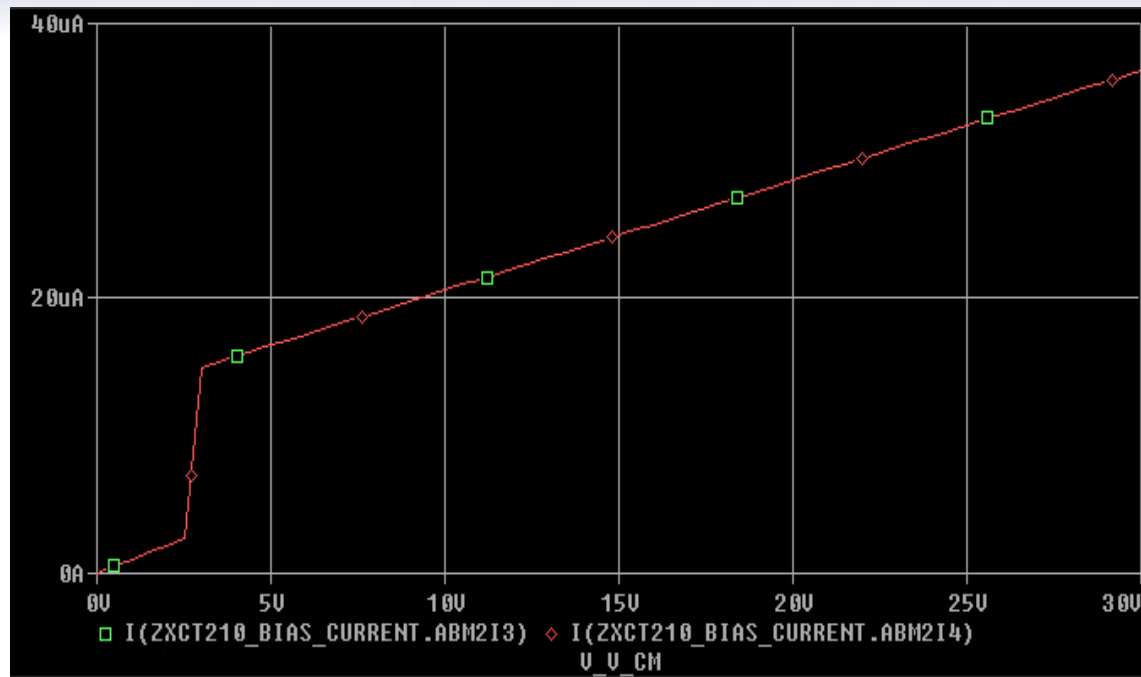
## Testbench Description

- The above testbench has been set-up to observe the variation of the input bias current with respect to the common mode voltage variation.
- Time taken for the simulation to complete = Few seconds.



# PSpice Simulation Result / Datasheet

P-Spice Result



Datasheet

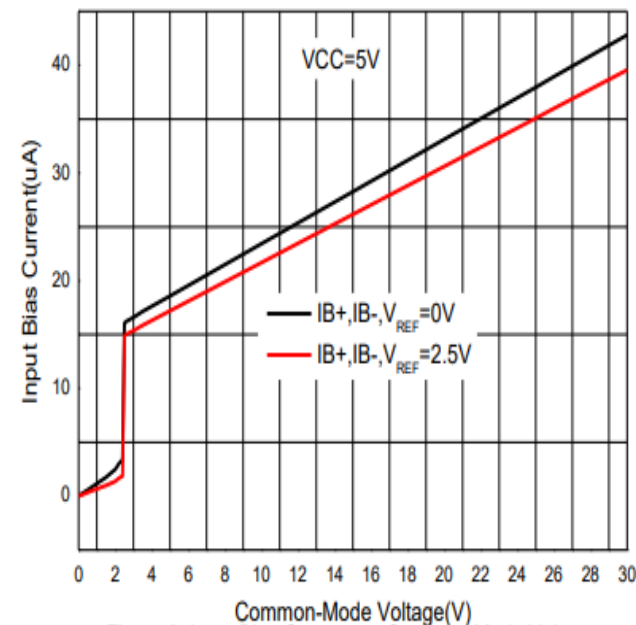
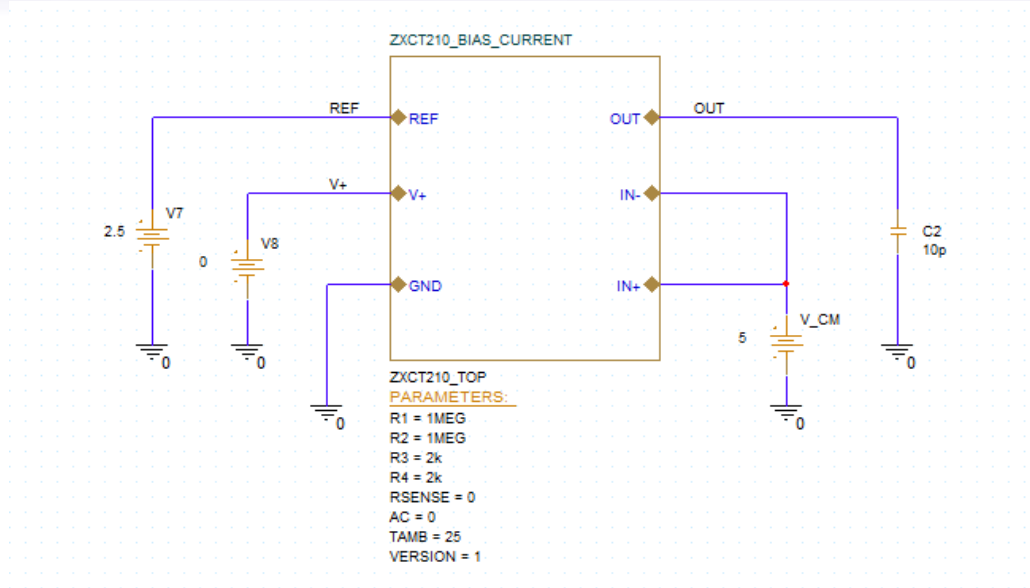


Figure 8. Input Bias Current vs. Common-Mode Voltage

Internal nodes are plotted to avoid the effect of loop resistors.  
ABM213: Non inverting; ABM214: Inverting

# Bias Current Test Setup 2 and Condition

Test Condition: VSUPPLY=0V, VREF=2.5V, COMMON MODE VOLTAGE (V\_CM)=5

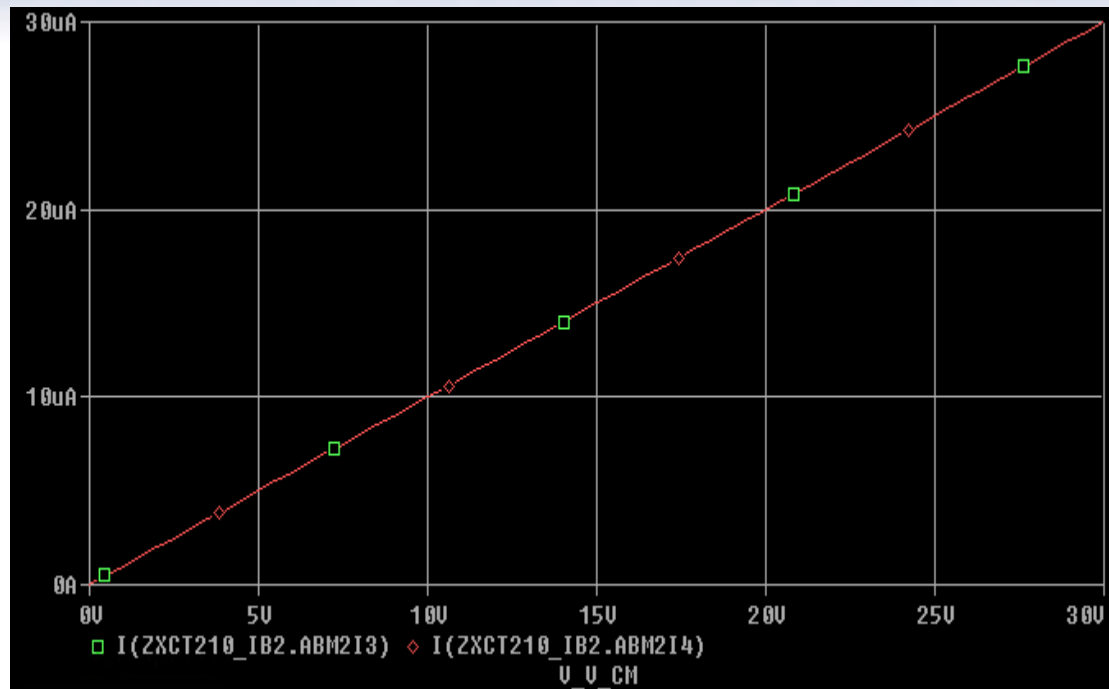


## Testbench Description

- The above testbench has been set-up to observe the variation of the input bias current with respect to the common mode voltage variation.
- Time taken for the simulation to complete = Few seconds.

# PSpice Simulation Result / Datasheet

P-Spice Result



Datasheet

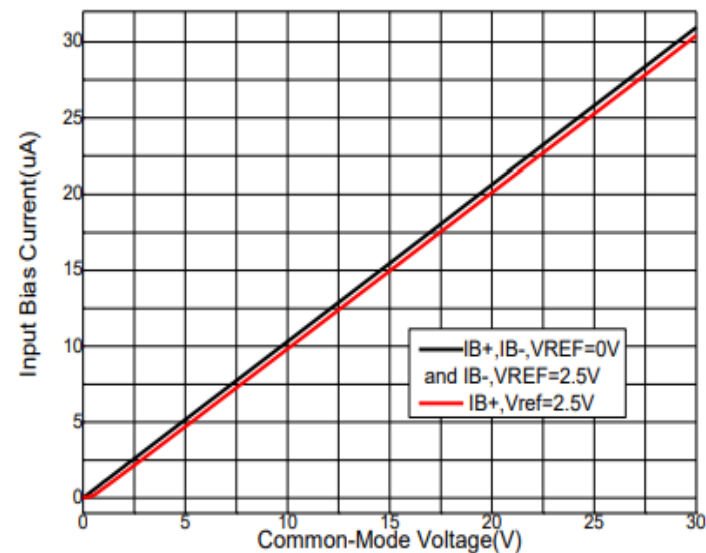
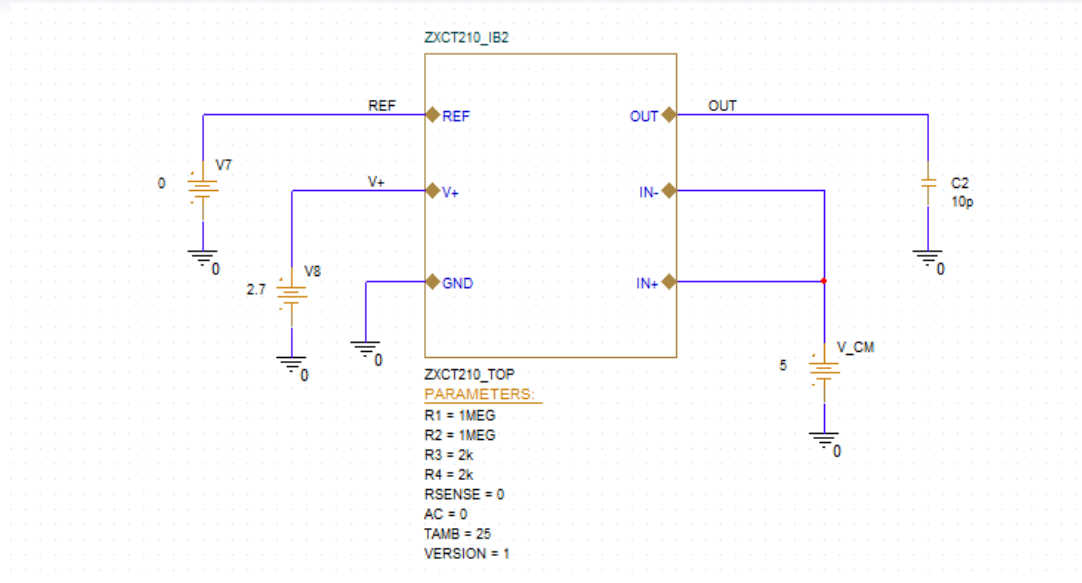


Figure 9. Input Bias Current vs. Common-Mode Voltage With Supply Voltage=0V(Shutdown)

Internal nodes are plotted to avoid the effect of loop resistors.  
ABM213: Non inverting; ABM214: Inverting

# Bias Current Test Setup 3 and Condition

Test Condition:  $V_{SUPPLY}=2.7V$ ,  $V_{REF}=0V$ , COMMON MODE VOLTAGE ( $V_{CM}$ )= $5V$

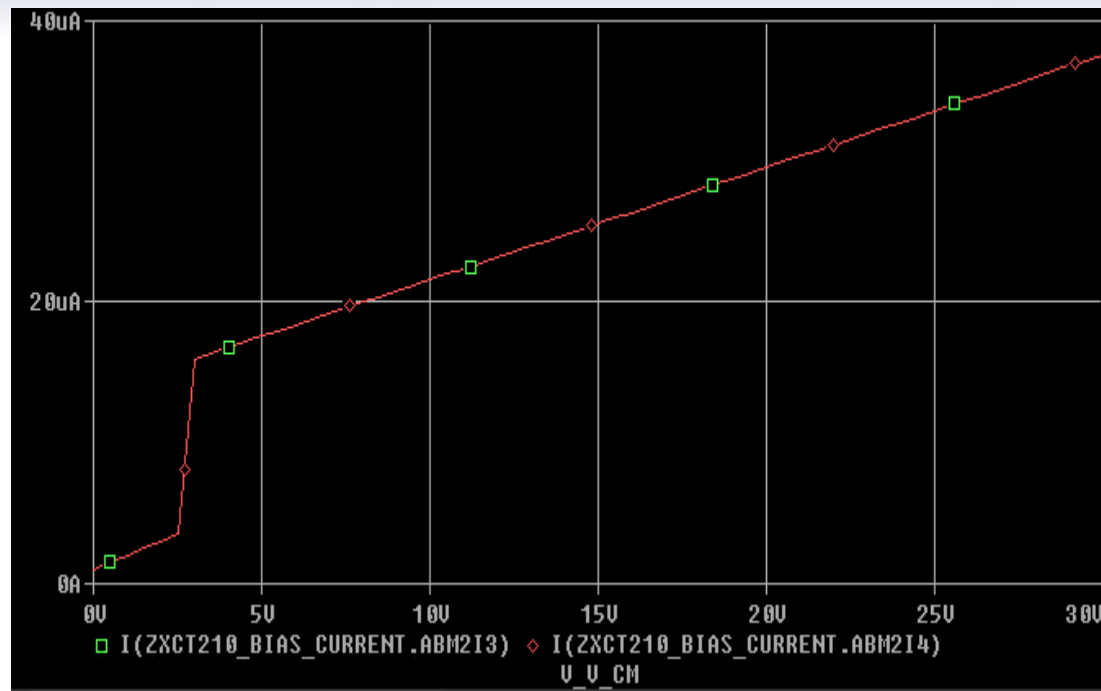


## Testbench Description

- The above testbench has been set-up to observe the variation of the input bias current with respect to the common mode voltage variation.
- Time taken for the simulation to complete = Few seconds.

# PSpice Simulation Result / Datasheet

P-Spice Result



Datasheet

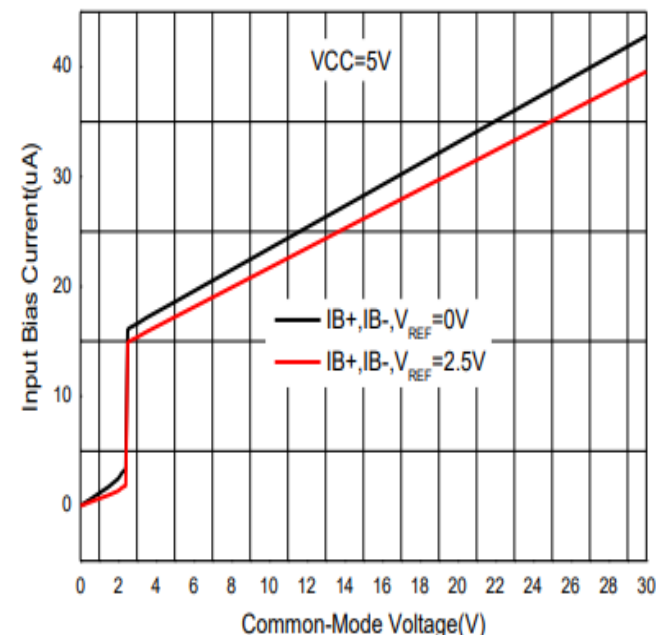
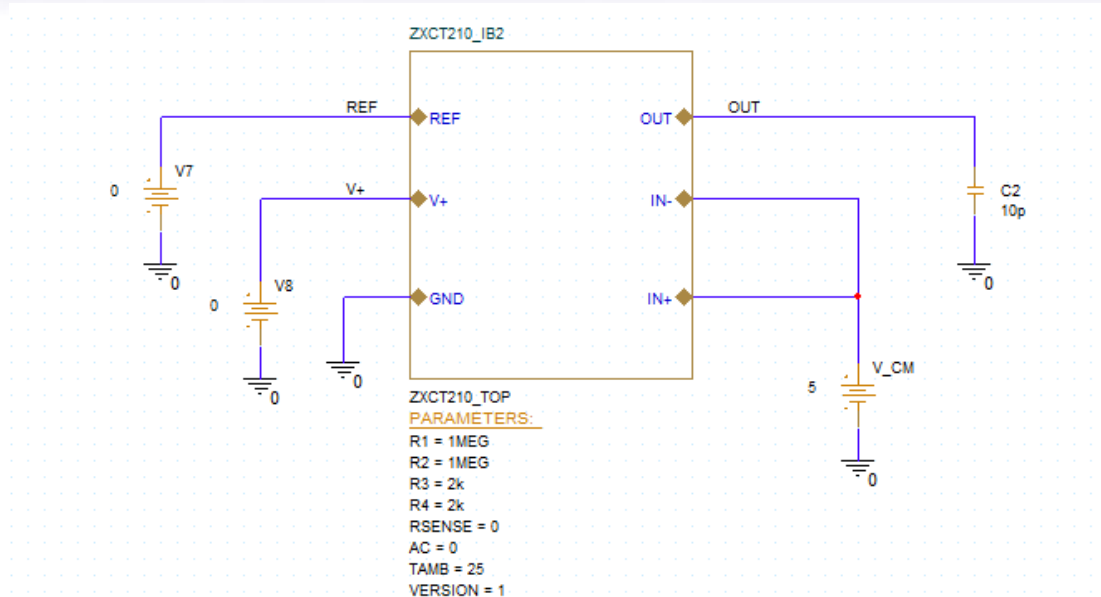


Figure 8. Input Bias Current vs. Common-Mode Voltage

Internal nodes are plotted to avoid the effect of loop resistors.  
ABM213: Non inverting; ABM214: Inverting

# Bias Current Test Setup 4 and Condition

Test Condition: VSUPPLY=0V, VREF=0V, COMMON MODE VOLTAGE ( $V_{CM}$ )=5V

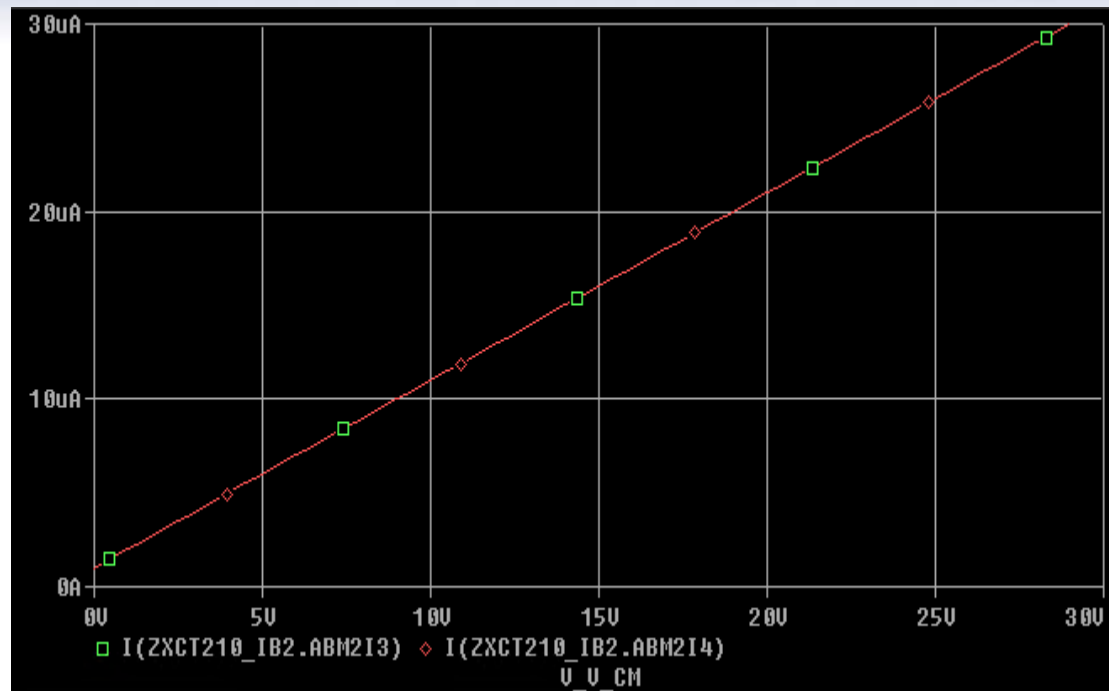


## Testbench Description

- The above testbench has been set-up to observe the variation of the input bias current with respect to the common mode voltage variation.
- Time taken for the simulation to complete = Few seconds.

# PSpice Simulation Result / Datasheet

P-Spice Result



Datasheet

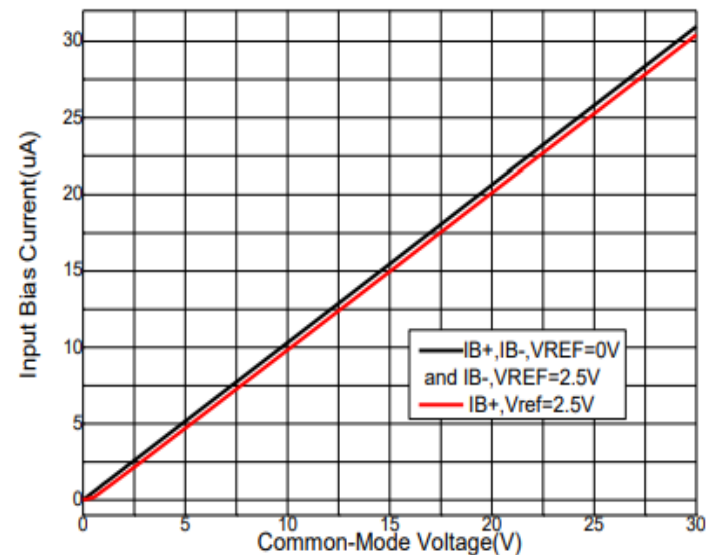


Figure 9. Input Bias Current vs. Common-Mode Voltage With Supply Voltage=0V(Shutdown)

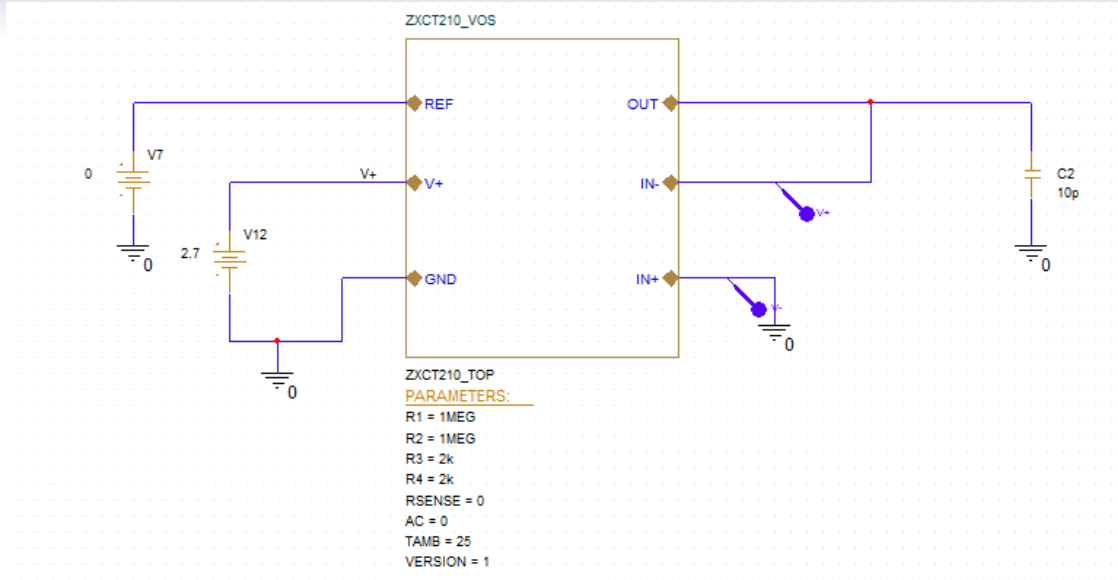
Internal nodes are plotted to avoid the effect of loop resistors.  
ABM213: Non inverting; ABM214: Inverting

# Transient Analysis



# Offset voltage test setup

Test Condition: VSUPPLY=2.7V, VREF=0V

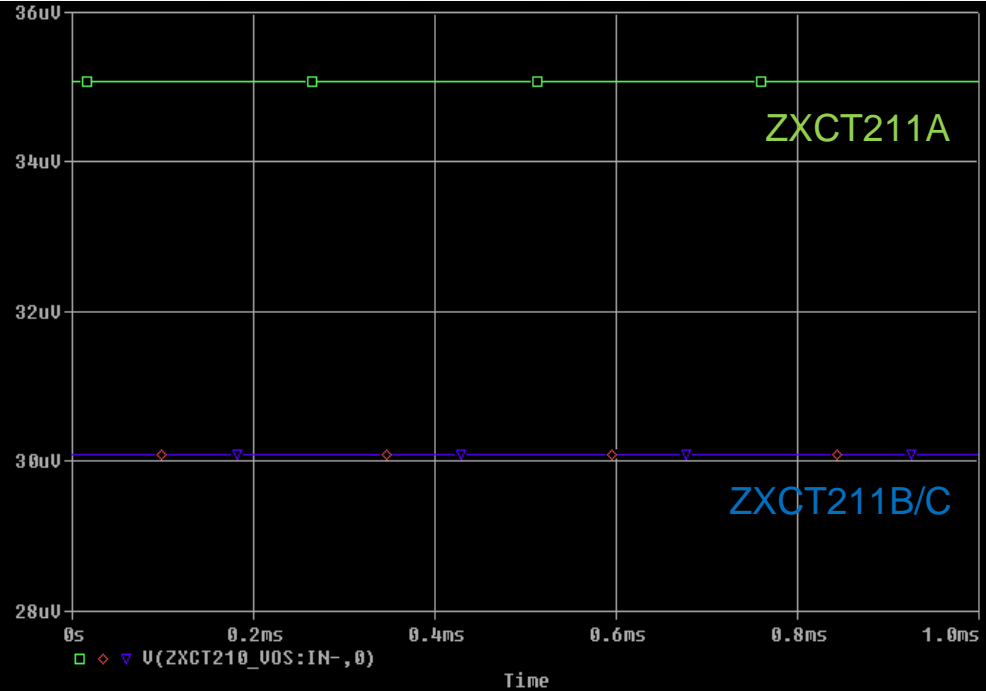


## Testbench Description

- The above testbench has been set-up to observe the offset voltage of ZXCT211 A, B & C version. Parameter “VERSION” is used to control the A(VERSION=1), B(VERSION=2), C(VERSION=3) versions.
- Keep AC=1 : For AC analysis; Keep AC=0 : For transient analysis.
- Time taken for the simulation to complete = Few seconds.

# PSpice Simulation Result / Datasheet

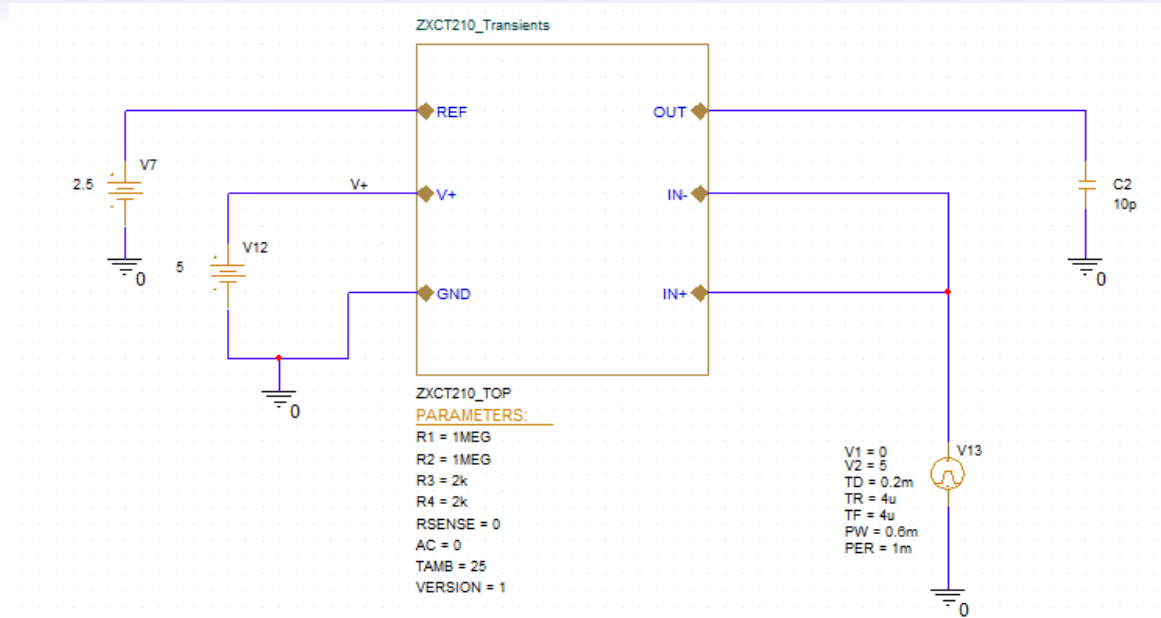
P-Spice Result



Version	Datasheet Value	PSPICE Value
ZXCT211A	35uV	35uV
ZXCT211B	30uV	30.1uV
ZXCT211C	30uV	30.1uV

# Common Mode Voltage Vs Transient Response Test Setup and Condition

Test Condition: VSUPPLY=2.7V, VREF=200mV, COMMON MODE VOLTAGE (CM)=0V-5V-0V

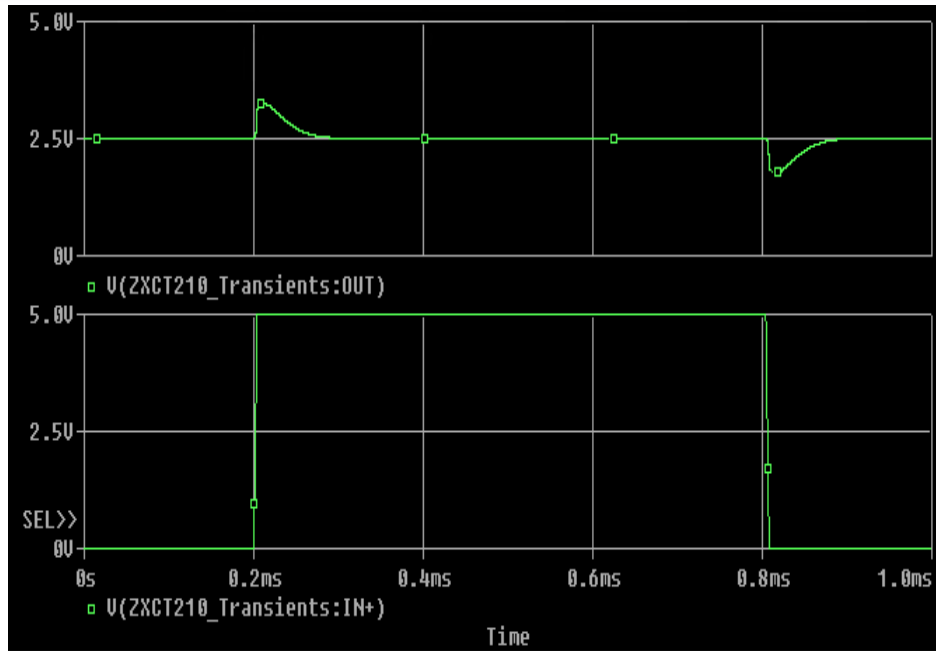


## Testbench Description

- The above testbench has been set-up to observe the transient response in case of common mode voltage.
- Keep AC=1 : For AC analysis; Keep AC=0 : For transient analysis.
- Time taken for the simulation to complete = Few seconds.

# PSpice Simulation Result / Datasheet

P-Spice Result



Datasheet

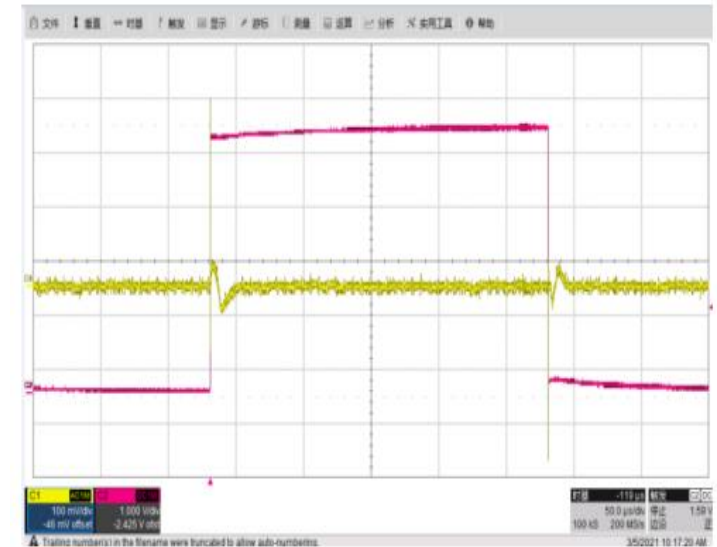
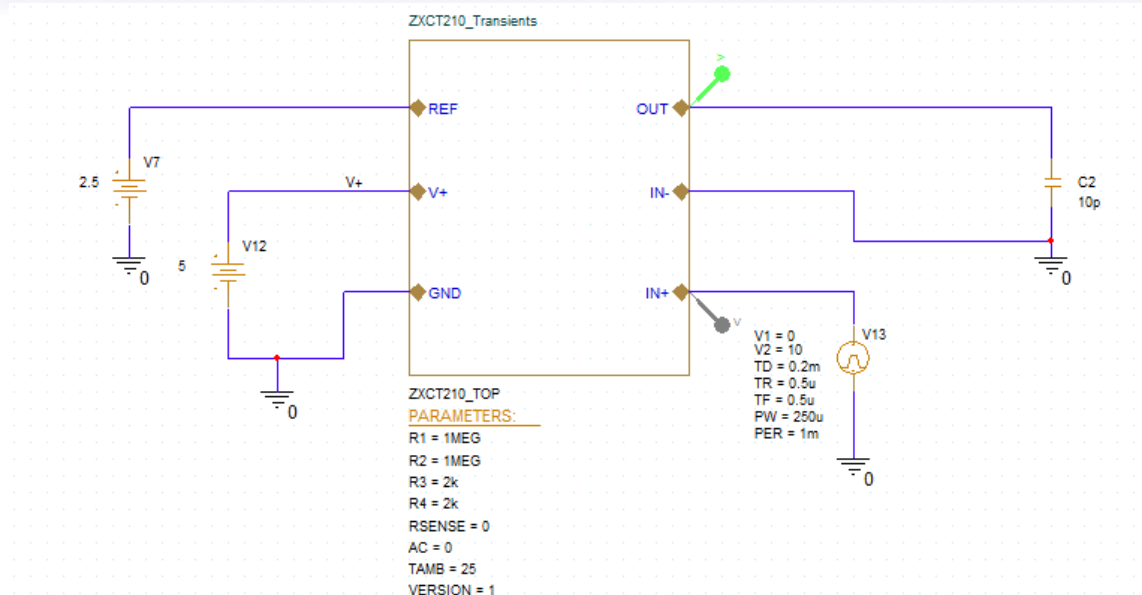


Figure 13 Common-Mode Voltage vs Transient Response

# Non Inverting Differential Input Overload Test Setup and Condition

Test Condition: VSUPPLY=5V, VREF=2.5V, Input Voltage=0V-10V-0V

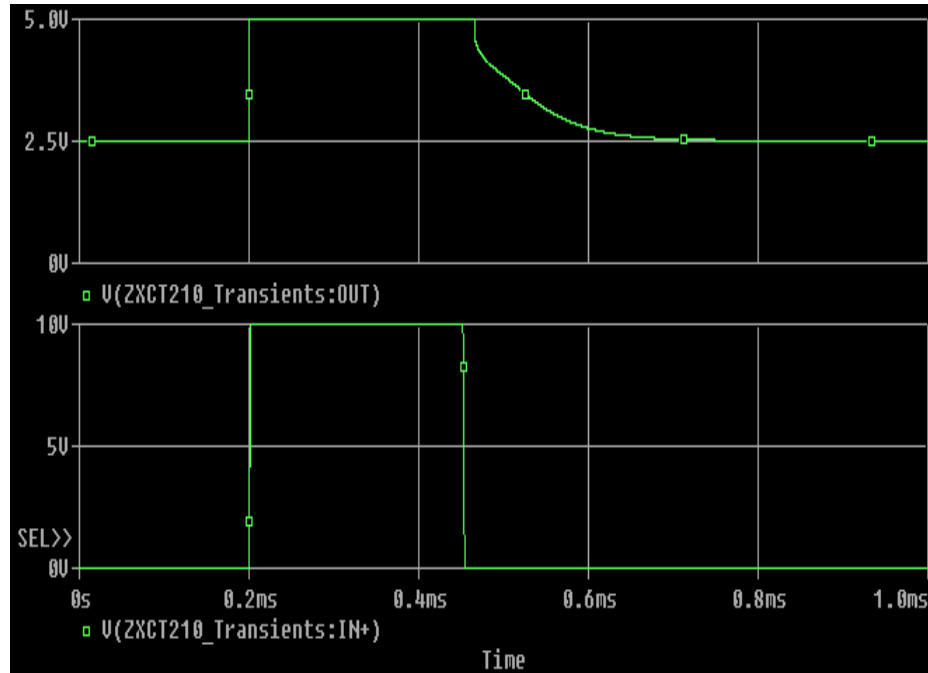


## Testbench Description

- The above testbench has been set-up to observe the response in non inverting input overload.
- Keep AC=1 : For AC analysis; Keep AC=0 : For transient analysis.
- Time taken for the simulation to complete = Few seconds.

# PSpice Simulation Result / Datasheet

## P-Spice Result



## Datasheet

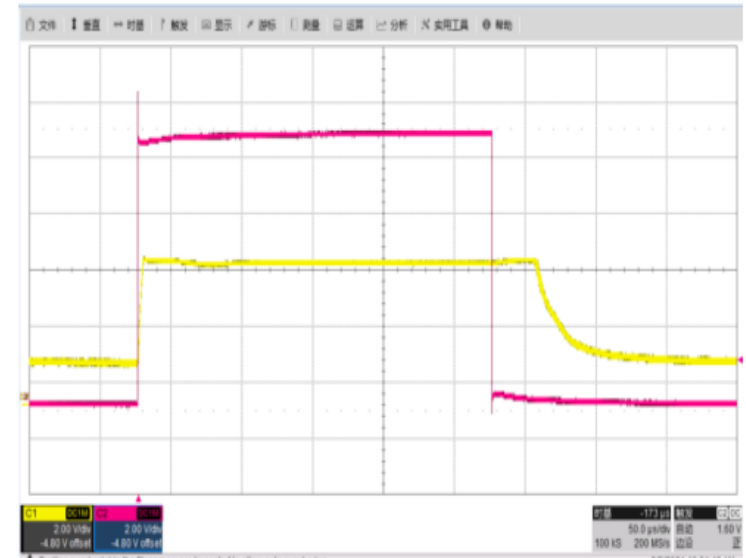
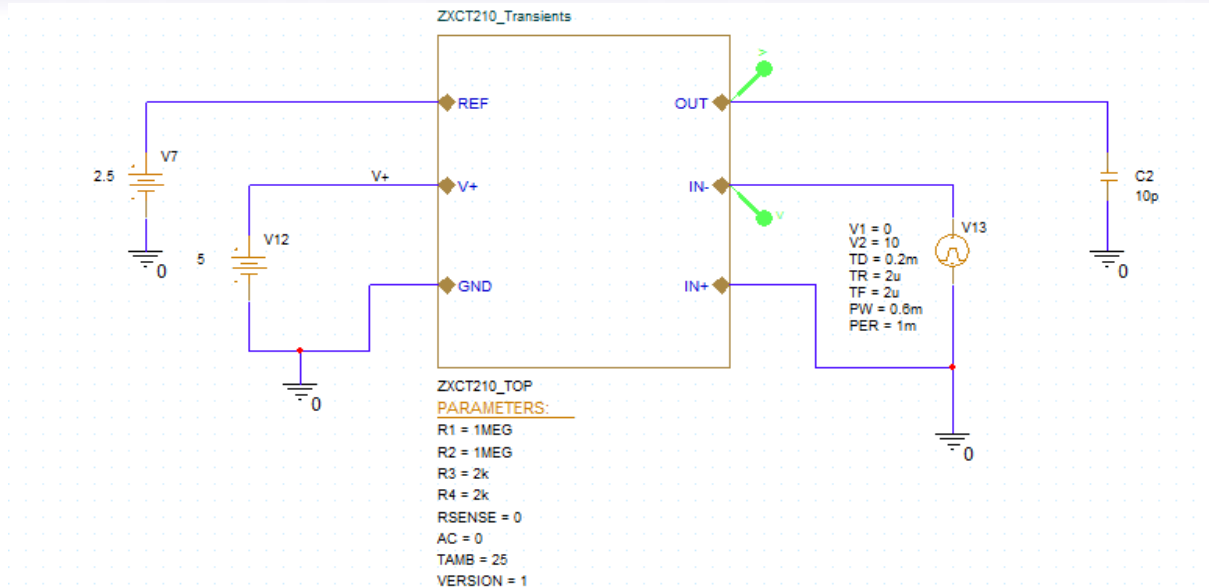


Figure14 Noninverting Differential Input Overload

# Inverting Differential Input Overload Test Setup and Condition

Test Condition: VSUPPLY = 5V, VREF = 2.5V, Input Voltage = 0V-10V-0V

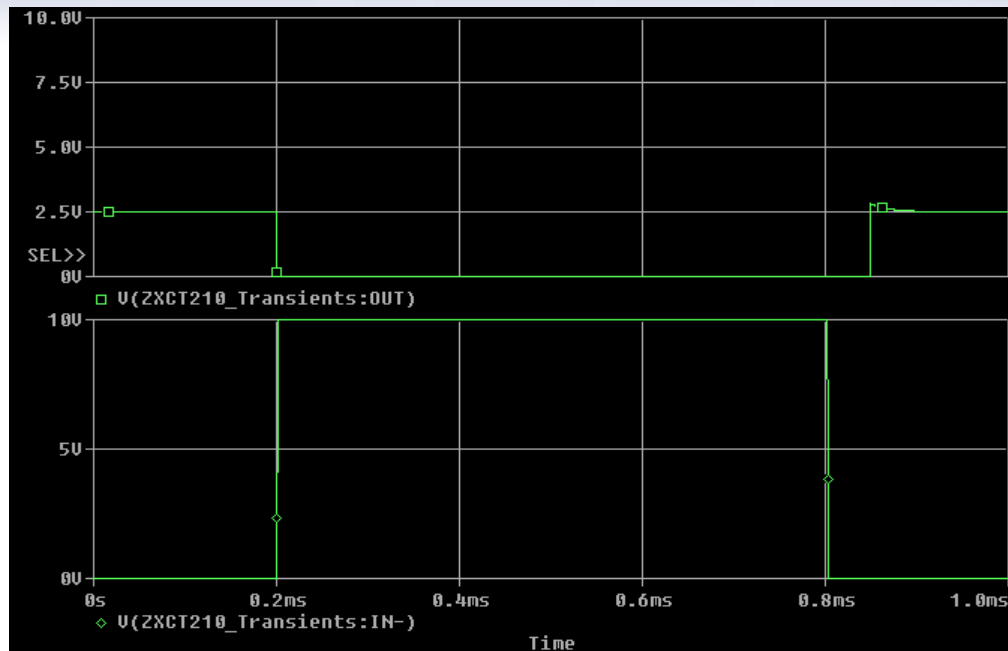


## Testbench Description

- The above testbench has been set-up to observe the response in inverting input overload.
- Keep AC=1 : For AC analysis; Keep AC=0 : For transient analysis.
- Time taken for the simulation to complete = Few seconds.

# PSpice Simulation Result / Datasheet

## P-Spice Result



## Datasheet

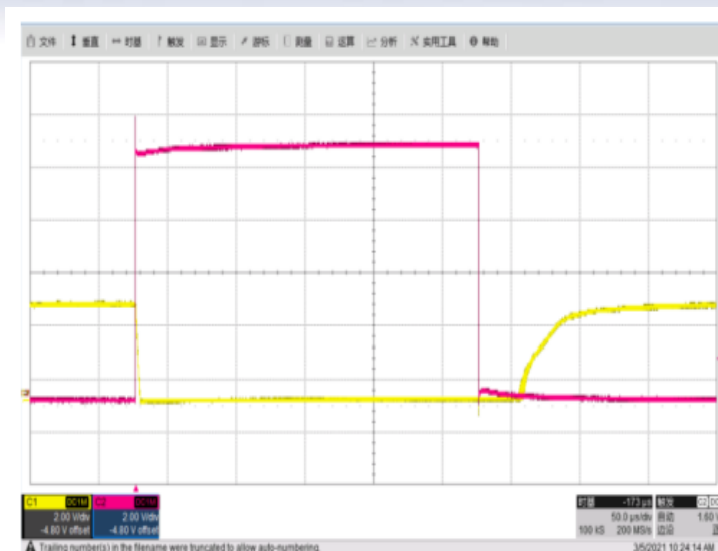


Figure 15 Inverting Differential. Input Overload



THANK YOU