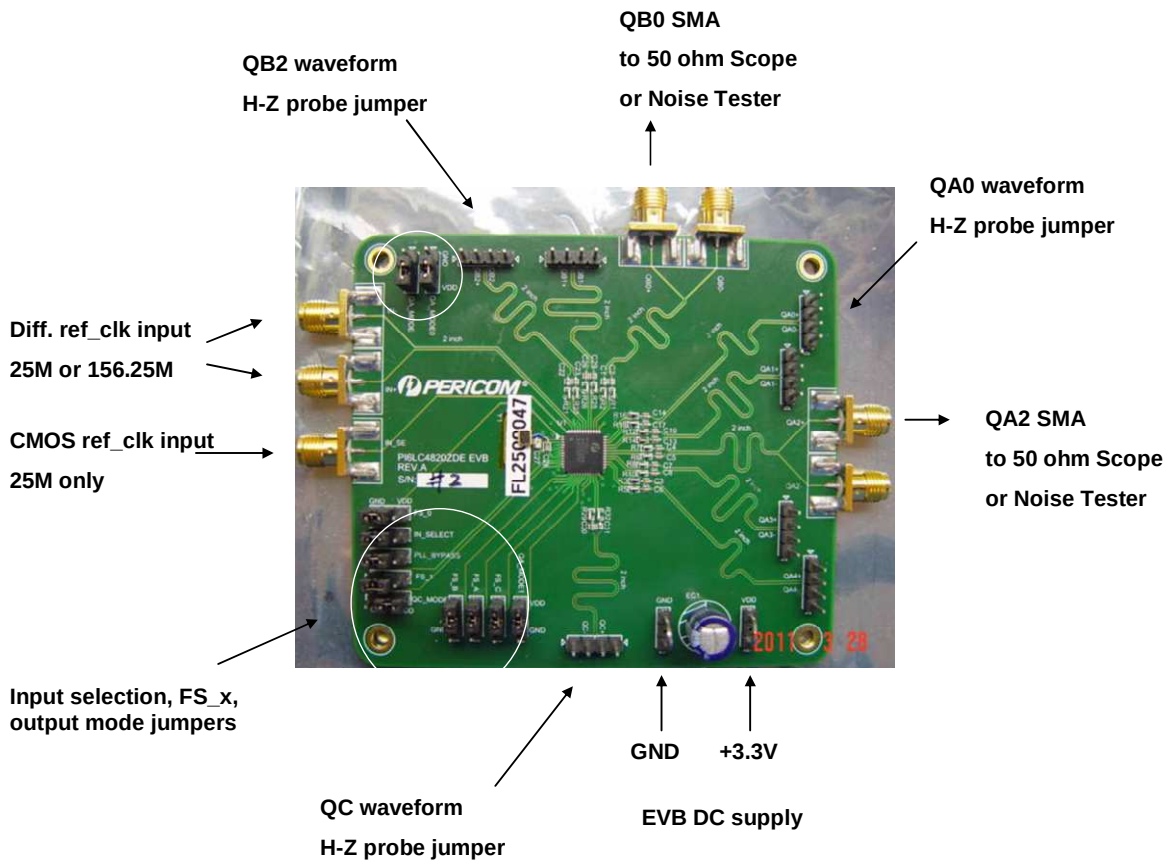
PI6LC4820 EVB Use Manual

Pericom Application Engineering

1. Introduction

PI6LC4820 is a LC family high performance jitter clock generator for advance Gigabit Ethernet system design. It has independent 3 bank outputs that can be set LVPECL or LVDS in 3 output frequencies: 125MHz, 156.25MHz, and 312.5MHz. This doc. is to provide EVB use guide and test reference data.

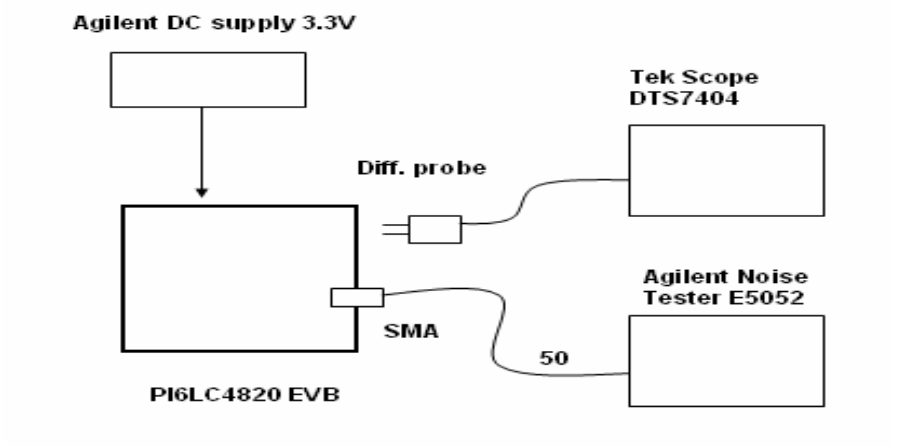
2. PI6C4820 EVB Test Setup Requirement



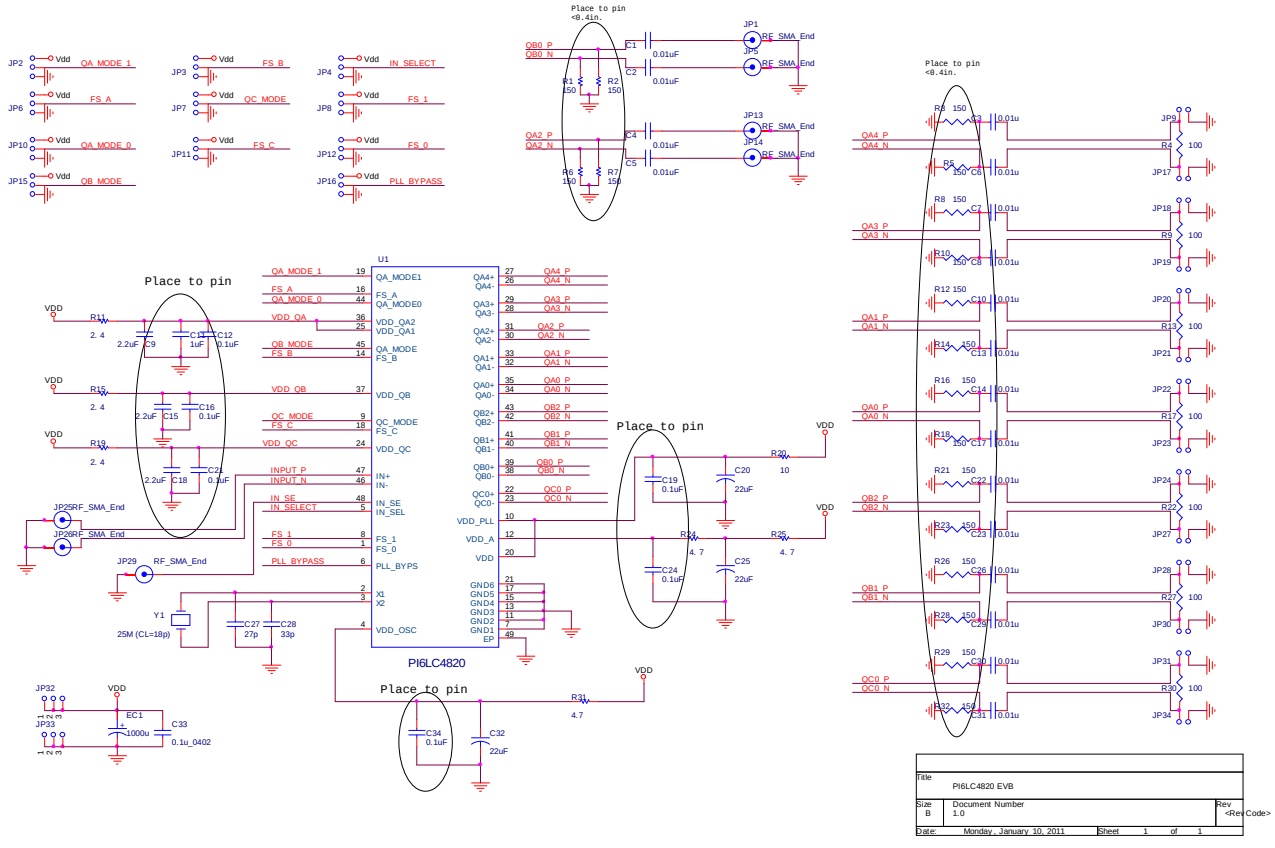
Test equipment:

1) Tek 20G/S real time scope TDS7404;
2) Agilent phase noise tester E5052A;
3) Agilent DC Power supply

3. PI6C4820 EVB Test Connection Diagram



4. PI6LC4820 EVB Reference Schematic

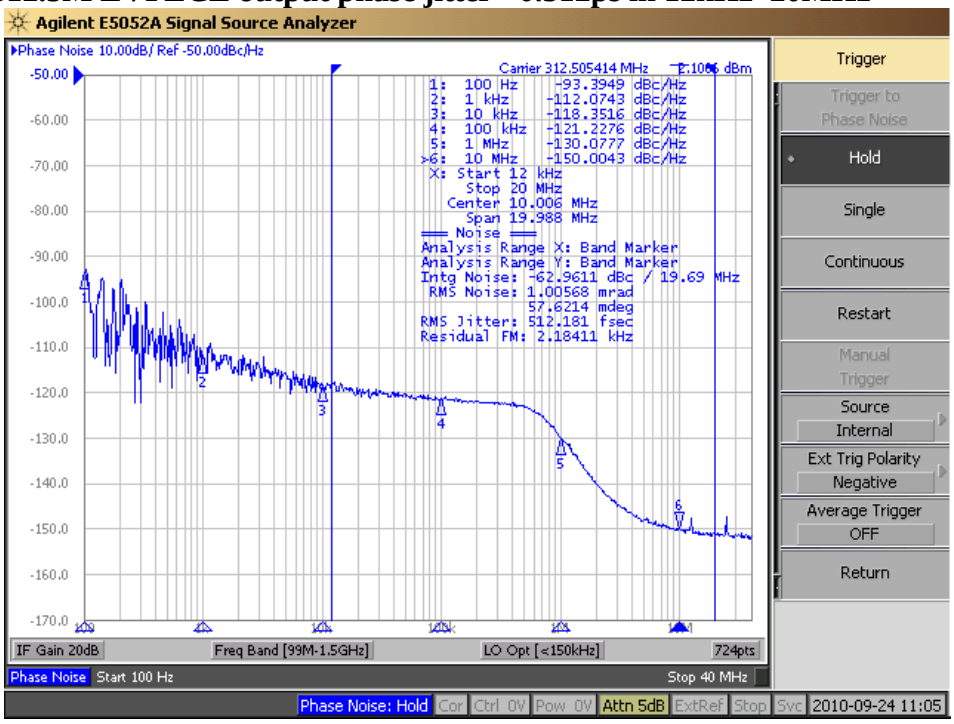


Note:

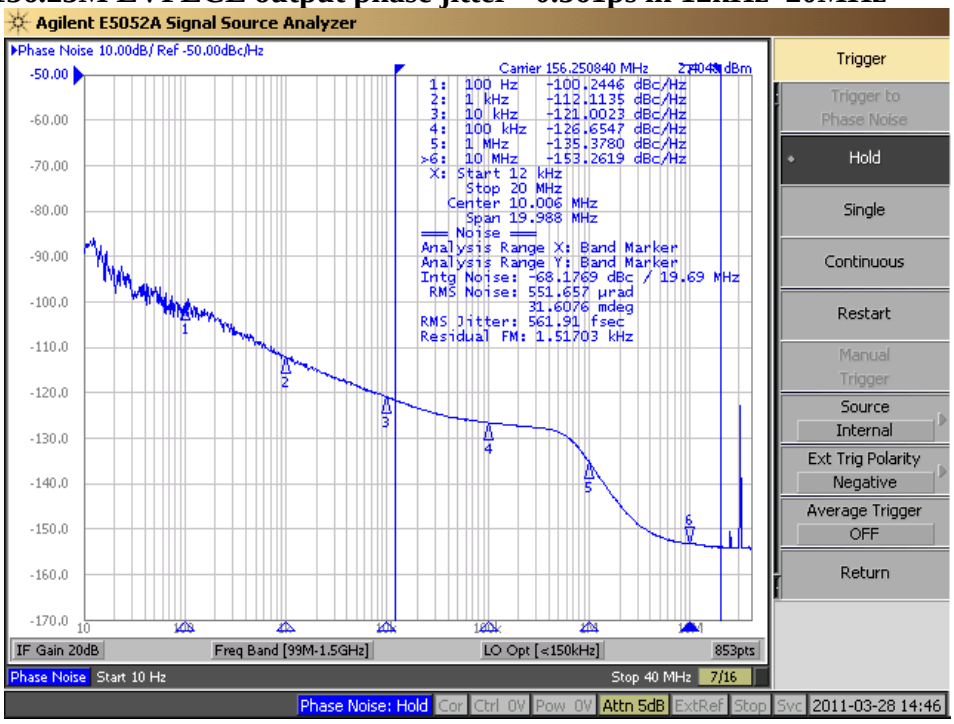
1) It is suggested to use the schematic's decoupling RC value to get best board noise filtering; .
2) Typical LVPECL is using 150 pull down in AC or DC coupling drive according to ASIC ref_clk I/O spec.
3) The crystal external load C1=C2=22pF is for CL=18pF crystal;
4) Please refer to the datasheet other logic set for the output mode and output frequencies in each bank;
5) Please refer to "PI6LC4820 Application and PCB guide" doc. for more detail circuit design;

5. PI6LC4820 EVB Test Phase Noise Plots

1) 312.5M LVPECL output phase jitter= 0.512ps in 12kHz~20MHz



2) 156.25M LVPECL output phase jitter= 0.561ps in 12kHz~20MHz



3) 125M LVPECL output phase jitter= 0.503ps in 12kHz~20MHz