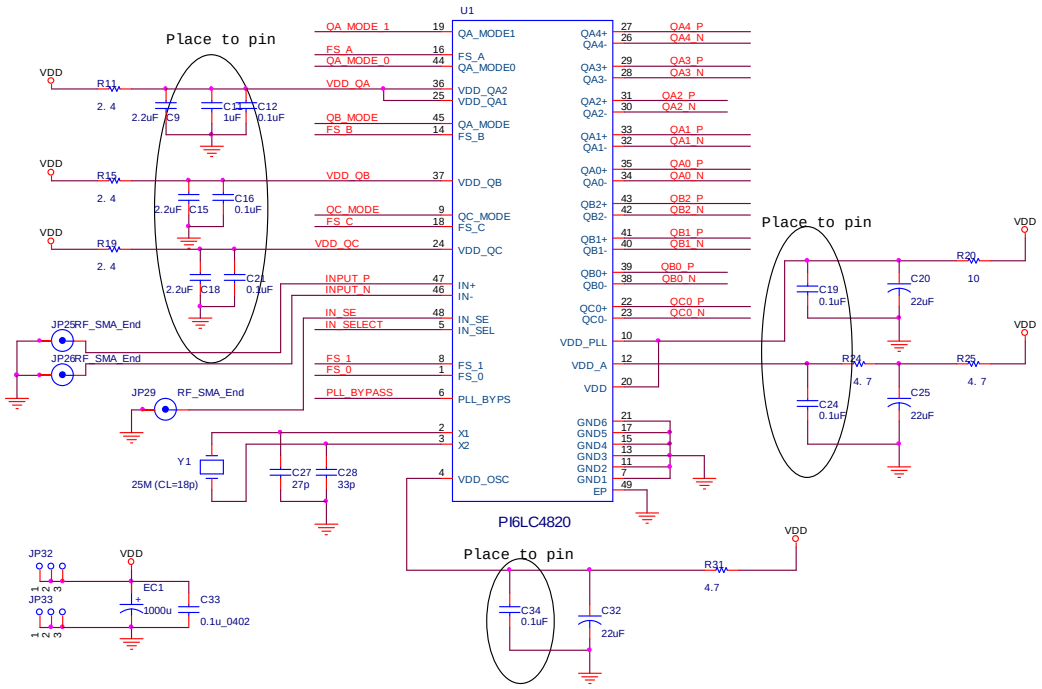
PI6LC4820 Decoupling and PCB Layout Guide

Pericom Application Engineering

1. Introduction

PI6LC4820 is a LC high performance jitter clock generator for advance Gigabit Ethernet system design. It has independent 3 bank outputs that can be set LVPECL or LVDS in 3 output frequencies: 125MHz, 156.25MHz, and 312.5MHz. This doc. is to provide general schematic and PCB layout guide to ensure customer proper application to get the best and constant board design performance.

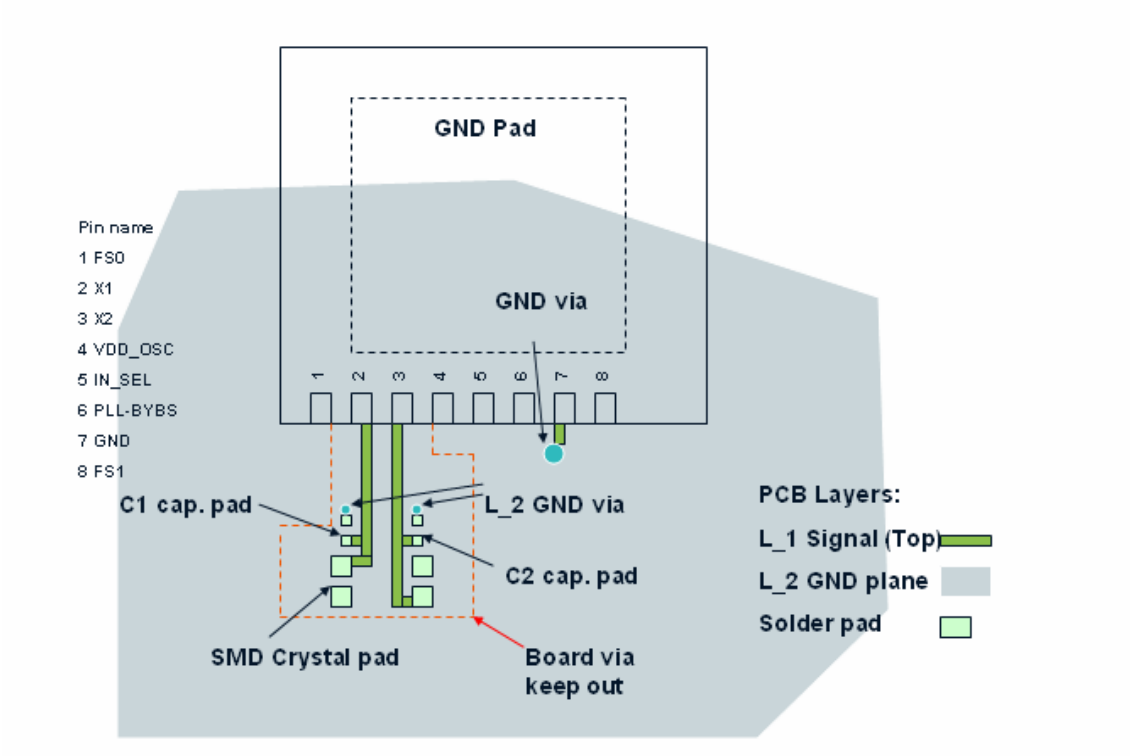
2. Power Decoupling Schematic



Note:

1) It is suggested to use the schematic's decoupling RC value to get best board noise filtering; .
2) Typical LVPECL is using 150 pull down in AC or DC coupling drive according to ASIC ref_clk I/O spec.
3) The crystal circuit C1/C2 load valve is for CL=18pF crystal, they can be adjusted for other CL crystal;
4) Please refer to the datasheet for other static I/O logic set for the request work mode and output frequencies;

3. Crystal Circuit Layout Guide



Note:

1) Xin pin is the most sensitive as crystal amplifier input;
2) Xin and Xout pins connected to crystal trace loop should be very narrow without any board via in the loop and keep out area;
3) Place crystal closer to the IC as possible and route crystal C1/C2 load caps. on the top layer without via to the crystal;
4) Keep crystal load cap. C1/C2 GND sides as close as possible, with min. board noise coupling into the caps.;

4. VDD and GND Pins Layout

1) Small value decoupling caps. (0.1uF, 1uF, and 2.2uF) should be placed close each VDD pin/via;
2) It is suggested each GND pin has its own via to the common GND plane;
3) Thermal pad must be connected to the GND plane for better thermal distribution and signal conducting with reasonable via count (>6);

5. LVPECL Differential Output Layout

1) 150 ohm pull-down would be put close to clock output side with symmetrical position in one pair;
2) It is better not to share 150 ohm pull-down GND via between each pairs;

6. Differential Input Layout

1) This device differential input (pin 47, 48) can accept 25MHz, 125MHz, and 156.25MHz frequencies in most common differential signals (LVPECL, LVDS, HCSL etc.) in either AC or DC coupling, with proper IN_SEL, FS0, and FS1 setting.
2) The device differential input has equivalent 100ohm differential termination on chip, so PCB 100ohm external termination is normally not necessary.

7. PI6LC4820 EVB Reference Circuit