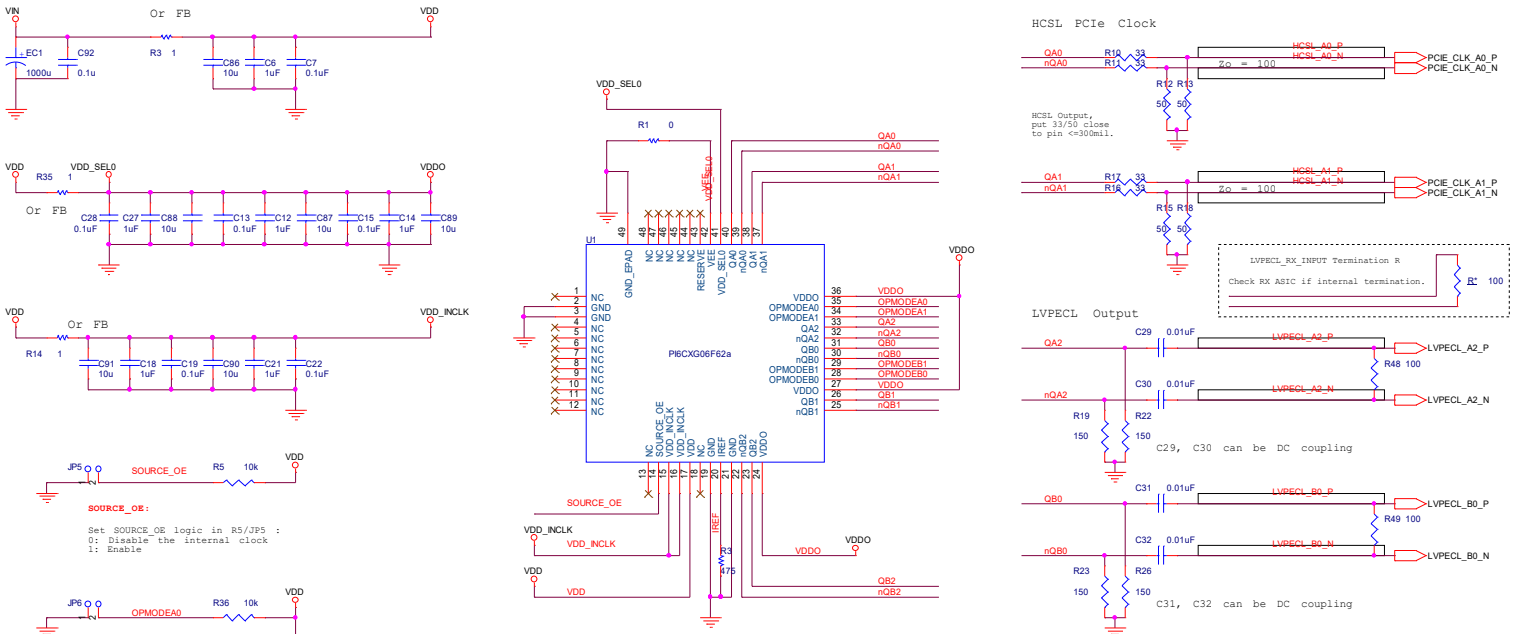


App Note:

1. Each VDD pin needs 0.1u +1uF decoupling close to pin.

2. VDD uses small R=1-2 ohm or FB(ferrite bead)+C=10uF filtering for better DC/DC ripple noise rejection

3. This is HCSL type output: Place 33ohm serial and 50 ohm pull down <250mil close to IC output pins on comp. side.

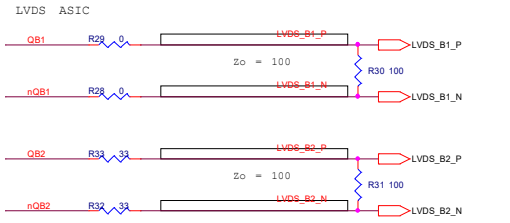
4. LVPECL Output: Place 150ohm pull-down in comp. side close to pin <=300mil.
HCSL Output: Place serial 33 ohm and 50ohm pull-down in comp. side close to pin <=300mil.

5. Suggest to use DC coupling in LVPECL/LVDS drive input clock with 100ohm cross at input pins <200mil; HCSL drive input clock without 100 ohm cross at input pins.

6. when in AC input drive either just use 100ohm cross to bias balance

7. Leave un-used 156.25M_Qx+ and 156.25M_Qx- open

8. IREF pin: A 475 ohm resistor to GND.



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Date: Friday, March 29, 2024		Sheet 1 of 1	