**PI6CV304 IBIS Model Check**

**One IBIS Models: PI6CV304.ibs.**

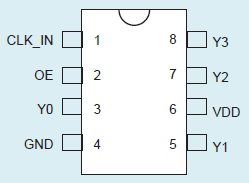
**1. Model Type**

Modify the original PI6CV304.ibs to following two ibis models which are different in packaging, while their pins’ information is the same.

PI6CV304\_L\_RevA.ibs– 8-pin 173-mil wide TSSOP (L)

PI6CV304\_W\_RevA.ibs– 8-pin 150-mil wide SOIC (W)

**[Pin]** signal\_name model\_name **Pin Configuration**

1 CLK\_IN IN

2 OE IN

3 Y0 OUTPUT

4 GND GND

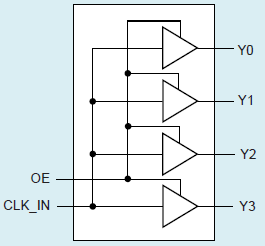
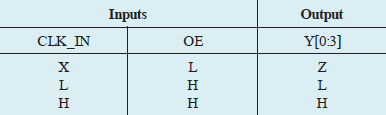
5 Y1 OUTPUT

6 VDD POWER

7 Y2 OUTPUT

8 Y3 OUTPUT

**Block Diagram Function Table**

****

**Conclusion**

The PIN information described in IBIS model is **exactly correct** according to the datasheet.

**2. Internal Series Resistor based on IBIS Model:**

PI6CV304\_L\_RevA.ibs and PI6CV304\_W\_RevA.ibs share the same Pulldwon and Pullup data.

1). **PullDown**: TYP:

V = 0.20054V, I = 0.01232A, so **Rs = 16.27760Ω**

V = -0.20054V, I = -0.01228A, so **Rs = 16.33062Ω**

MIN:

V = 0.20054V, I = 0.011088A, so **Rs = 18.08622Ω**

V = -0.20054V, I = -0.011052A, so **Rs = 18.14513Ω**

MAX:

V = 0.20054V, I = 0.013552A, so **Rs = 14.79782Ω**

V = -0.20054V, I = -0.013508A, so **Rs = 14.84602Ω**

2). **PullUp**: TYP:

V = 0.09958V, I = -0.00614A, so **Rs = 16.21824Ω**

V = -0.09961V, I = 0.00607A, so **Rs = 16.41021Ω**

MIN:

V = 0.09958V, I = -0.005526A, so **Rs = 18.02027Ω**

V = -0.09961V, I = 0.005463A, so **Rs = 18.23357Ω**

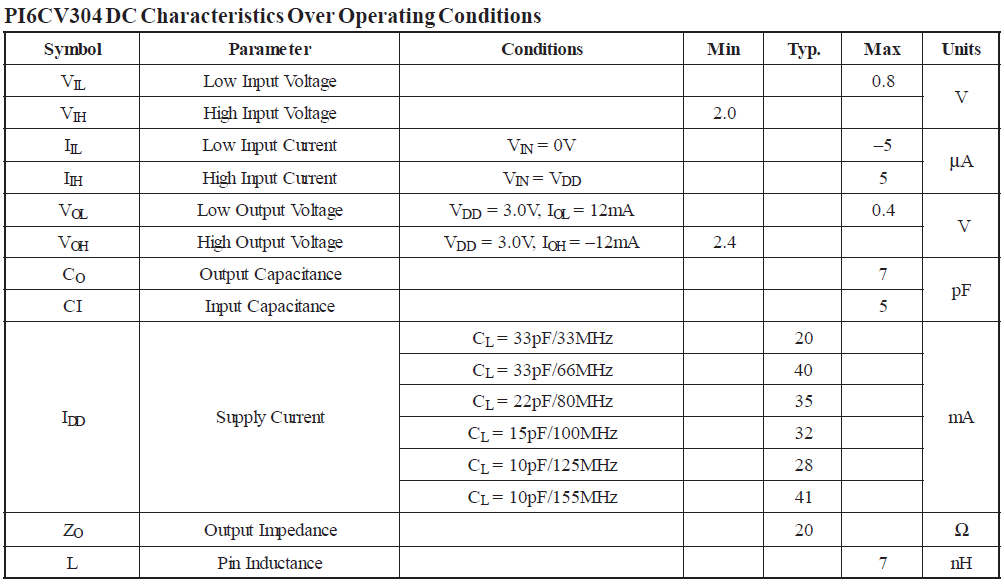
MAX:

V = 0.09958V, I = -0.006754A, so **Rs = 14.74386Ω**

V = -0.09961V, I = 0.006677A, so **Rs = 14.91838Ω**

**Conclusion:**

The values of Internal Series Resistor based on IBIS model are quite **correct** according to the datasheet.



**3. Analog Switch simulation result with following circuit diagram:**

Input signal frequency is **125MHz**: vin clk\_in 0 pulse(0 clamp 0n 0.1n 0.1n 3.9n 8n)

1) Without trace, and add **50Ω pull-down** resistor and **5pF** **pull-down** capacitance to the output.

PI6CV304

OUT

**SCL\_C**

**SDA\_C**

50Ω

**SCL\_C**

**SDA\_C**

IN

**SCL\_C**

**SDA\_C**

C

**SCL\_C**

**SDA\_C**

**IN**

**SCL\_C**

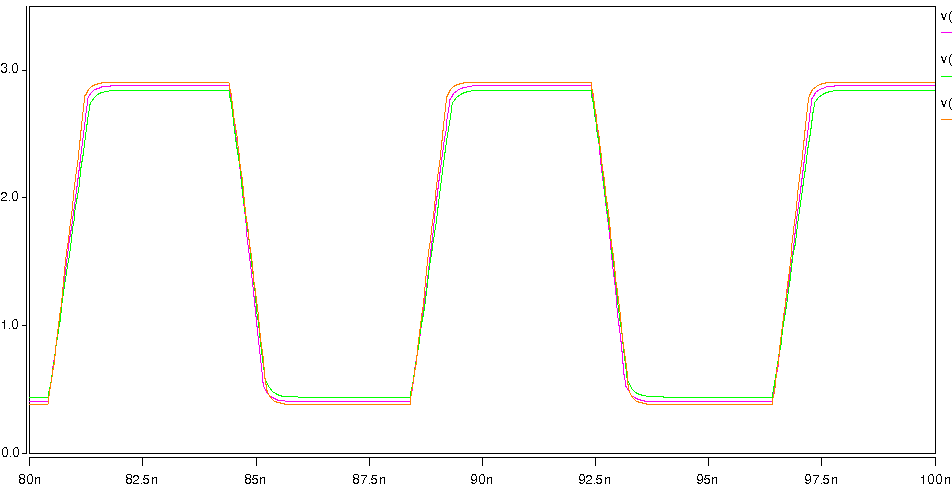
**SDA\_C**

VDD/2

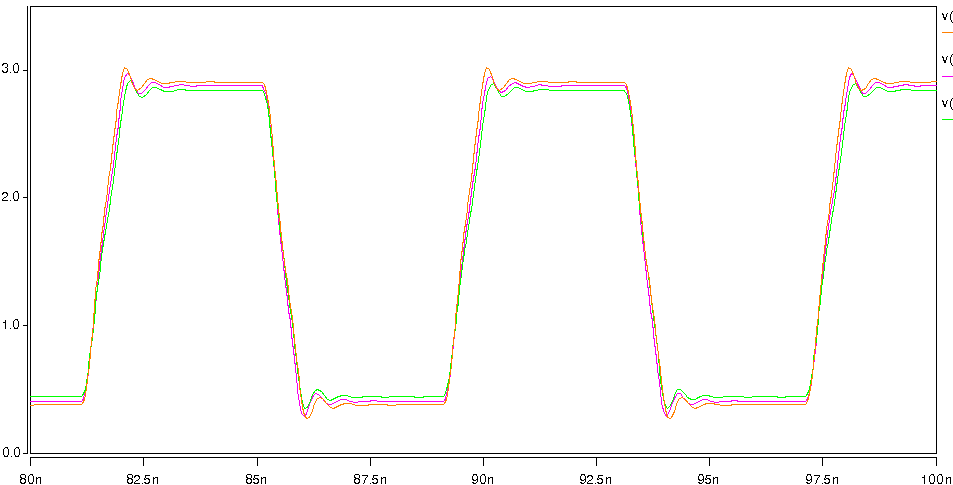
**SCL\_C**

**SDA\_C**

Without Package:



With Package:



2) With **2inch trace** beforethe output

PI6CV304

OUT1

**SCL\_C**

**SDA\_C**

25Ω / 33Ω

**SCL\_C**

**SDA\_C**

50Ω

**SCL\_C**

**SDA\_C**

IN

**SCL\_C**

**SDA\_C**

C

**SCL\_C**

**SDA\_C**

OUT

**SCL\_C**

**SDA\_C**

**IN**

**SCL\_C**

**SDA\_C**

OUT0

**SCL\_C**

**SDA\_C**

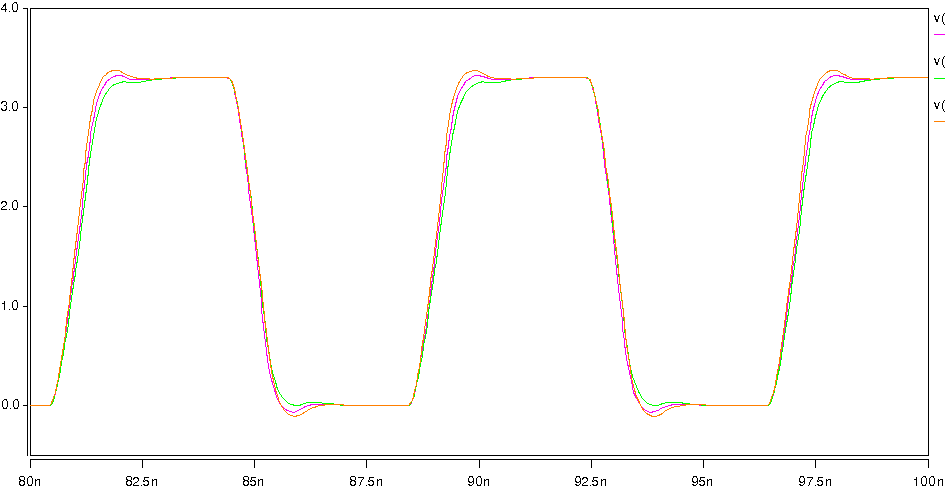
Trace=2inch

**SCL\_C**

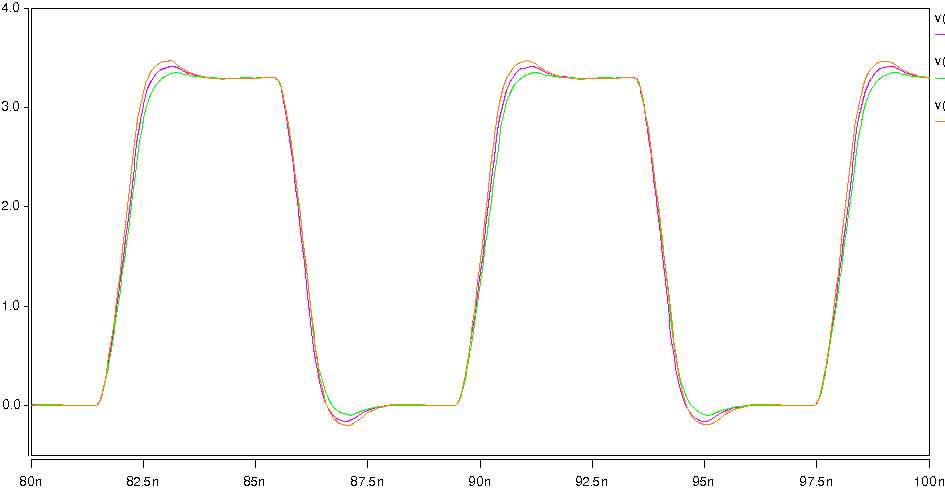
**SDA\_C**

a. Add **25Ω** resistor, **2inch trace** and **5pF** **pull-down** capacitance to the output.

Without Package:

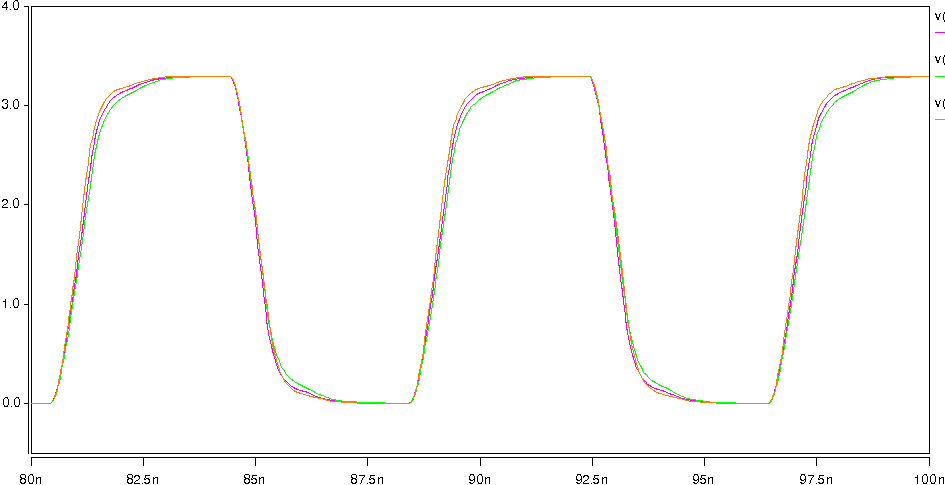


With Package:

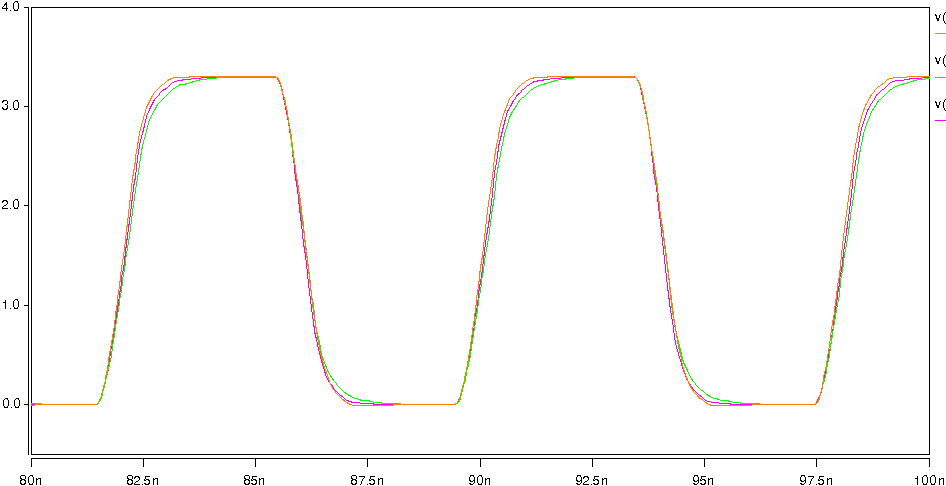


b. Add **33Ω** resistor, **2inch trace** and **5pF** **pull-down** capacitance to the output.

Without Package:



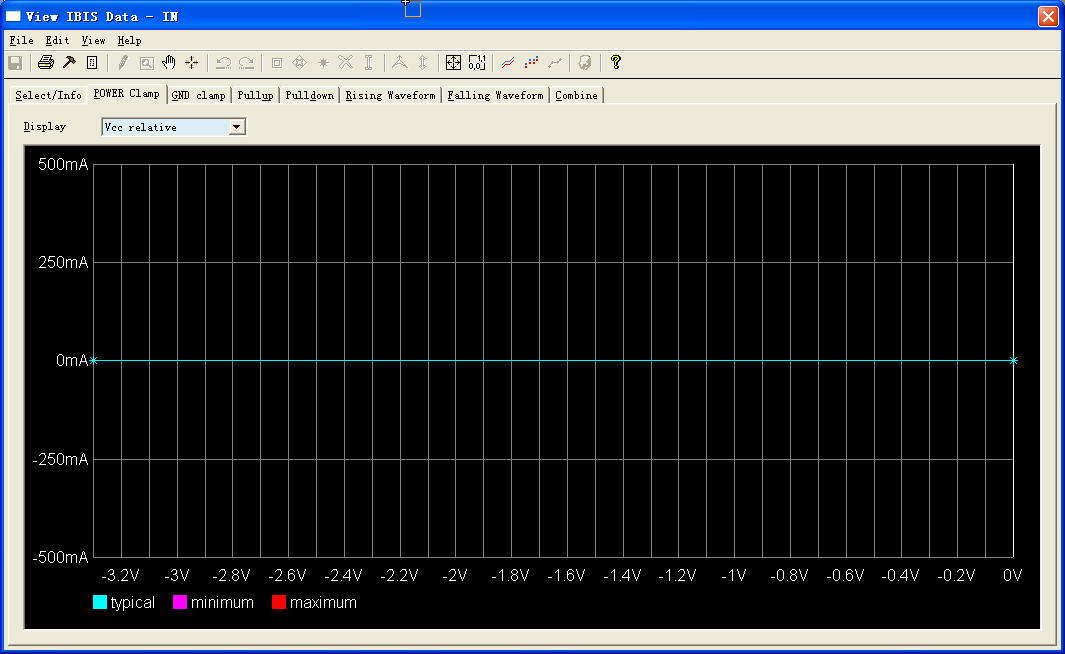
With Package:



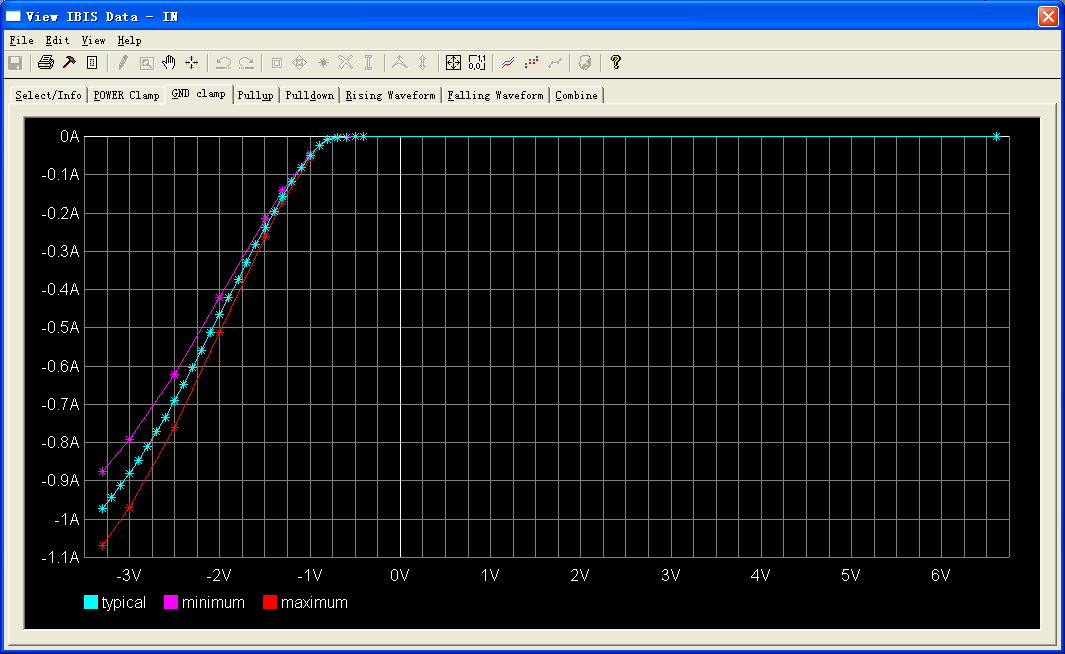
**4. IBIS Data Graph of PI6CV304\_L\_RevA.ibs and PI6CV304\_W\_RevA.ibs**

**(1) Model IN: C\_comp=4.000pF**

a. POWER Clamp

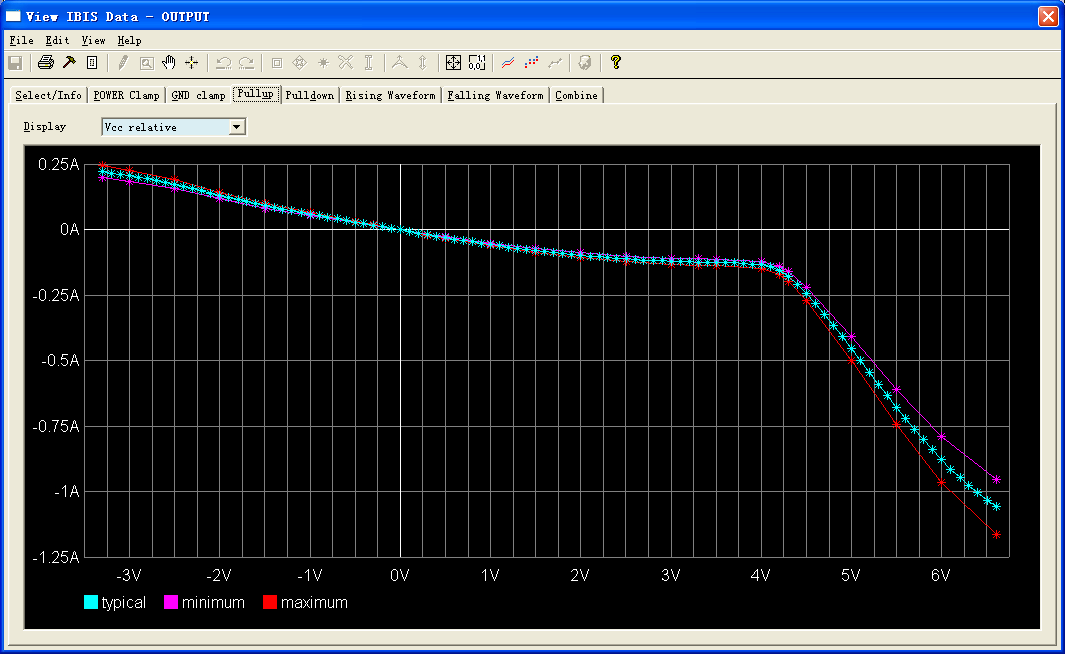
****

b. GND Clamp

****

**(2) Model TRI\_OUT: C\_comp=6.000pF**

a. Pullup

****

b. Pulldown

