



R1, R2, SMBUS Address set

\* C1=C2=8pF for CL=8pF crystal, other CL value crystal use C1=C2=2xCL-8

25M CMOS for LAN Ref. CLK

Put close pin <300mil

Put close to pin <300mil

**8 Low Power HCSL Output**

**App Note:**

1. All VDD pin needs 0.1u +1uF decoupling cloase to pin, put 0.1uF on comp.side
2. VDDA, VDDOSC use small R+C filtering for better DC/DC ripple noise rejection
3. This is LP-HCSL type output: serial 0 ohm is optional, but it can be replace in 5 to 10 ohm for fine tune the board RX end skew for different trace length if needed
4. Select CL=8pF crystal can C1=C2=8pF, other CL value crystal C1=C2=2xCL-5-3, 3 is PCB C\_stray pF estimation
5. Note SSC\_SEL and SMBUS address (SADR) pins are power on latch once set;
6. Make LVDS clock, it needs AC coupling and then RX side use pull-up/down Rs to bias LVDS level, refer to datasheet;
7. OEx# pins have internal pull-down for enable output
8. Make => 8 vias to GND plane on thermal e-pad

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