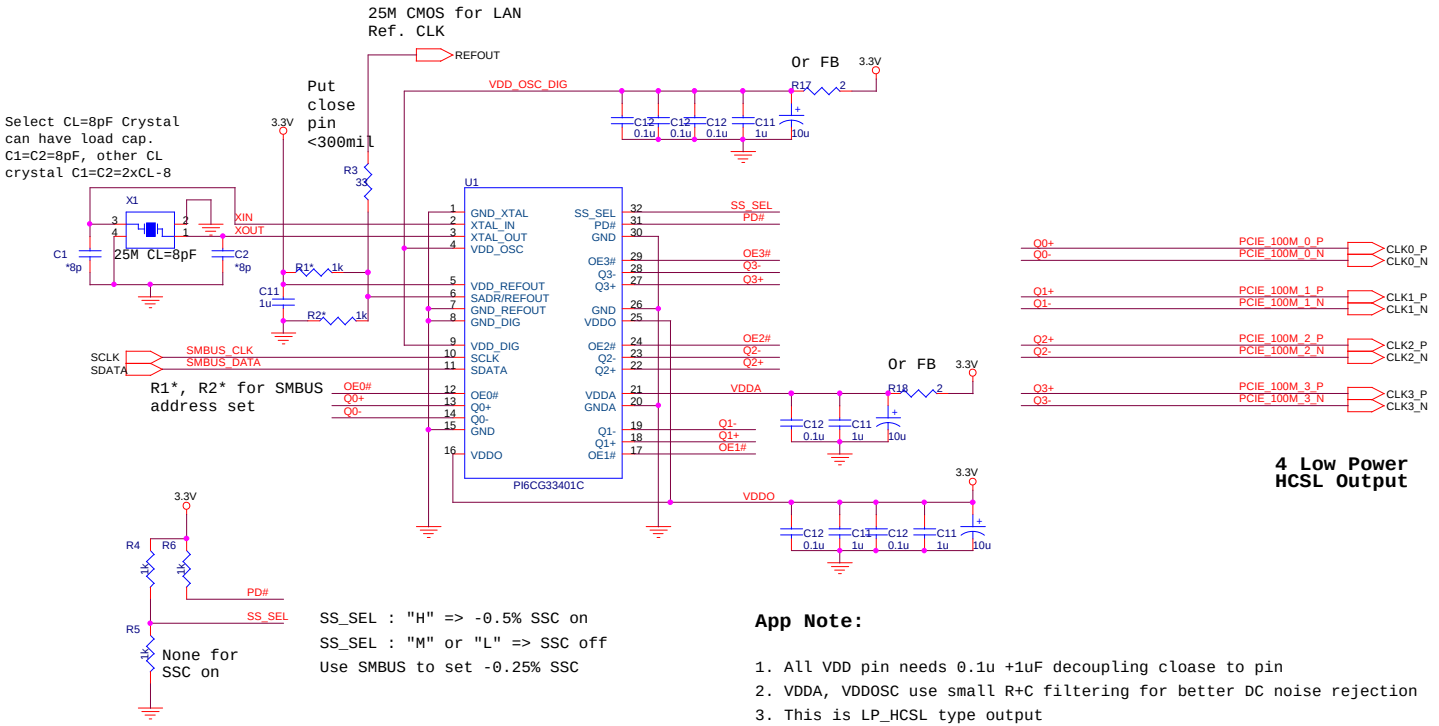

SS_SEL : "H" => -0.5% SSC on

SS_SEL : "M" or "L" => SSC off

Use SMBUS to set -0.25% SSC

App Note:

1. All VDD pin needs 0.1u +1uF decoupling cloase to pin
2. VDDA, VDDOSC use small R+C filtering for better DC noise rejection
3. This is LP_HCSL type output
4. Since OSC pin cap.=5pF so select CL=8pF crystal can C1=C2=8pF, other CL value crystal C1=C2=2xCL-5-3, 3 is C_stray pF
5. Note SSC_EN and SMBUS address pins are power on latch once set;
6. OEx pins have internal pull-down
7. Make LVDS clock, it needs AC coupling and then RX side use pull-up/down Rs to bias LVDS level, refer to datasheet;
8. Connect epad in 6 vias to GND plane

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