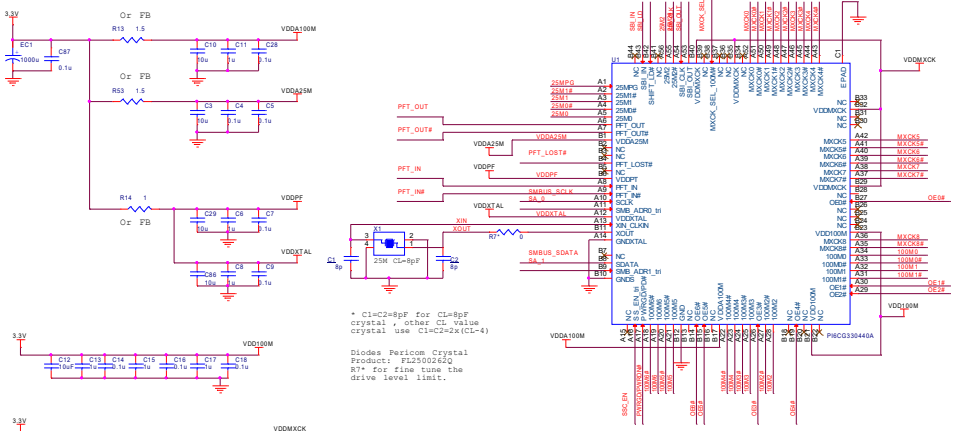
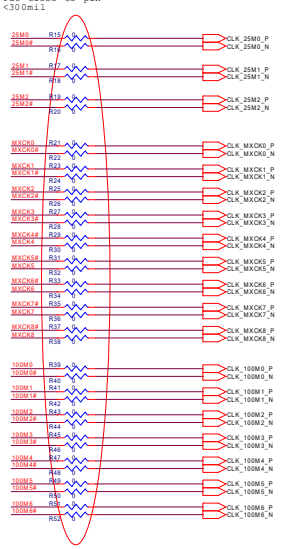
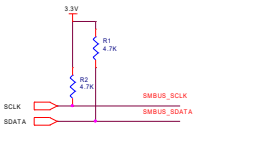


Put close to pin
<300mil



* C1=C2=8pF for CL=8pF crystal , other CL value crystal use C1=C2=2x(CL-4)

Diodes Pericom Crystal Product: FL2500262Q R7* for fine tune the drive level limit.



Make individual OEx# pull-up/down to enable/disable each output

PWRGD/PWRDN#:

Set PWRGD/PWRDN# logic in R4/JP6

0: Power Down Mode;
1: Exit Power Down Mode;

SSC_EN_tri:

Set Spread Spectrum logic in R4/R5

"0"=OFF,"M"=-0.3%,"1"=-0.5%

25MPG:

Set 25MPG logic in R7/JP3 in PWRGD/PWRDN#=0 condition:

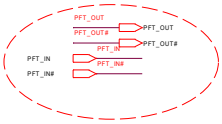
0: Disable 25M[2]
1: Enable 25M[2]

MXCK_SEL_100#:

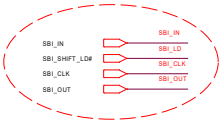
Set MXCK[0:8] frequency in R4/R5

"0"=100MHz
"1"=25MHz

Platform Time Input/Output:

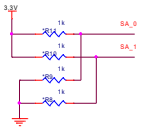


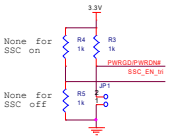
SBI Interface:

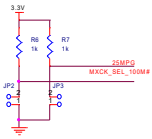


PFT_LOST# - Open Drain Type Assents when PFT_IN, PFT_IN# clock is not present.

SA_0/1 logic in *R11/*R9 *3IO/*R8, refer to datasheet SMBus Address Selection table







App Note:

1. Each VDD pin needs 0.1u +1uF decoupling close to pin. (e.g.: VDDA100M, VDD25M, VDD_XTAL...etc)
2. VDDA100M/25M, VDDXTAL/PF use small R=1~2 ohm or FB(ferrite bead)+C=10uF filtering for better DC/DC ripple noise rejection
3. This is LP-HCSL type output: serial 0 ohm is optional, but it can be replace in 5 to 15 ohm for the optimal fine tune the board RX end wavefrom for different trace length if needed
4. Note SSC_EN_tri and SMBUS address pins are power on latch select only
5. Make LVDS clock, it needs AC coupling and then RX side use pull-up/down Rs to bias LVDS level, refer to datasheet;
6. OEx# pins have internal pull-down, can be left open
7. Connect epad in 8 to 12 vias connected to GND plane

Title	PI6CG330440A Application Schematic	
Size: C	Document Number: Diodes Inc. Clock IC Application Engineering	Rev: 1.0
Date: Friday, March 29, 2024	Sheet 1 of 1	