**Verification of PI6CG18801 IBIS model**

1. **Introduction: to verify the correlation between the ibis model and hspice model, we need to do some simulations:**

**The frequency of signal is 25MHz:**

vin clkin 0 pulse(0 power 0 0.01n 0.01n 19.99n 40n)

1. **Without trace to the OUTPUT:**

PI6CG18801

**VOUT**

**SCL\_C**

**SDA\_C**

**Input Signals**

**SCL\_C**

**SDA\_C**

**VIN**

**SCL\_C**

**SDA\_C**

REFOUT

**SCL\_C**

**SDA\_C**

CLKIN

**SCL\_C**

**SDA\_C**

**…..**

**SCL\_C**

**SDA\_C**

1. **CMOS\_SLOWEST**
2. Simulation **without** package data;
3. Simulation **with** package data.
4. **CMOS\_SLOW**
5. Simulation **without** package data;
6. Simulation **with** package data.
7. **CMOS\_FAST**
8. Simulation **without** package data;
9. Simulation **with** package data.
10. **CMOS\_FASTEST**
11. Simulation **without** package data;
12. Simulation **with** package data.
13. **With 33Ohm resister, 2-inch trace and 5pF pulldown capacitance to the OUTPUT:**

**Input Signals**

**SCL\_C**

**SDA\_C**

**VIN**

**SCL\_C**

**SDA\_C**

**…..**

**SCL\_C**

**SDA\_C**

PI6CB18801

CLKIN

**SCL\_C**

**SDA\_C**

REFOUT

**SCL\_C**

**SDA\_C**

2-inch

**VOUT**

**SCL\_C**

**SDA\_C**

**C**

**SCL\_C**

**SDA\_C**

**R=33Ohm**

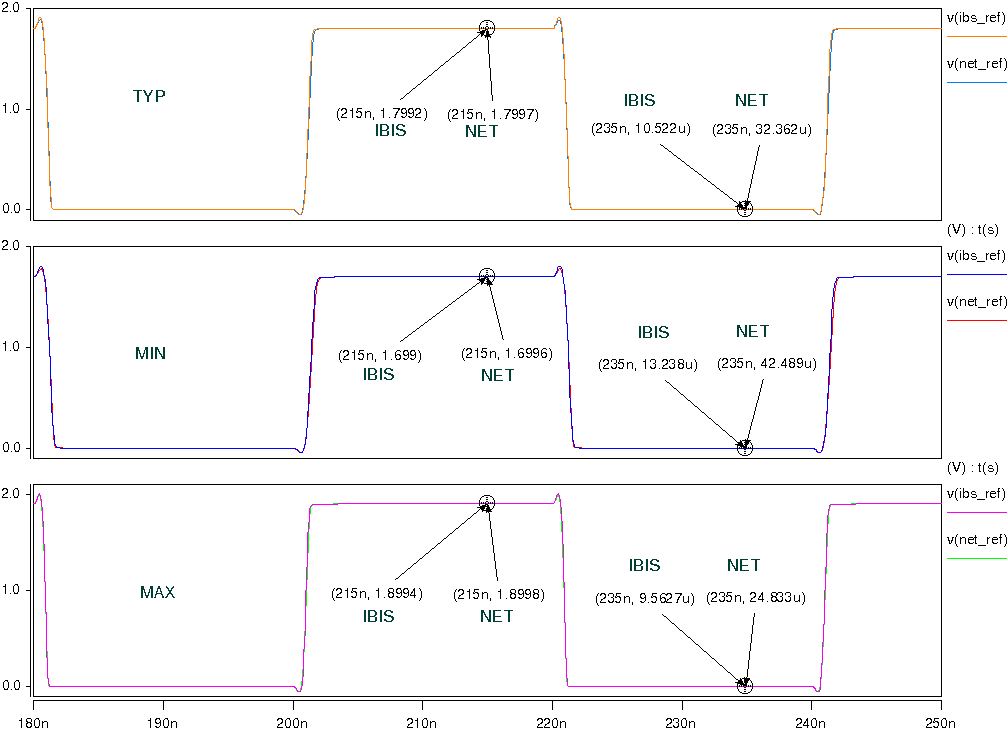
**SCL\_C**

**SDA\_C**

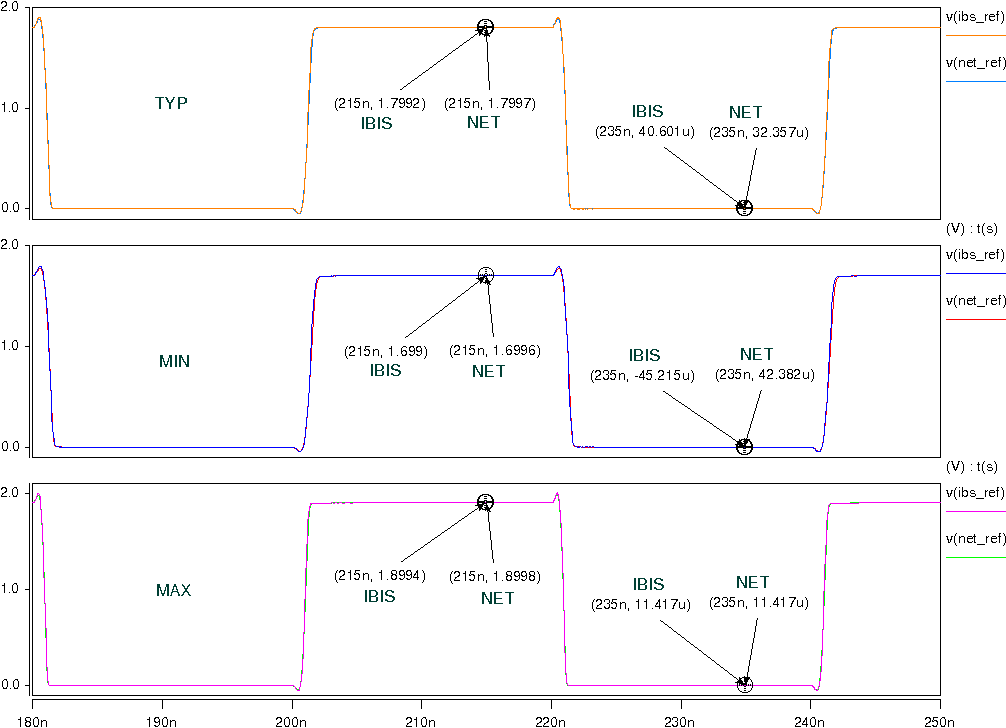
1. **CMOS\_SLOWEST**
2. Simulation **without** package data;
3. Simulation **with** package data.
4. **CMOS\_SLOW**
5. Simulation **without** package data;
6. Simulation **with** package data.
7. **CMOS\_FAST**
8. Simulation **without** package data;
9. Simulation **with** package data.
10. **CMOS\_FASTEST**
11. Simulation **without** package data;
12. Simulation **with** package data.
13. **Conclusion:**

For the verification, the simulation results of IBIS model can match quite well with the HSPICE model at different simulating conditions.

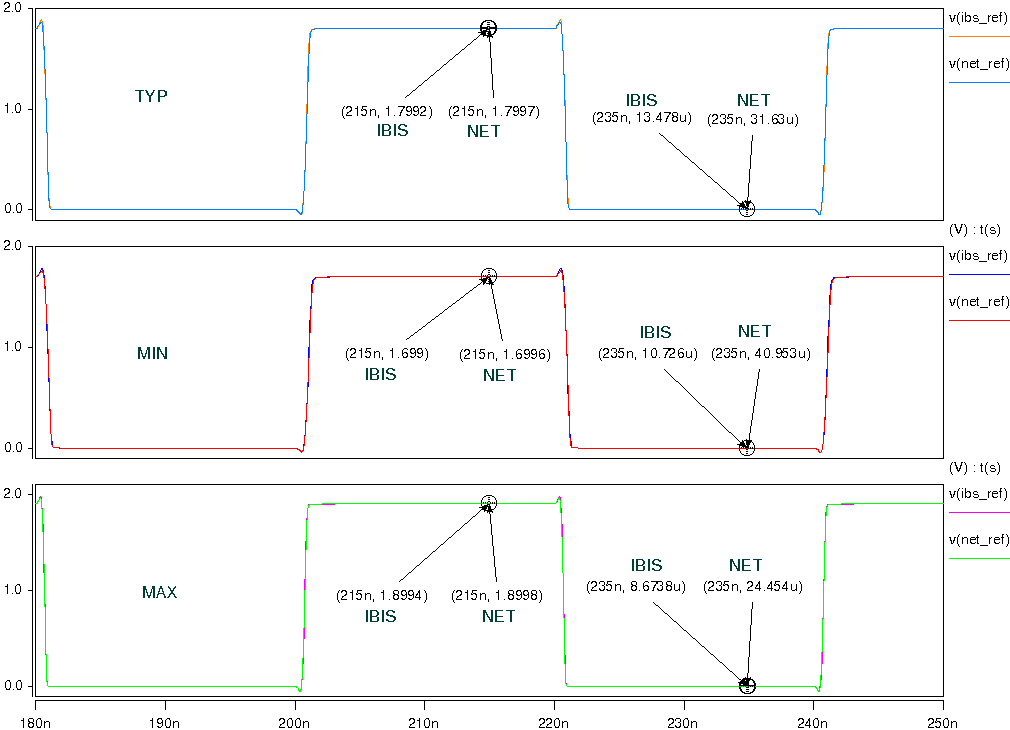
1. **Simulation Result:**
2. **Without trace to the OUTPUT:**
3. **CMOS\_SLOWEST**
4. Simulation **without** package data;



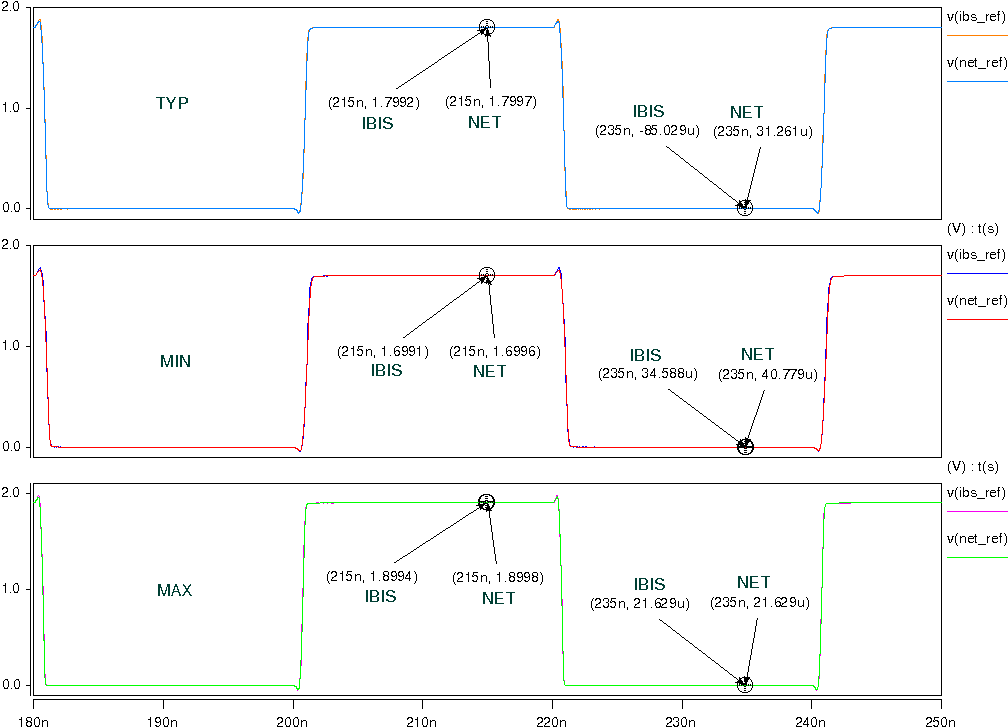
1. Simulation **with** package data.



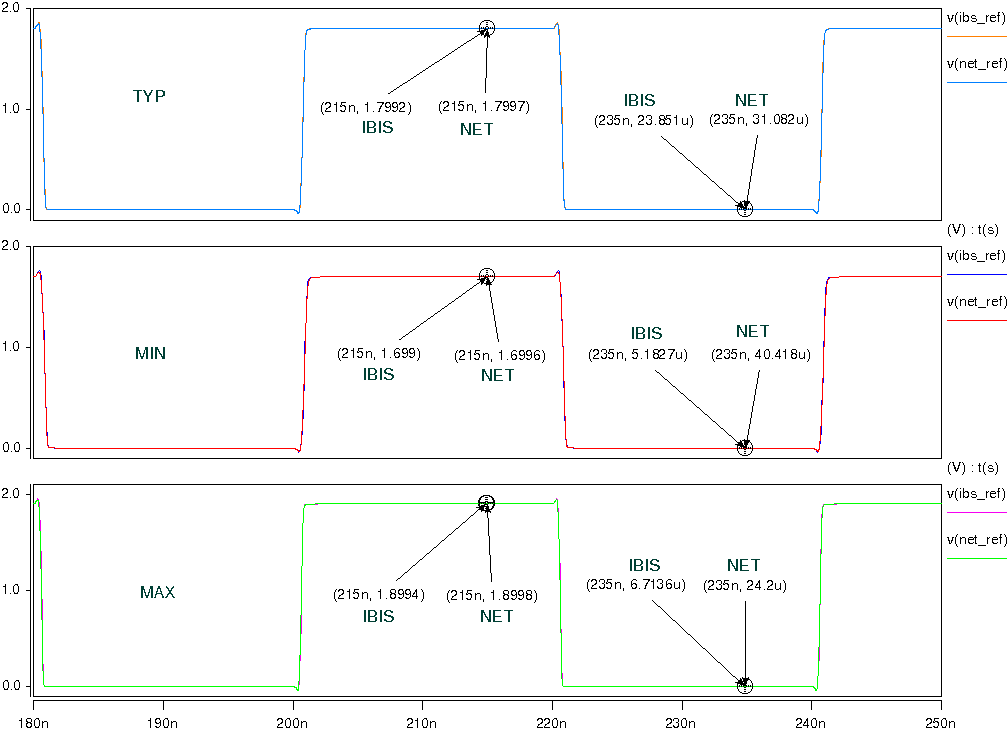
1. **CMOS\_SLOW**
2. Simulation **without** package data;



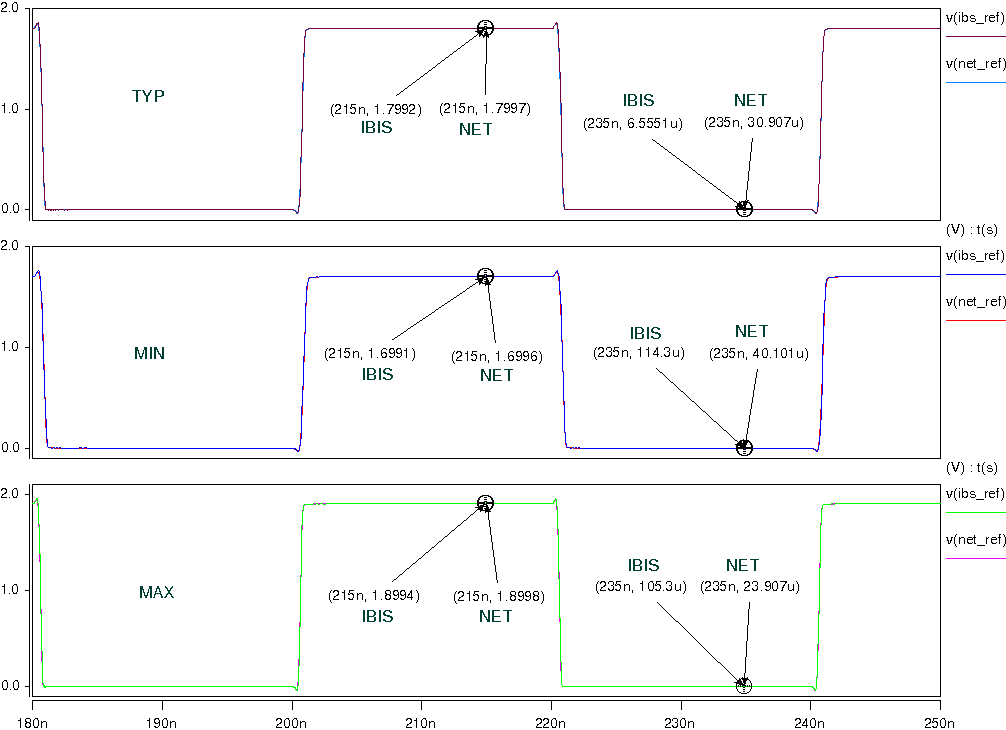
1. Simulation **with** package data.



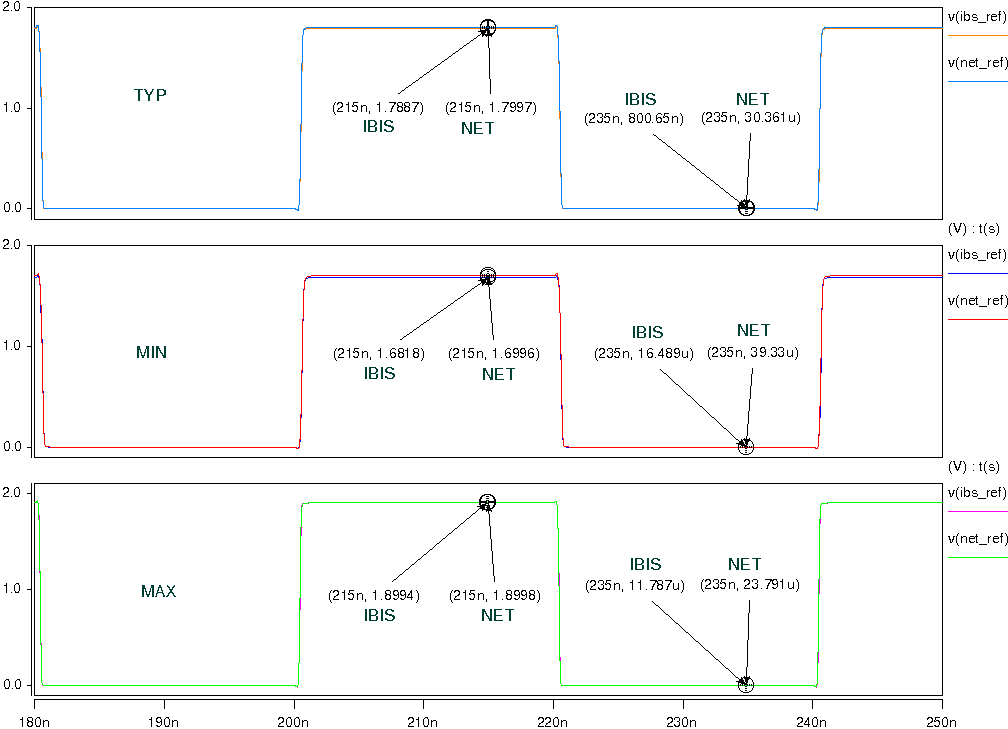
1. **CMOS\_FAST**
2. Simulation **without** package data;



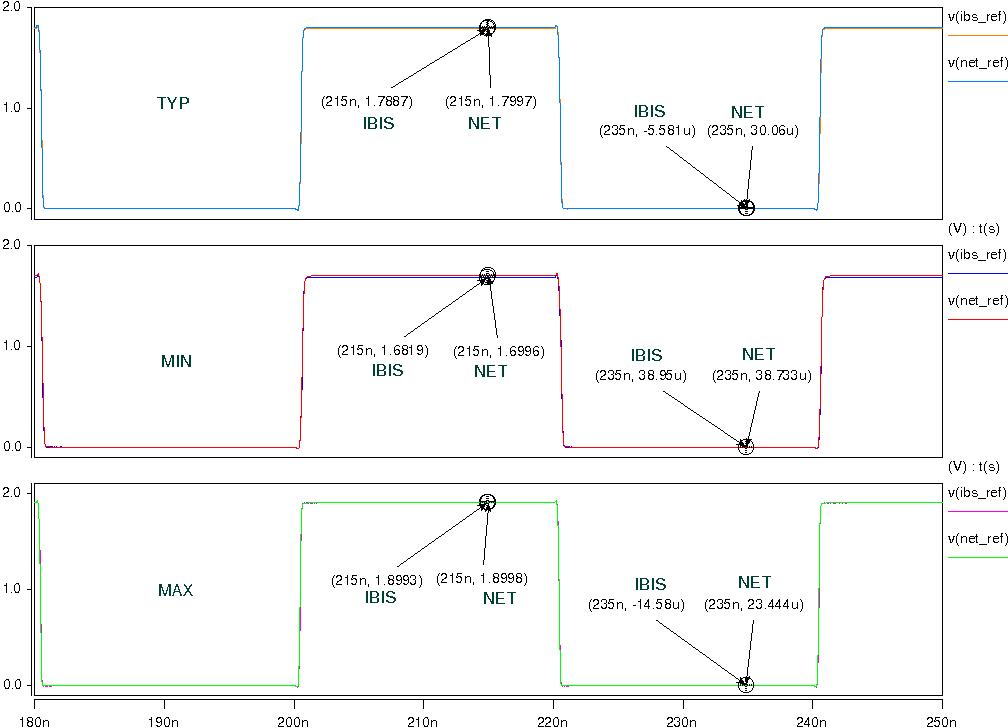
1. Simulation **with** package data.



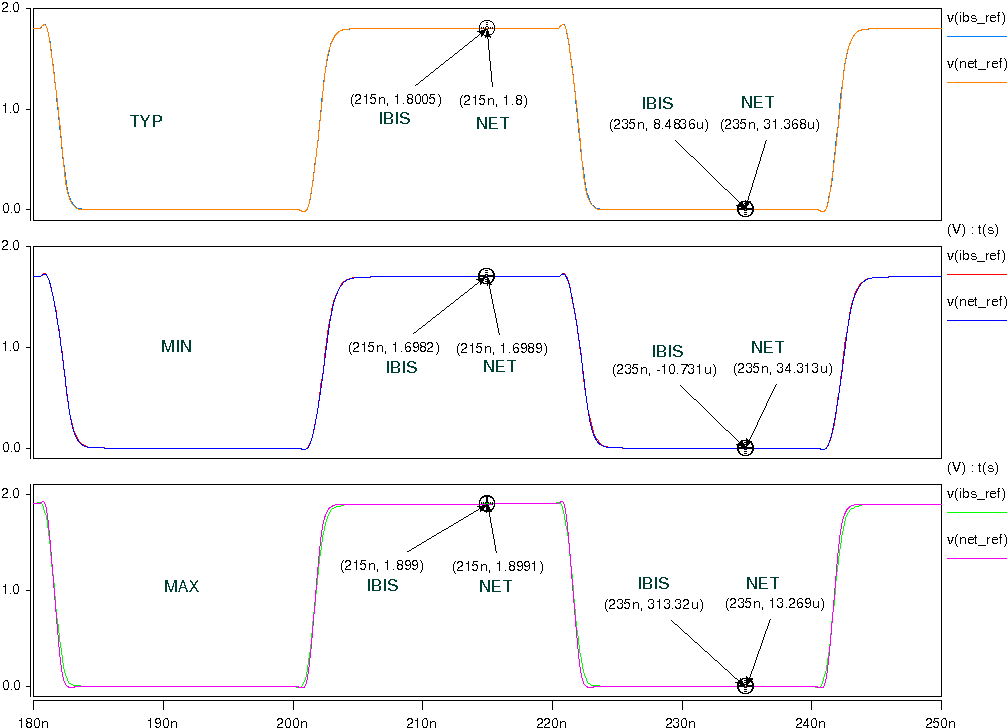
1. **CMOS\_FASTEST**
2. Simulation **without** package data;



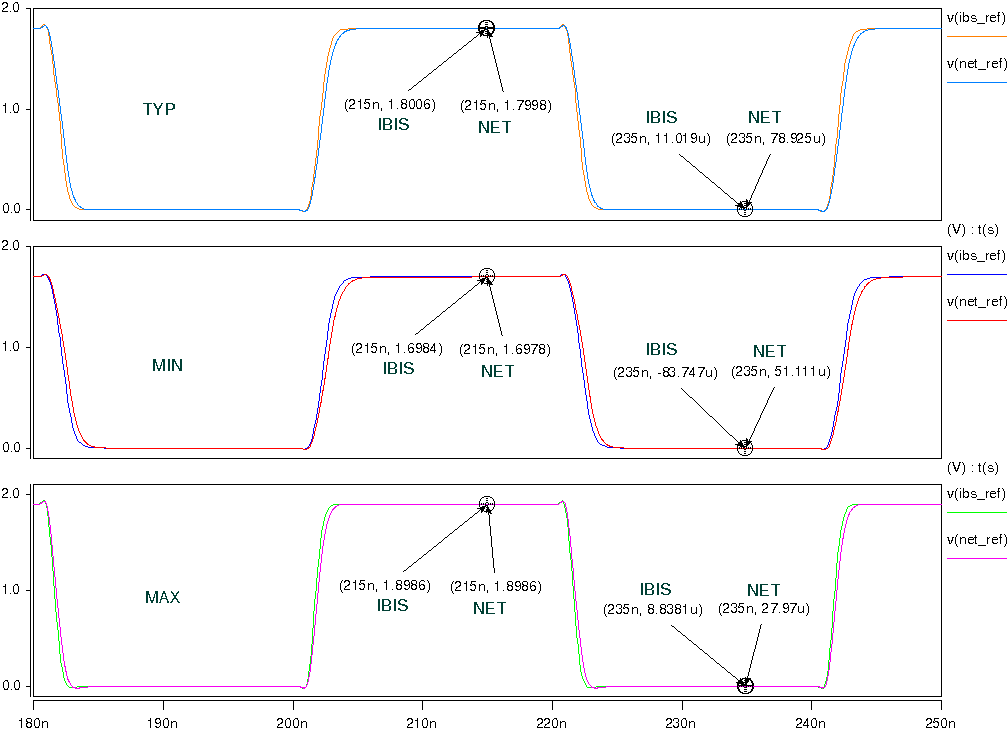
1. Simulation **with** package data.



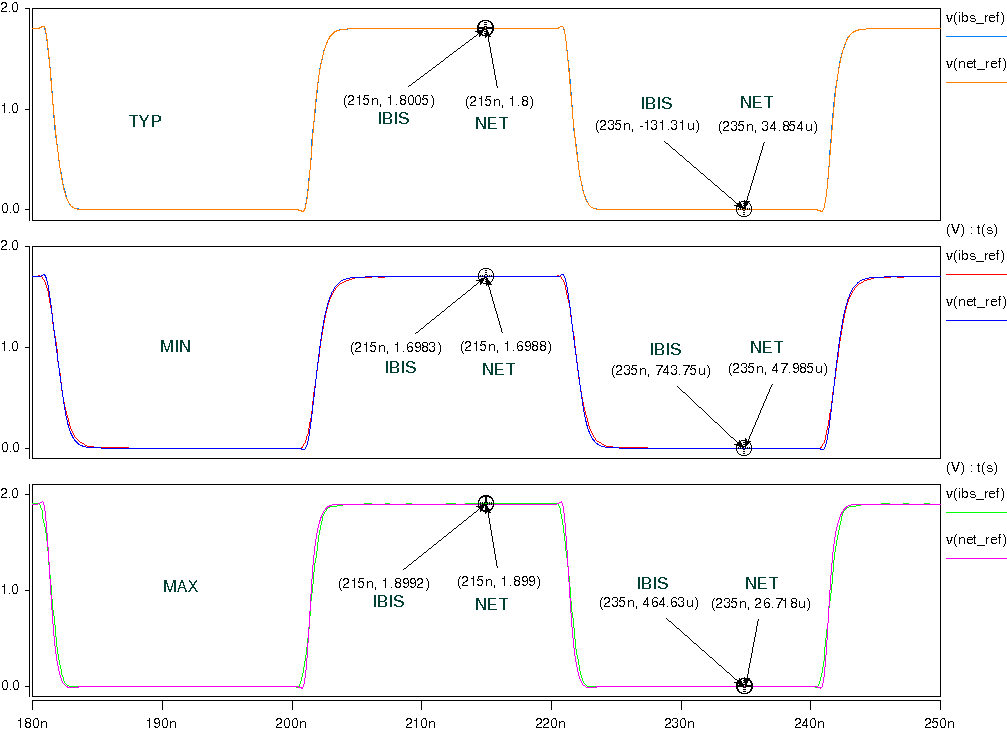
1. **With 33Ohm resister, 2-inch trace and 5pF pulldown capacitance to the OUTPUT:**
2. **CMOS\_SLOWEST**
3. Simulation **without** package data;



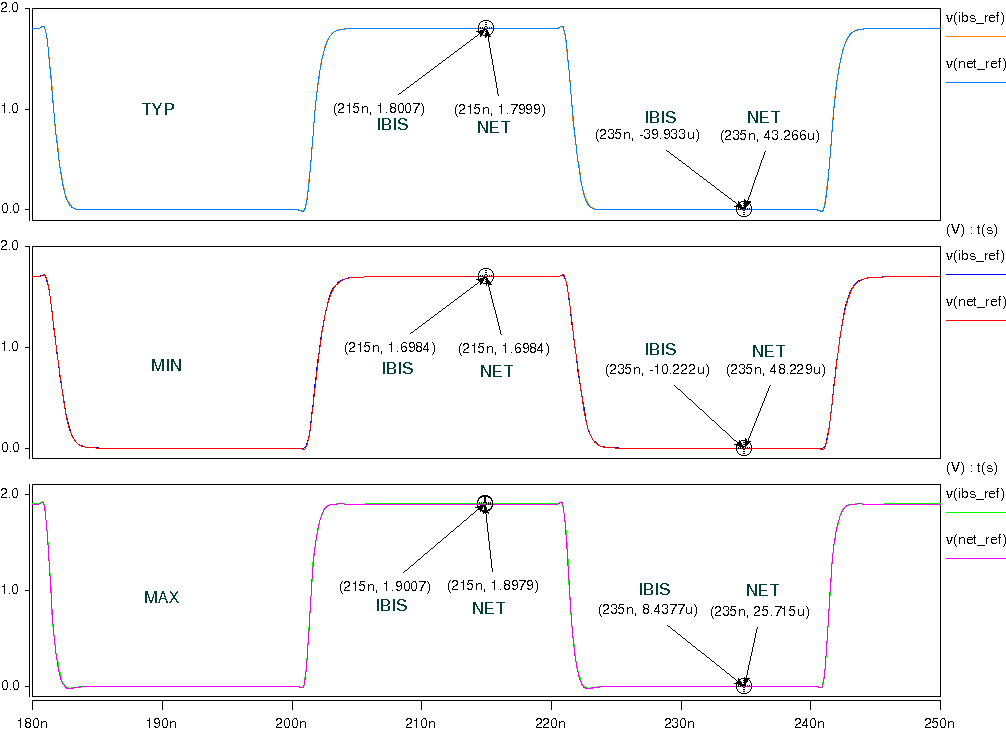
1. Simulation **with** package data.



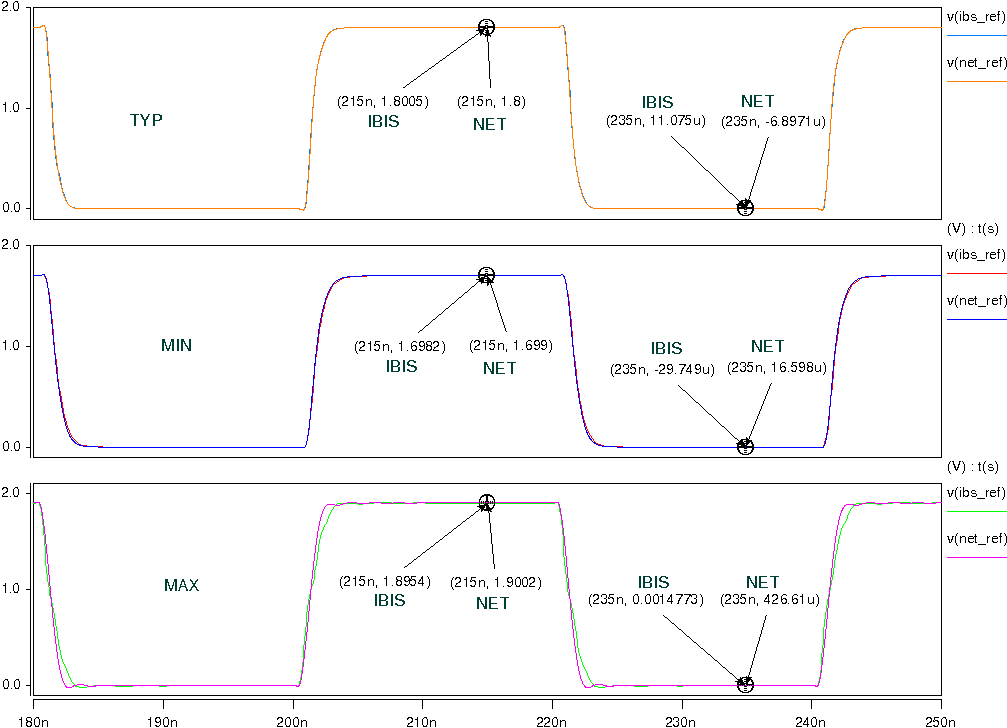
1. **CMOS\_SLOW**
2. Simulation **without** package data;



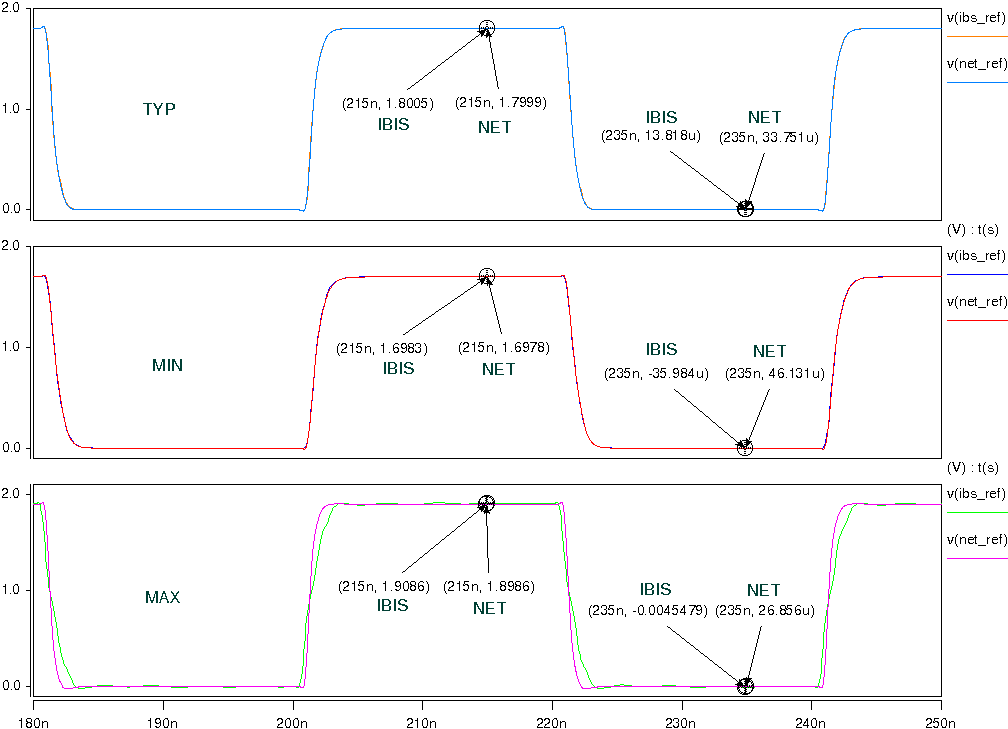
1. Simulation **with** package data.



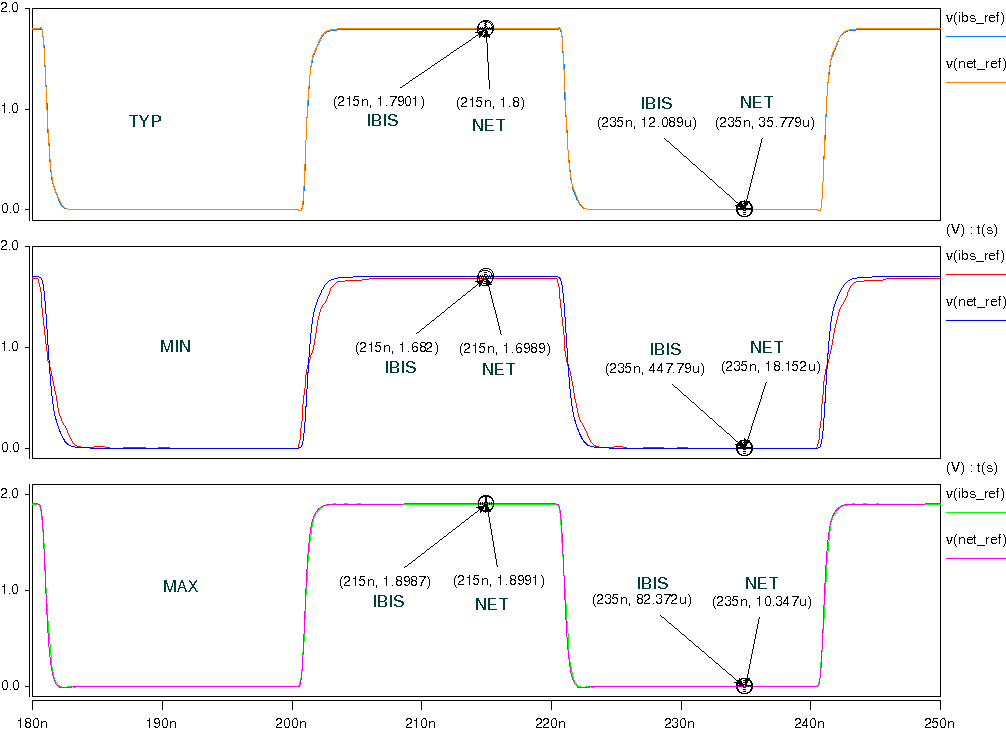
1. **CMOS\_FAST**
2. Simulation **without** package data;



1. Simulation **with** package data.



1. **CMOS\_FASTEST**
2. Simulation **without** package data;



1. Simulation **with** package data.

