**Verification of PI6CG18801 IBIS model**

1. **Introduction: to verify the correlation between the ibis model and hspice model, we need to do some simulations:**

**The frequency of signal is 50MHz:**

vvin clkin 0 pulse(0 power 0 0.1n 0.1n 9.9n 20n)

**Note:** DIF0 🡪 Q0+; DIF0# 🡪 Q0- .

1. **Without trace to the HCSL:**

PI6CG18801

**VOUT**

**SCL\_C**

**SDA\_C**

**Input Signals**

**SCL\_C**

**SDA\_C**

**VIN**

**SCL\_C**

**SDA\_C**

DIF0

**SCL\_C**

**SDA\_C**

CLKIN

**SCL\_C**

**SDA\_C**

**VOUT**

**SCL\_C**

**SDA\_C**

DIF0#

**SCL\_C**

**SDA\_C**

**…..**

**SCL\_C**

**SDA\_C**

1. **HCSL\_0P6\_FAST**
2. Simulation **without** package data;
3. Simulation **with** package data.
4. **HCSL\_0P6\_SLOW**
5. Simulation **without** package data;
6. Simulation **with** package data.
7. **HCSL\_0P7\_FAST**
8. Simulation **without** package data;
9. Simulation **with** package data.
10. **HCSL\_0P7\_SLOW**
11. Simulation **without** package data;
12. Simulation **with** package data.
13. **HCSL\_0P8\_FAST**
14. Simulation **without** package data;
15. Simulation **with** package data.
16. **HCSL\_0P8\_SLOW**
17. Simulation **without** package data;
18. Simulation **with** package data.
19. **HCSL\_0P9\_FAST**
20. Simulation **without** package data;
21. Simulation **with** package data.
22. **HCSL\_0P9\_SLOW**
23. Simulation **without** package data;
24. Simulation **with** package data.
25. **With 5-inch trace and 2pF pulldown capacitance to the HCSL:**

**VOUT**

**SCL\_C**

**SDA\_C**

CLKIN

**SCL\_C**

**SDA\_C**

**Input Signals**

**SCL\_C**

**SDA\_C**

**VIN**

**SCL\_C**

**SDA\_C**

DIF0

**SCL\_C**

**SDA\_C**

**…..**

**SCL\_C**

**SDA\_C**

5-inch

PI6CG18801

**VOUT**

**SCL\_C**

**SDA\_C**

DIF0#

**SCL\_C**

**SDA\_C**

5-inch

**C**

**SCL\_C**

**SDA\_C**

**C**

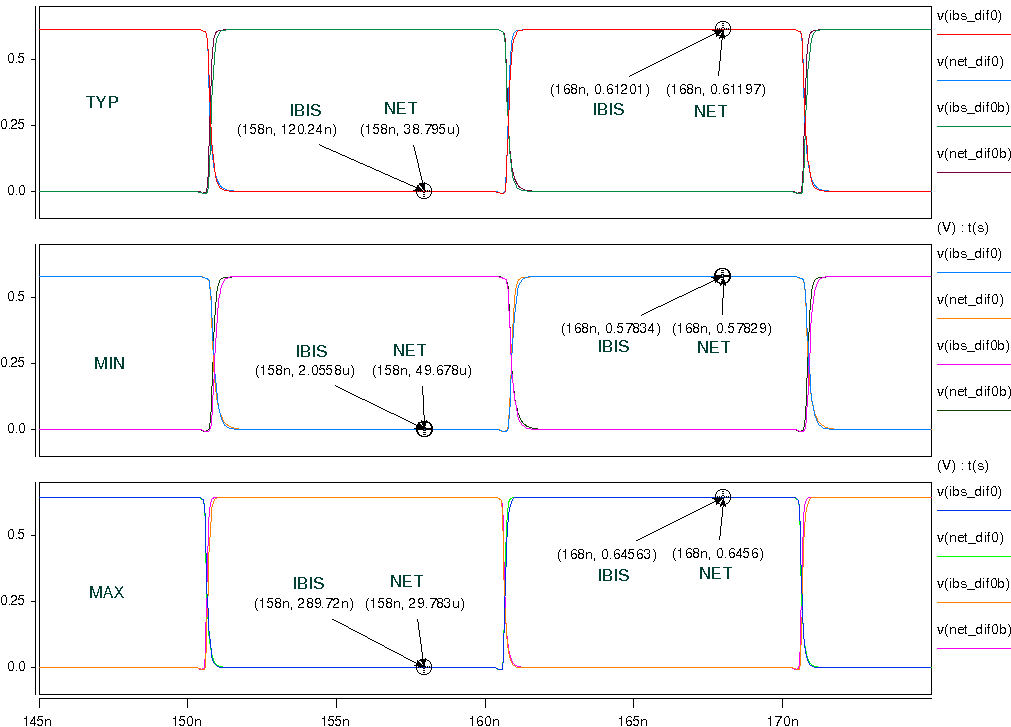
**SCL\_C**

**SDA\_C**

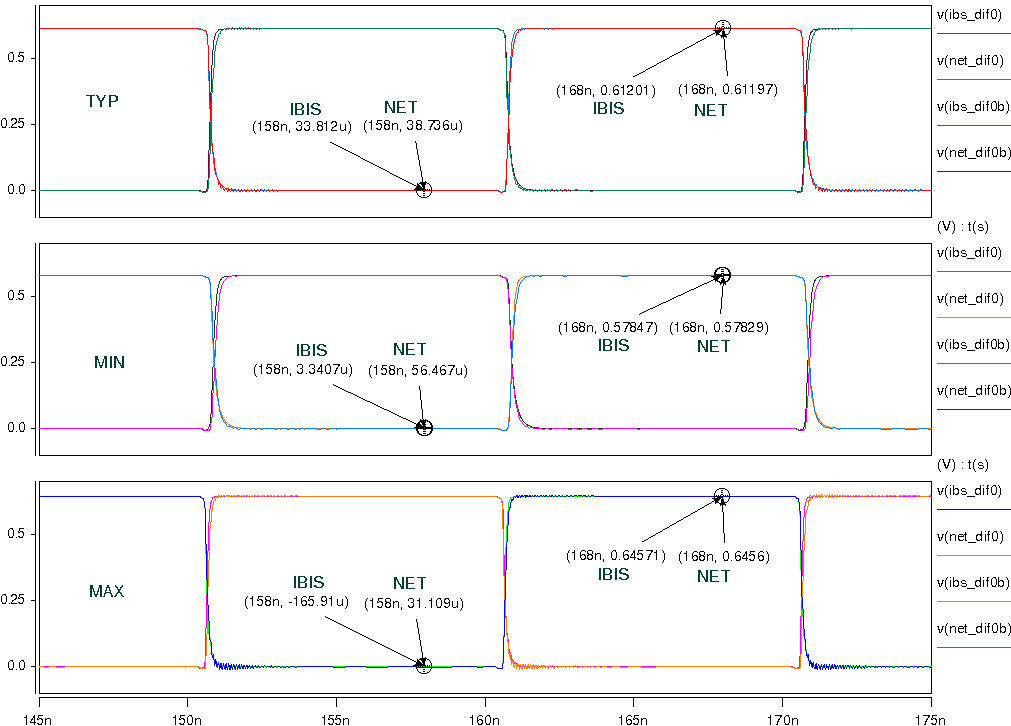
1. **HCSL\_0P6\_FAST**
2. Simulation **without** package data;
3. Simulation **with** package data.
4. **HCSL\_0P6\_SLOW**
5. Simulation **without** package data;
6. Simulation **with** package data.
7. **HCSL\_0P7\_FAST**
8. Simulation **without** package data;
9. Simulation **with** package data.
10. **HCSL\_0P7\_SLOW**
11. Simulation **without** package data;
12. Simulation **with** package data.
13. **HCSL\_0P8\_FAST**
14. Simulation **without** package data;
15. Simulation **with** package data.
16. **HCSL\_0P8\_SLOW**
17. Simulation **without** package data;
18. Simulation **with** package data.
19. **HCSL\_0P9\_FAST**
20. Simulation **without** package data;
21. Simulation **with** package data.
22. **HCSL\_0P9\_SLOW**
23. Simulation **without** package data;
24. Simulation **with** package data.
25. **Conclusion:**

For the verification, the simulation results of IBIS model can match quite well with the HSPICE model at most of different simulating conditions.

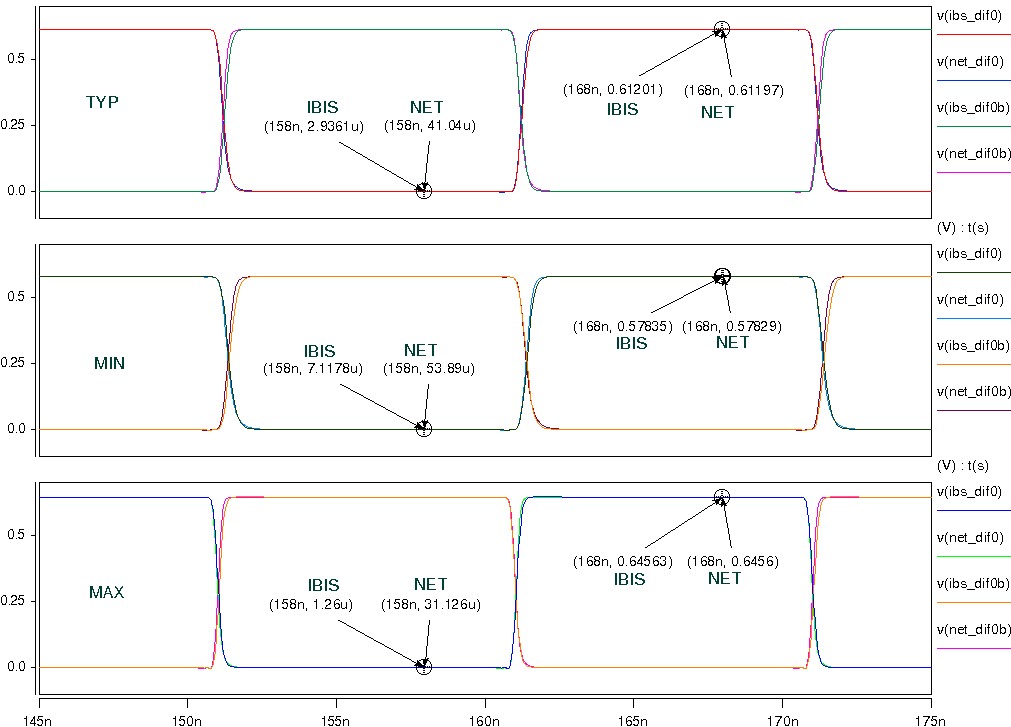
1. **Simulation Result: (DIF0 🡪 Q0+; DIF0# 🡪 Q0-)**
2. **Without trace to the HCSL:**
3. **HCSL\_0P6\_FAST**
4. Simulation **without** package data;



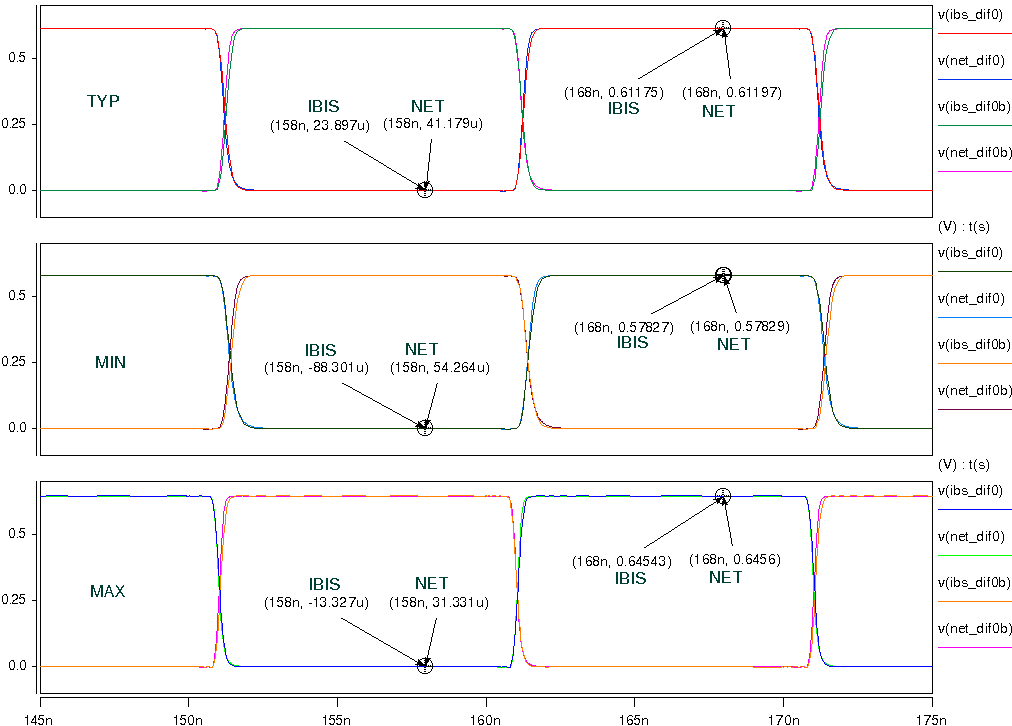
1. Simulation **with** package data.



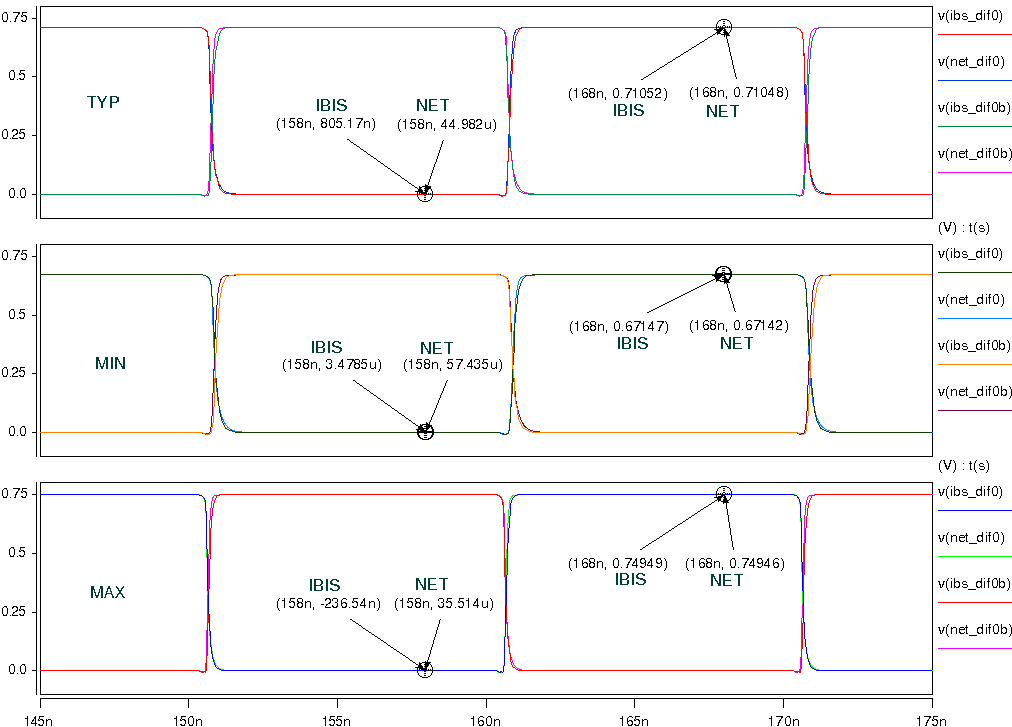
1. **HCSL\_0P6\_SLOW**
2. Simulation **without** package data;



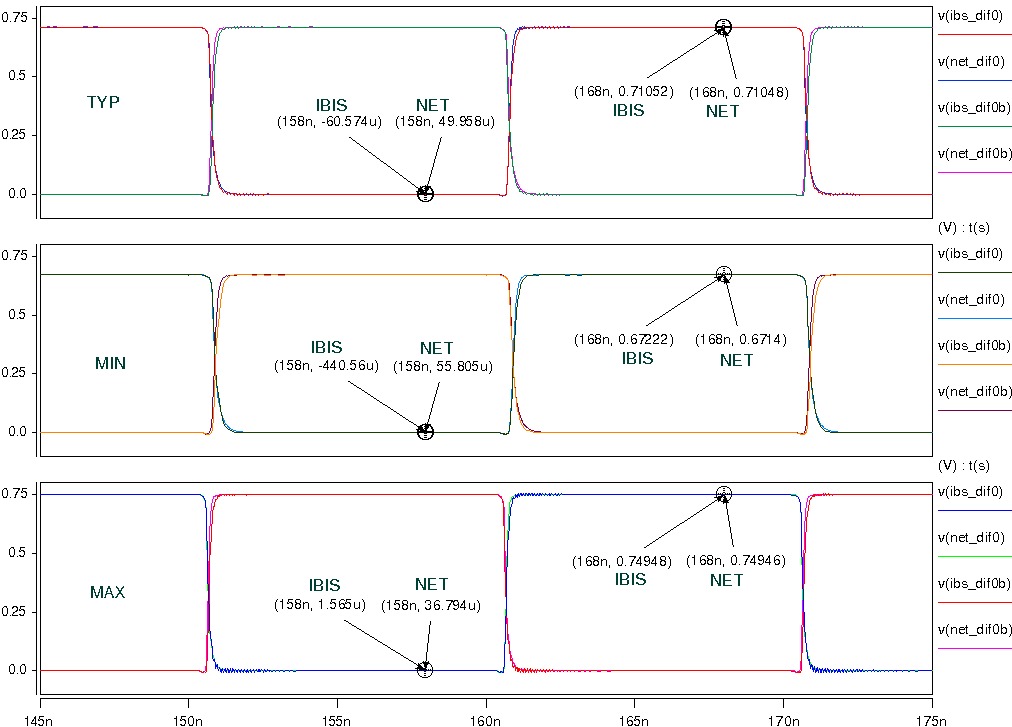
1. Simulation **with** package data.



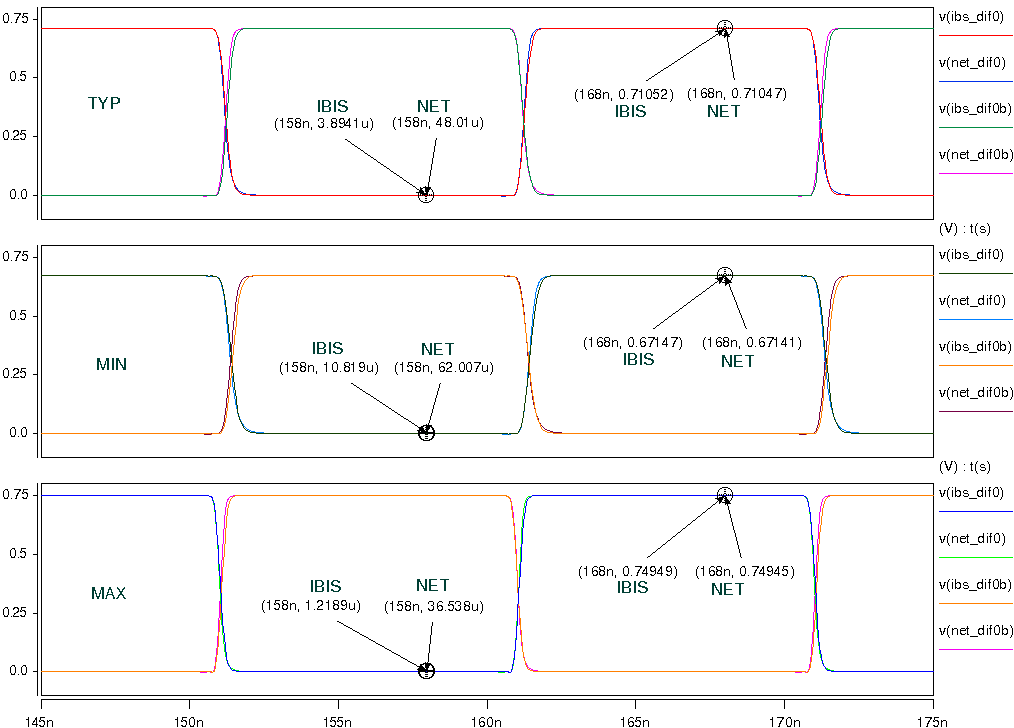
1. **HCSL\_0P7\_FAST**
2. Simulation **without** package data;



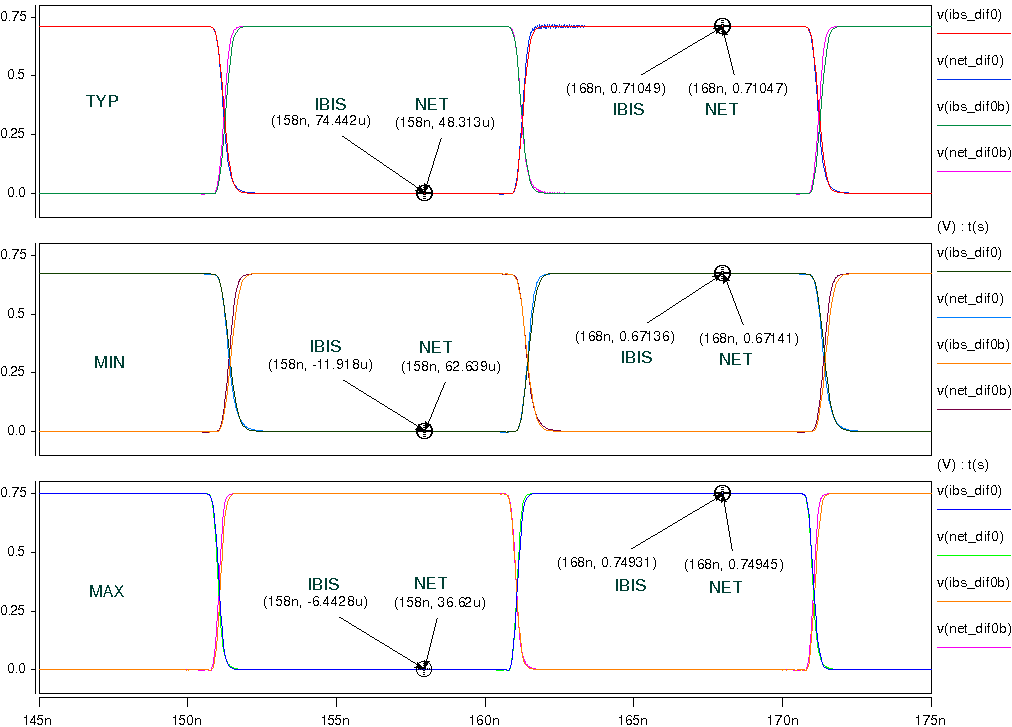
1. Simulation **with** package data.



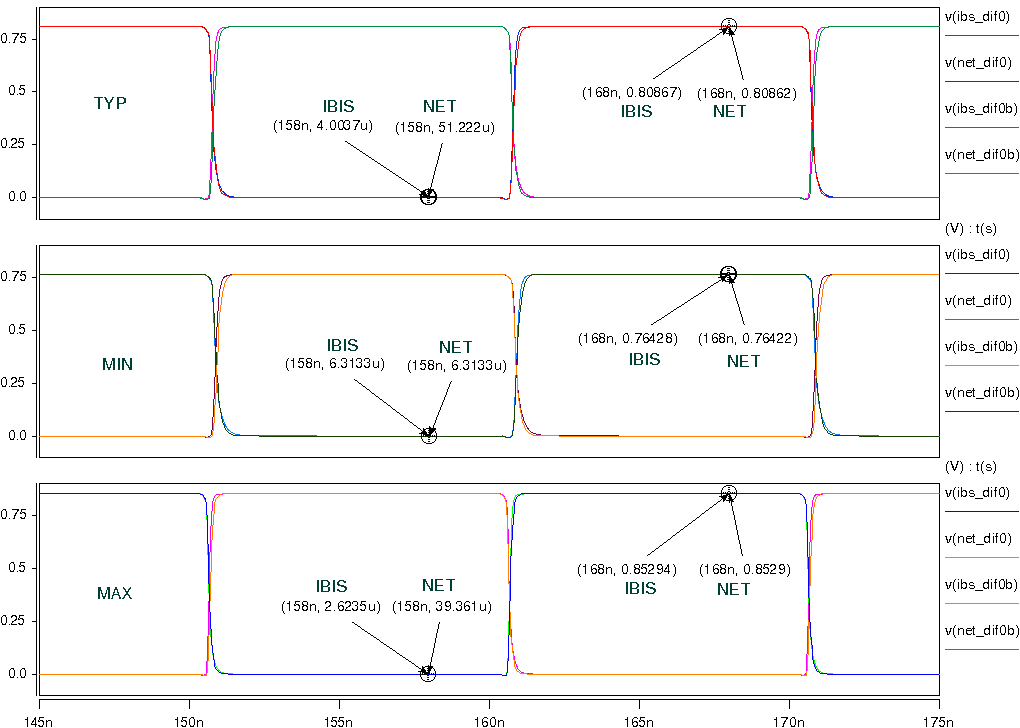
1. **HCSL\_0P7\_SLOW**
2. Simulation **without** package data;



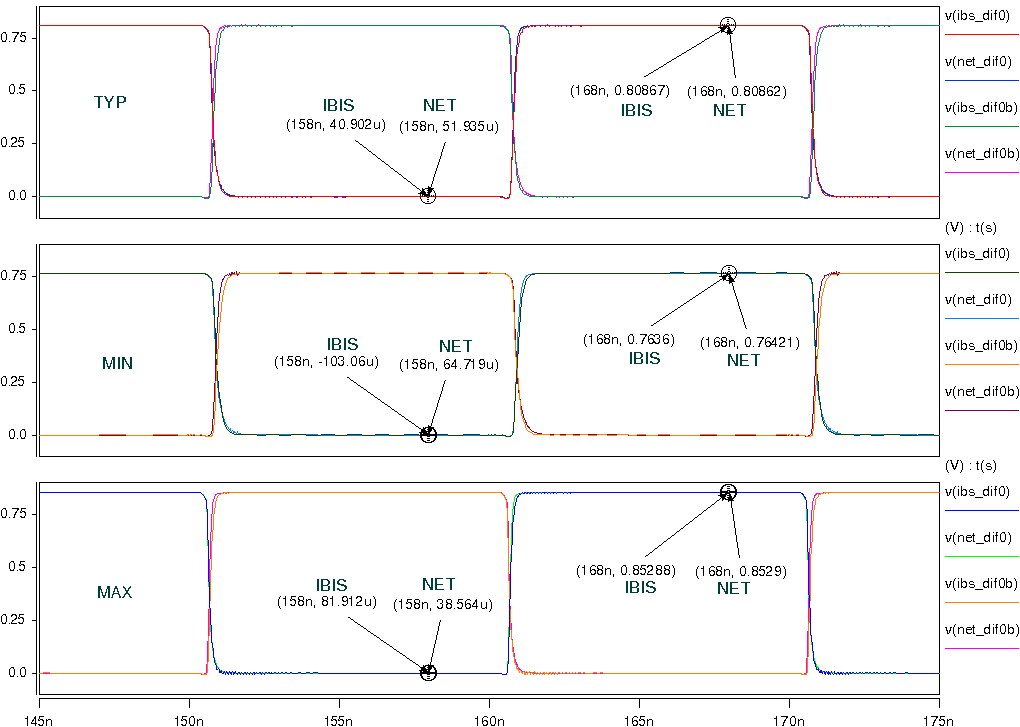
1. Simulation **with** package data.



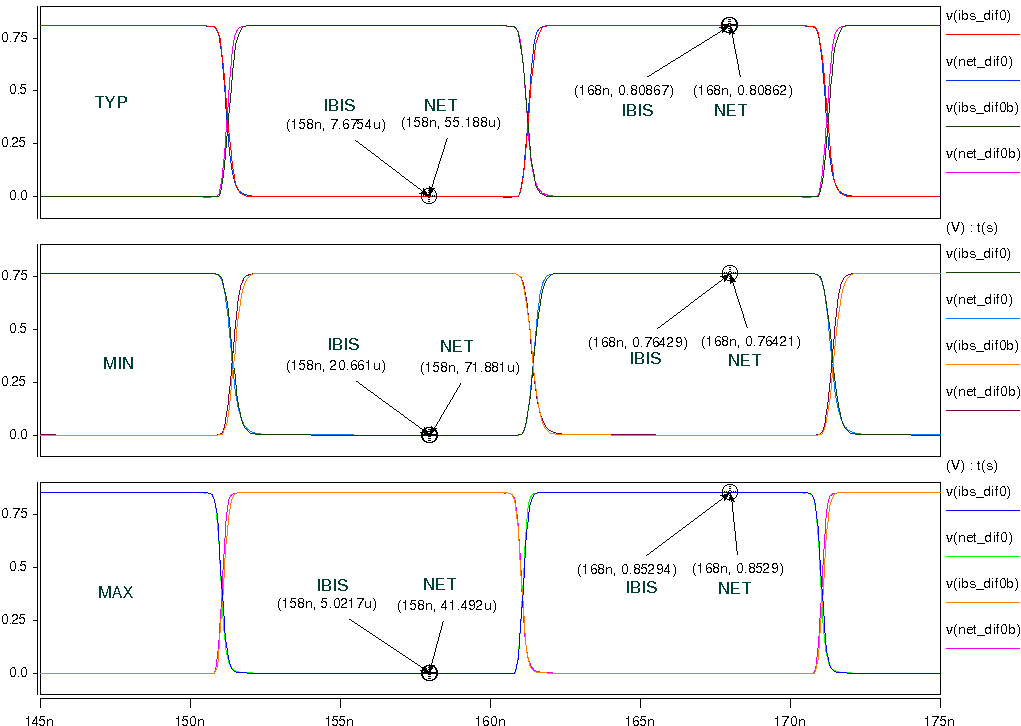
1. **HCSL\_0P8\_FAST**
2. Simulation **without** package data;



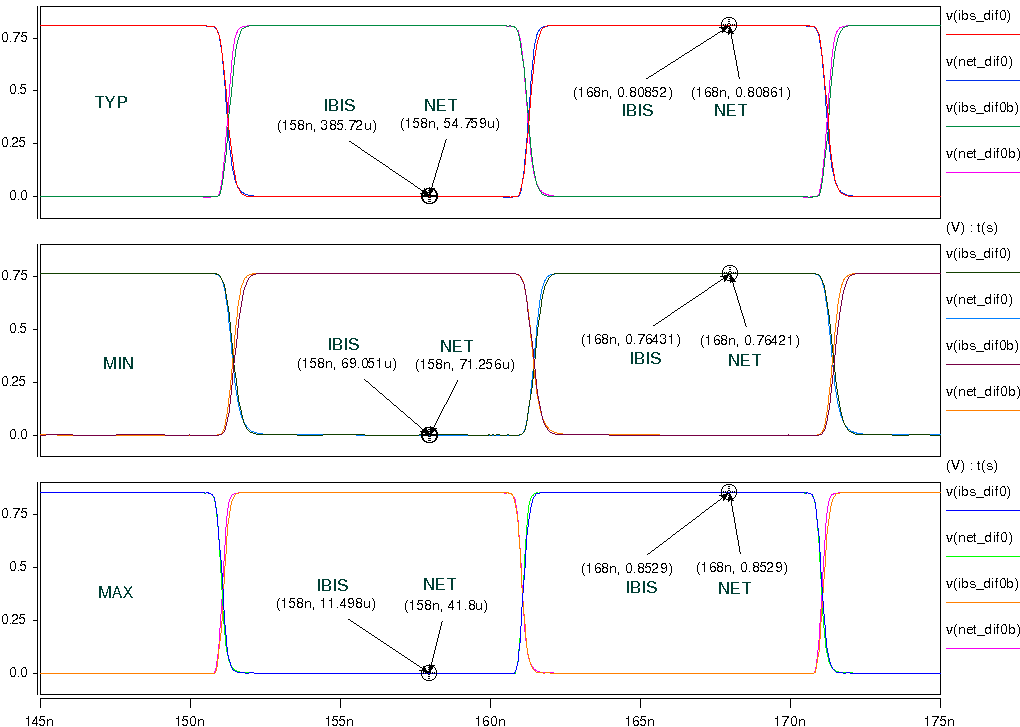
1. Simulation **with** package data.



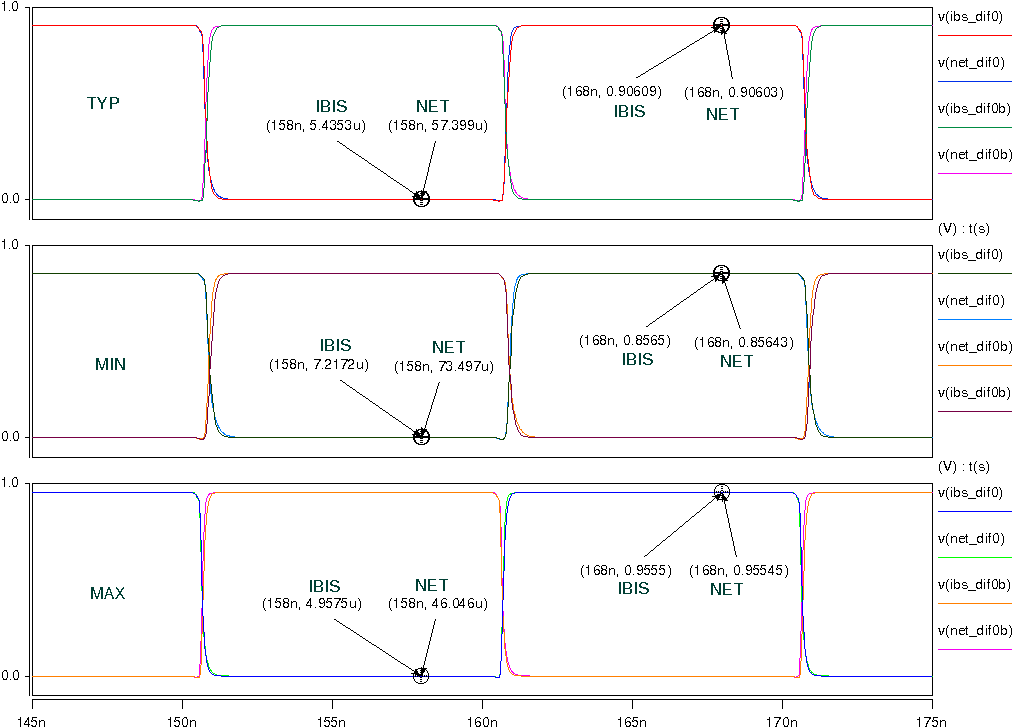
1. **HCSL\_0P8\_SLOW**
2. Simulation **without** package data;



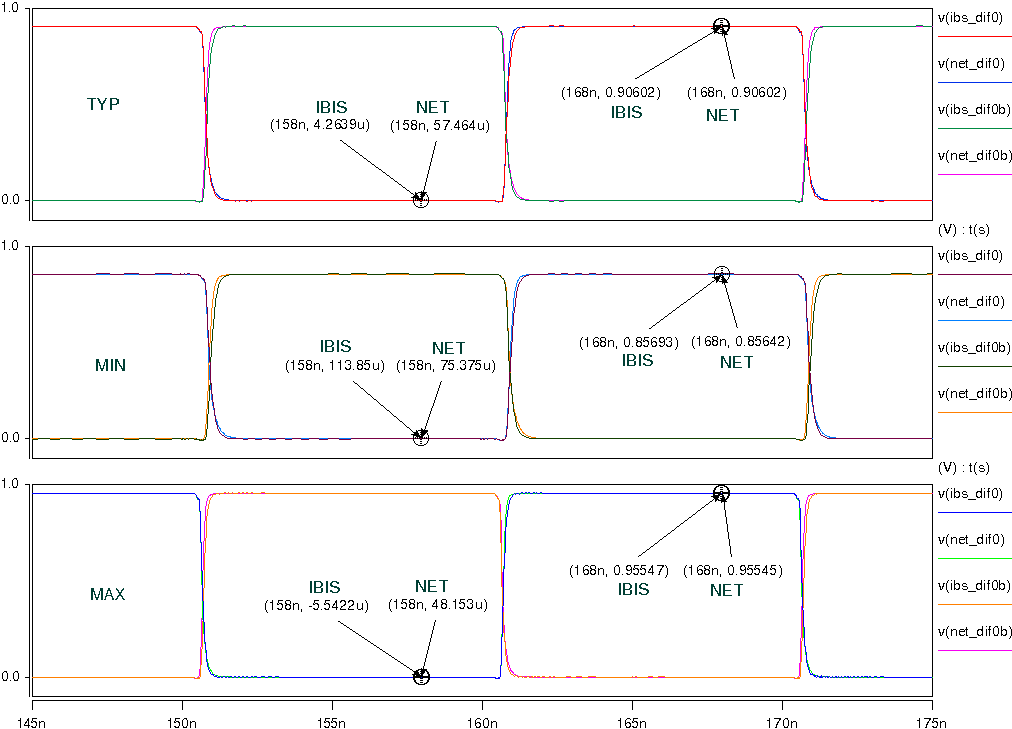
1. Simulation **with** package data.



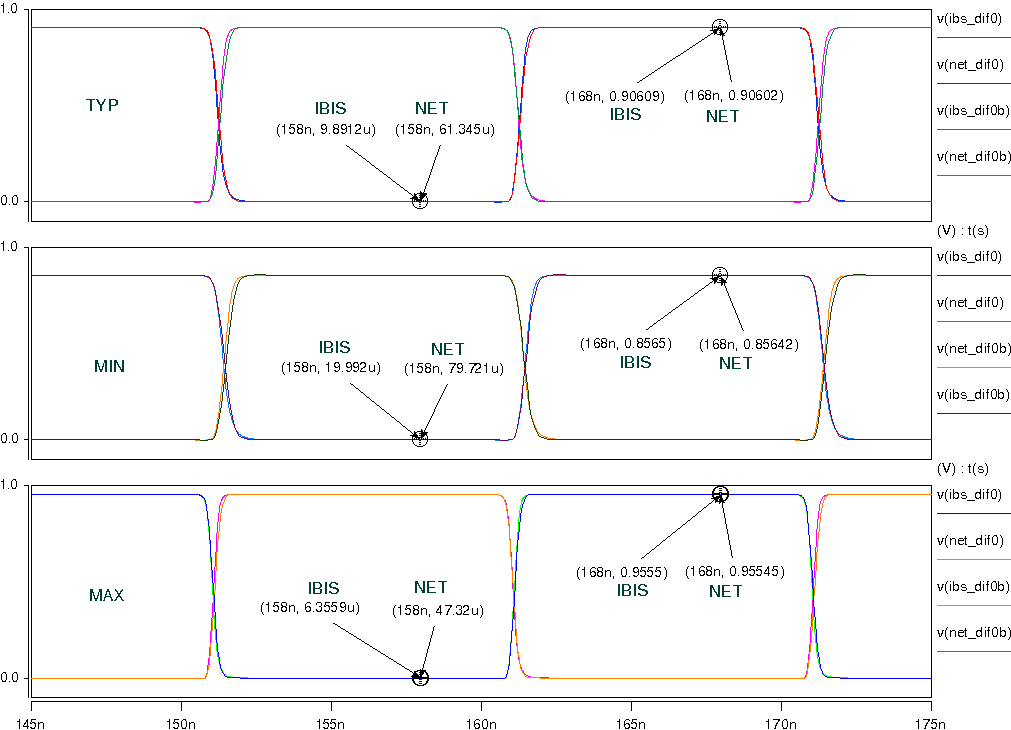
1. **HCSL\_0P9\_FAST**
2. Simulation **without** package data;



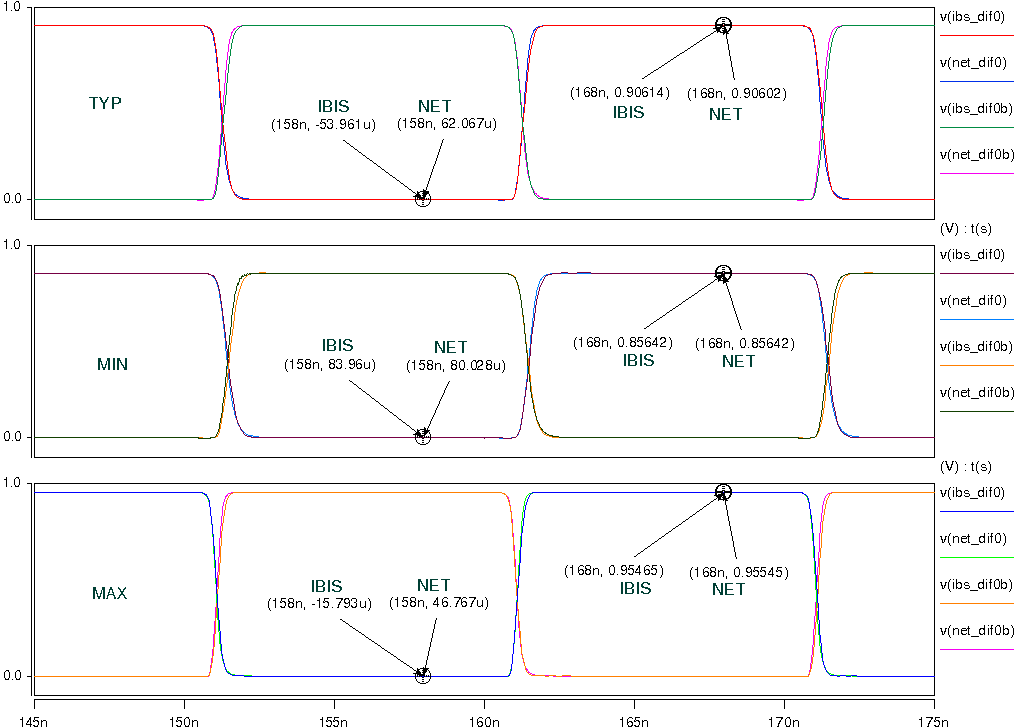
1. Simulation **with** package data.



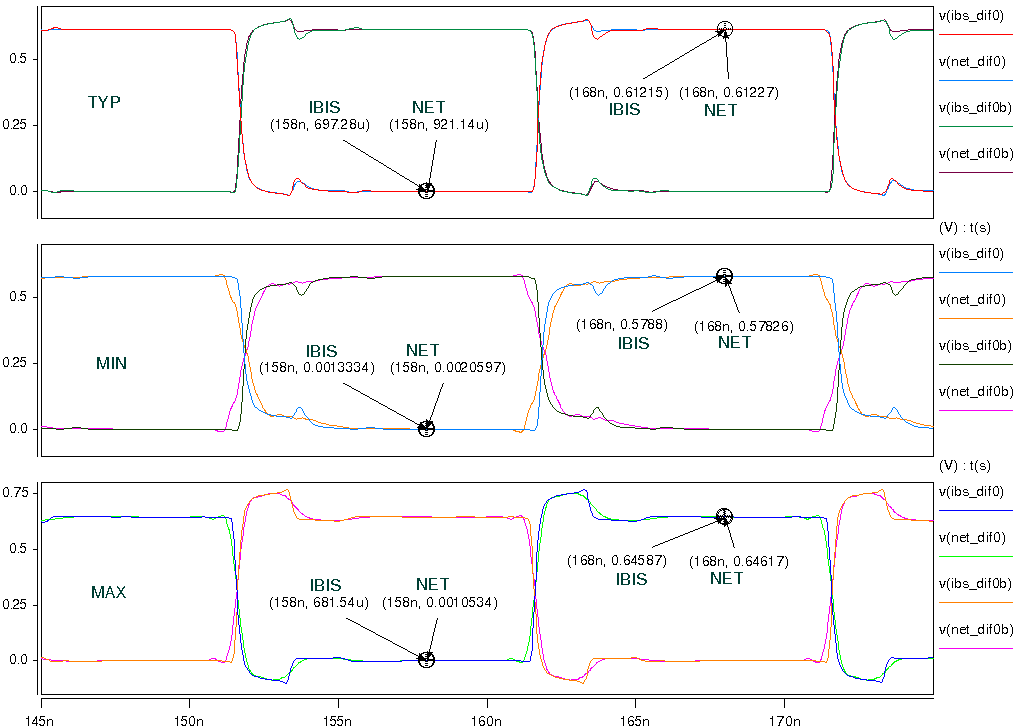
1. **HCSL\_0P9\_SLOW**
2. Simulation **without** package data;



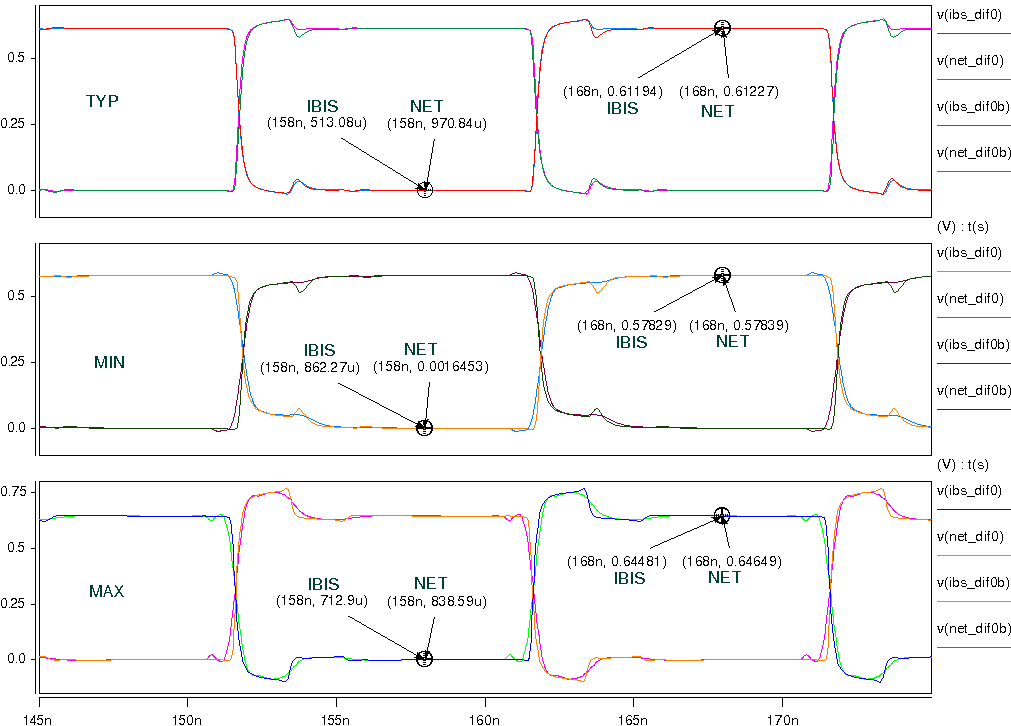
1. Simulation **with** package data.



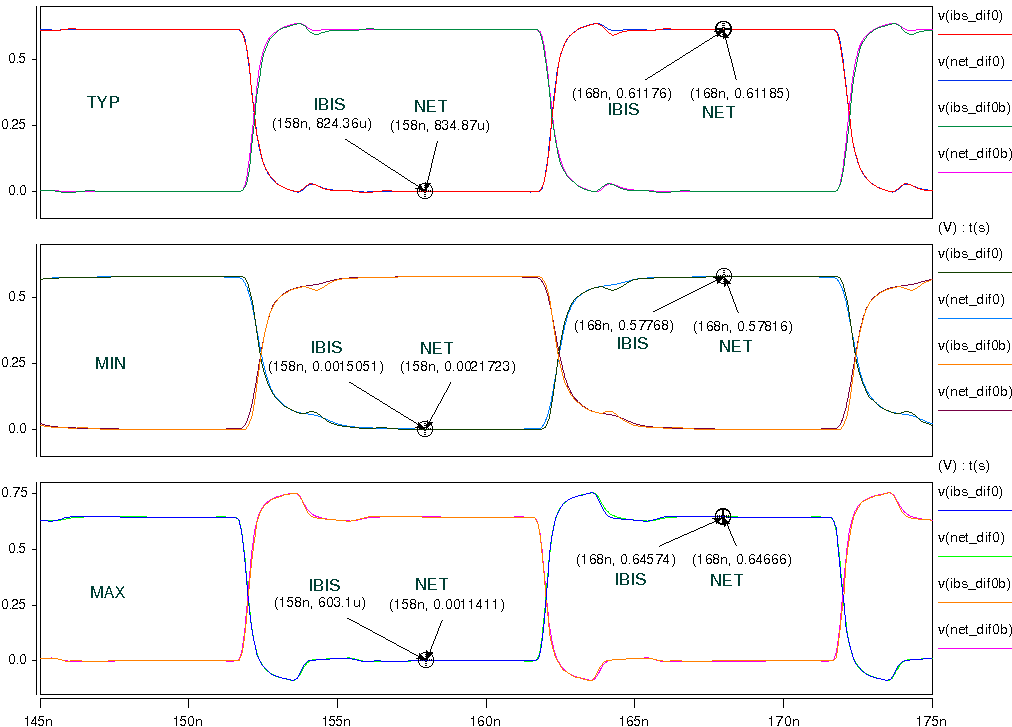
1. **With 5-inch trace and 2pF** **pulldown capacitance to the HCSL:**
2. **HCSL\_0P6\_FAST**
3. Simulation **without** package data;



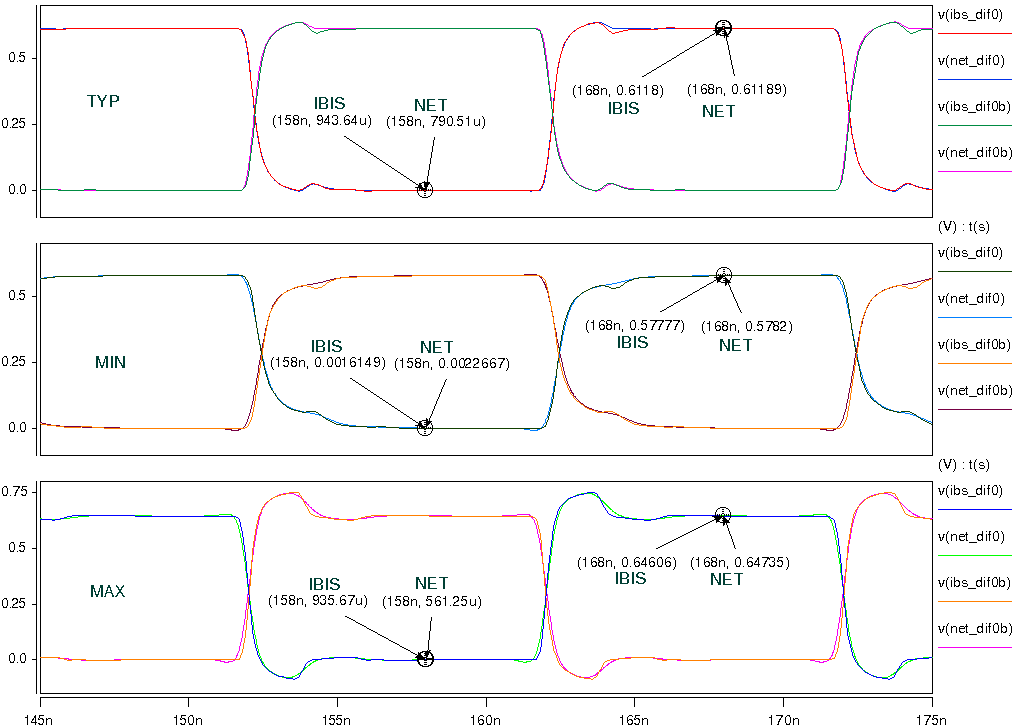
1. Simulation **with** package data.



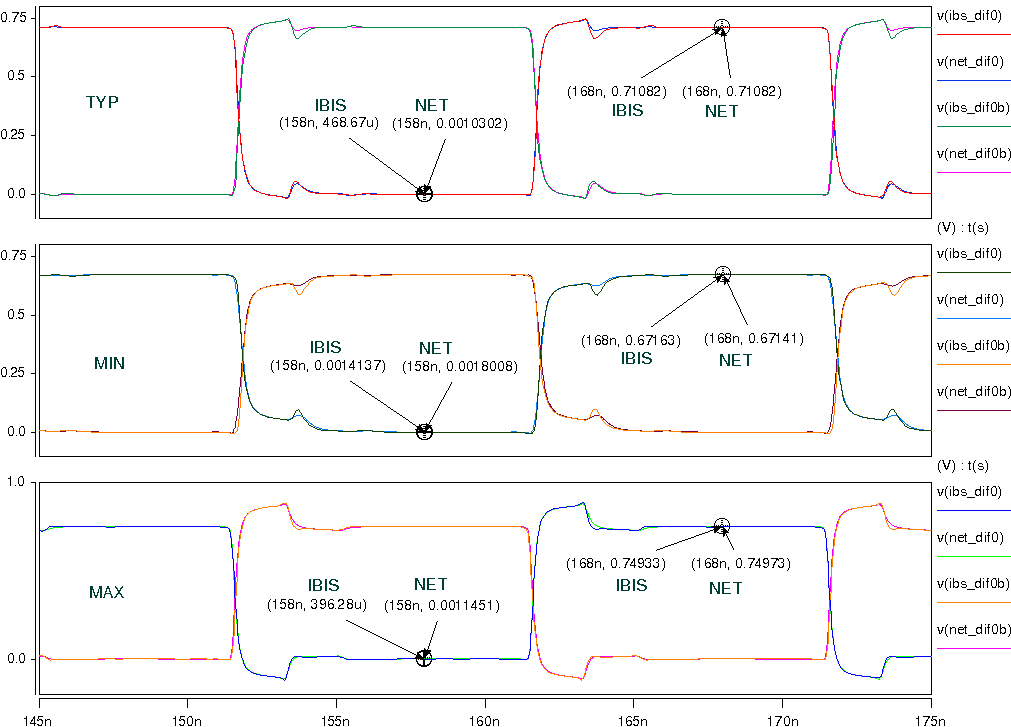
1. **HCSL\_0P6\_SLOW**
2. Simulation **without** package data;



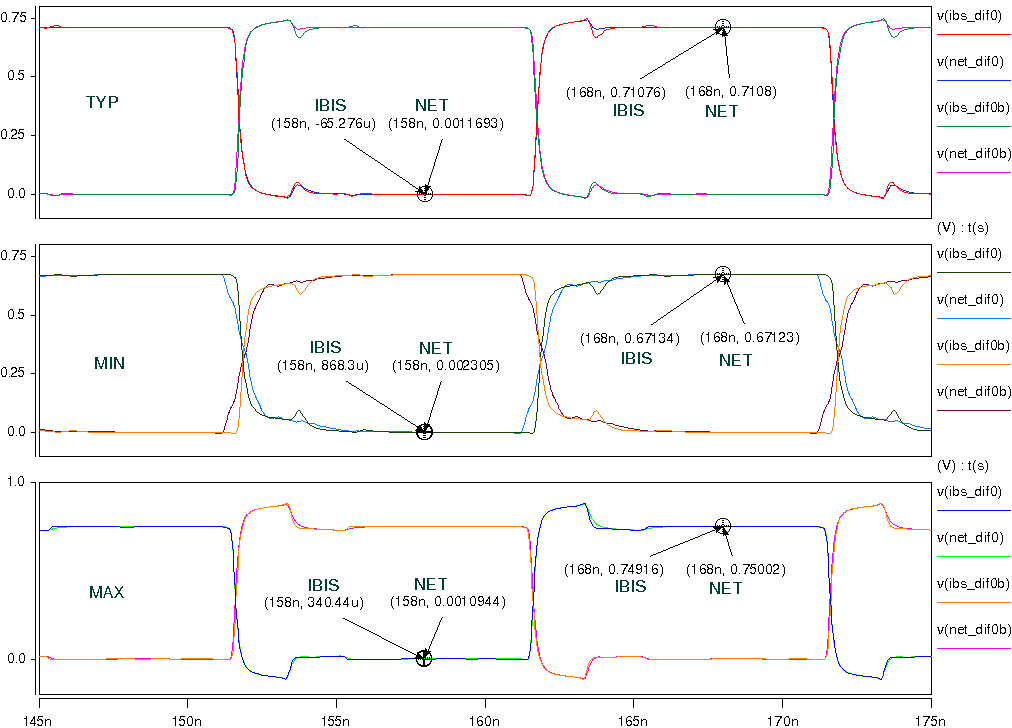
1. Simulation **with** package data.



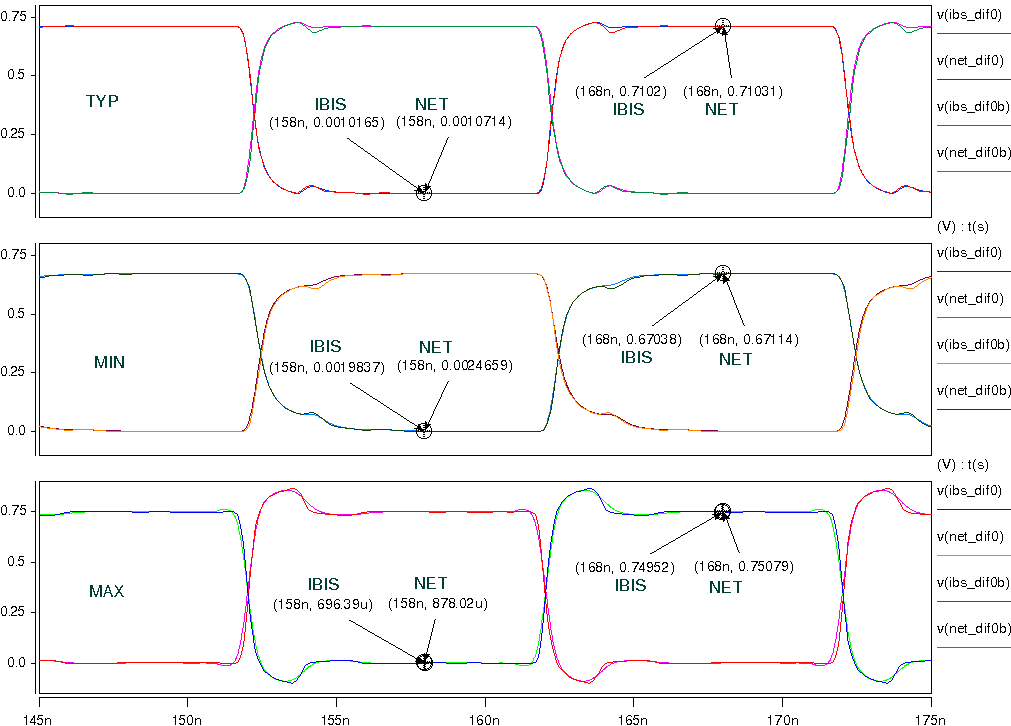
1. **HCSL\_0P7\_FAST**
2. Simulation **without** package data;



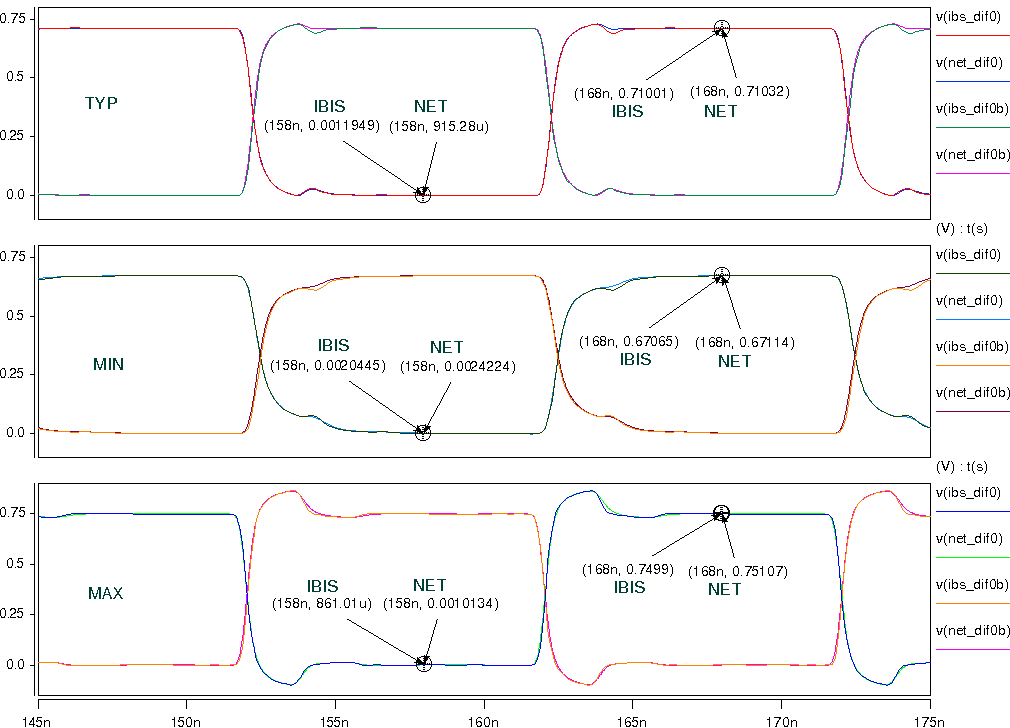
1. Simulation **with** package data.



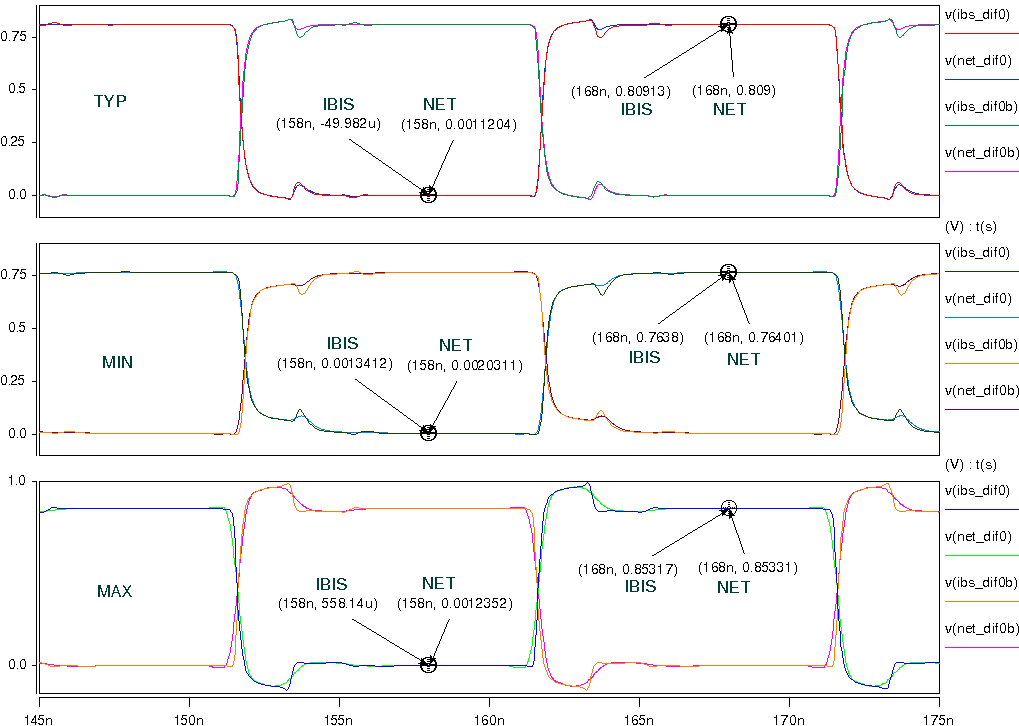
1. **HCSL\_0P7\_SLOW**
2. Simulation **without** package data;



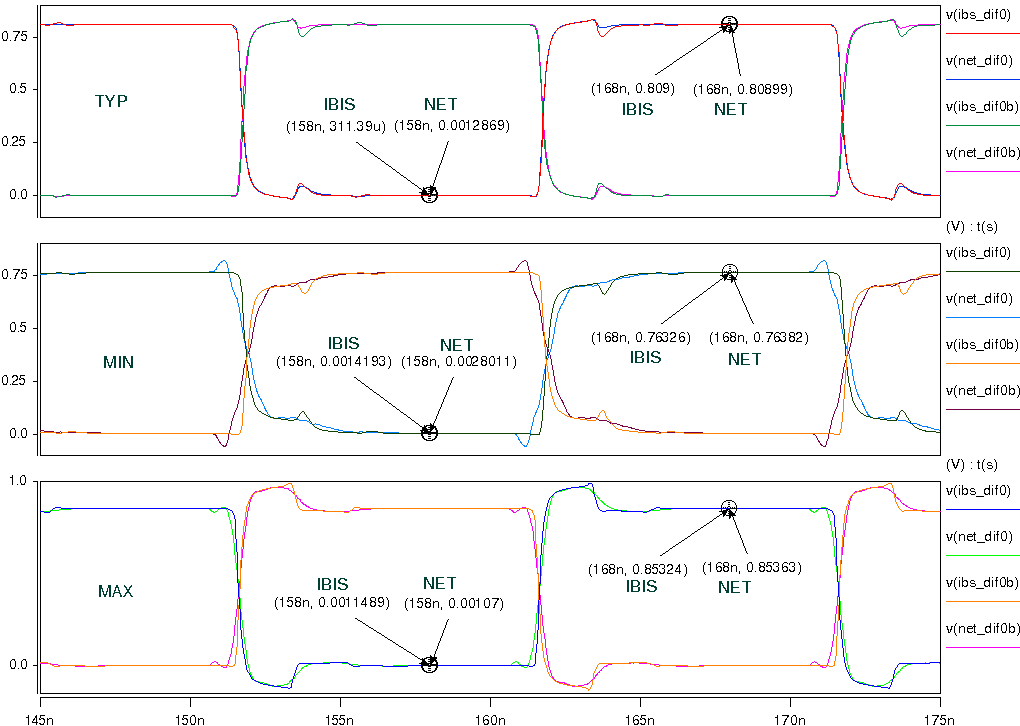
1. Simulation **with** package data.



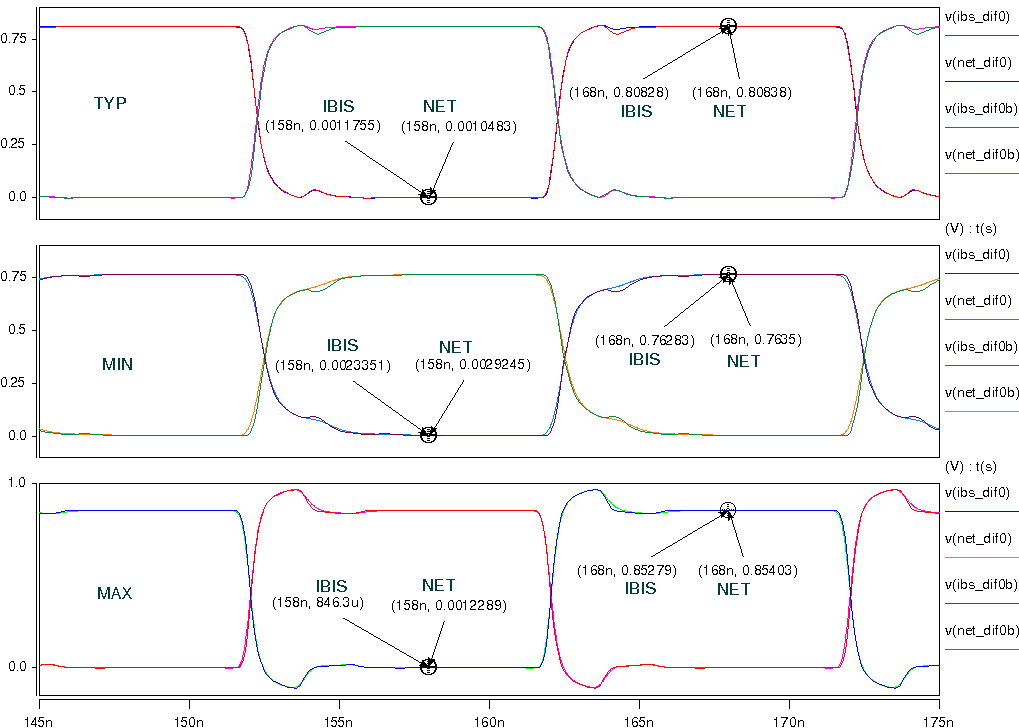
1. **HCSL\_0P8\_FAST**
2. Simulation **without** package data;



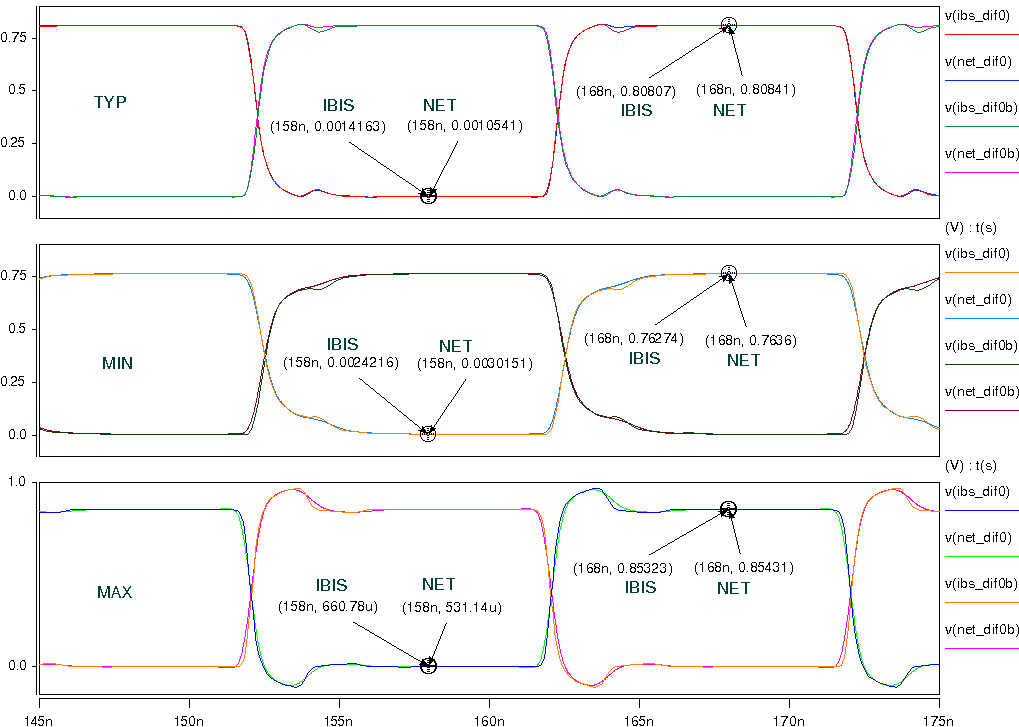
1. Simulation **with** package data.



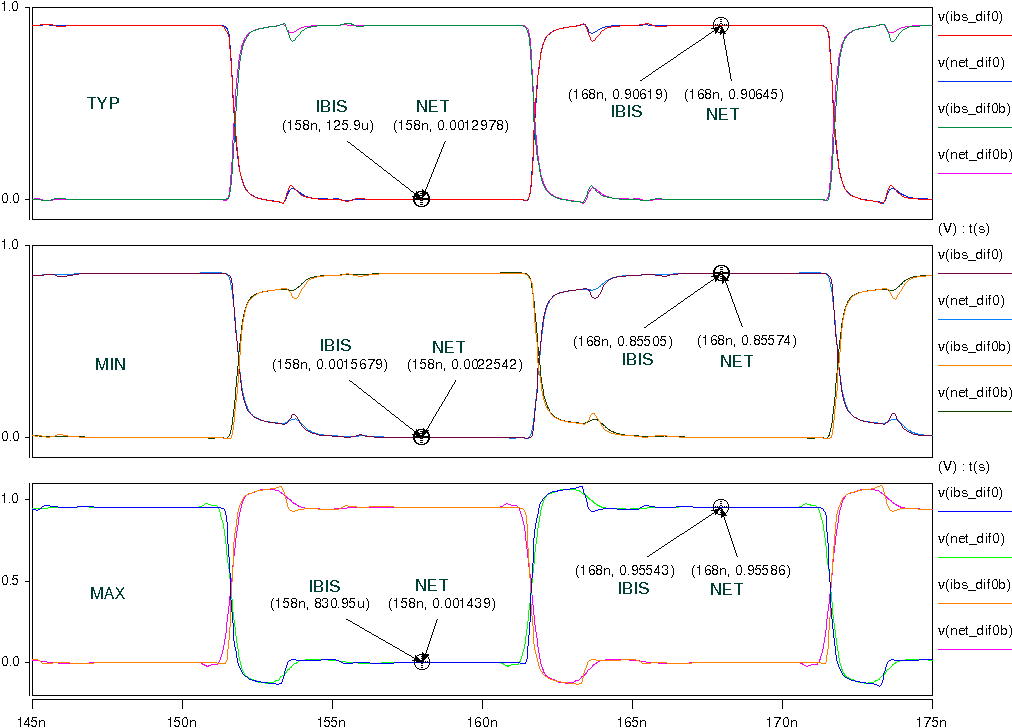
1. **HCSL\_0P8\_SLOW**
2. Simulation **without** package data;



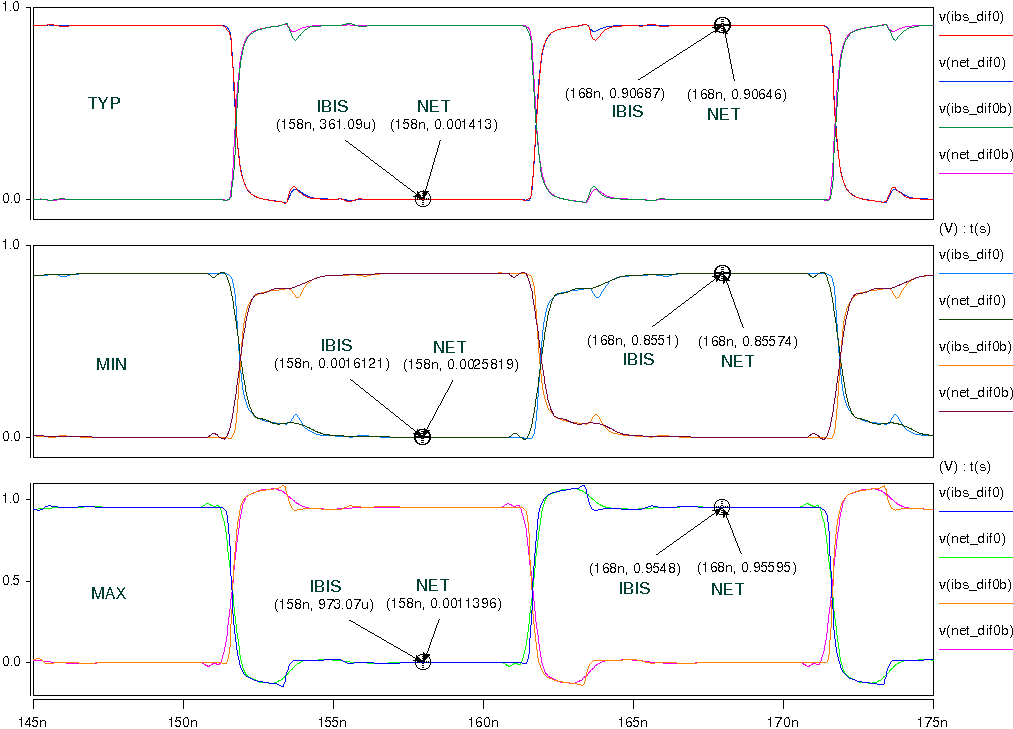
1. Simulation **with** package data.



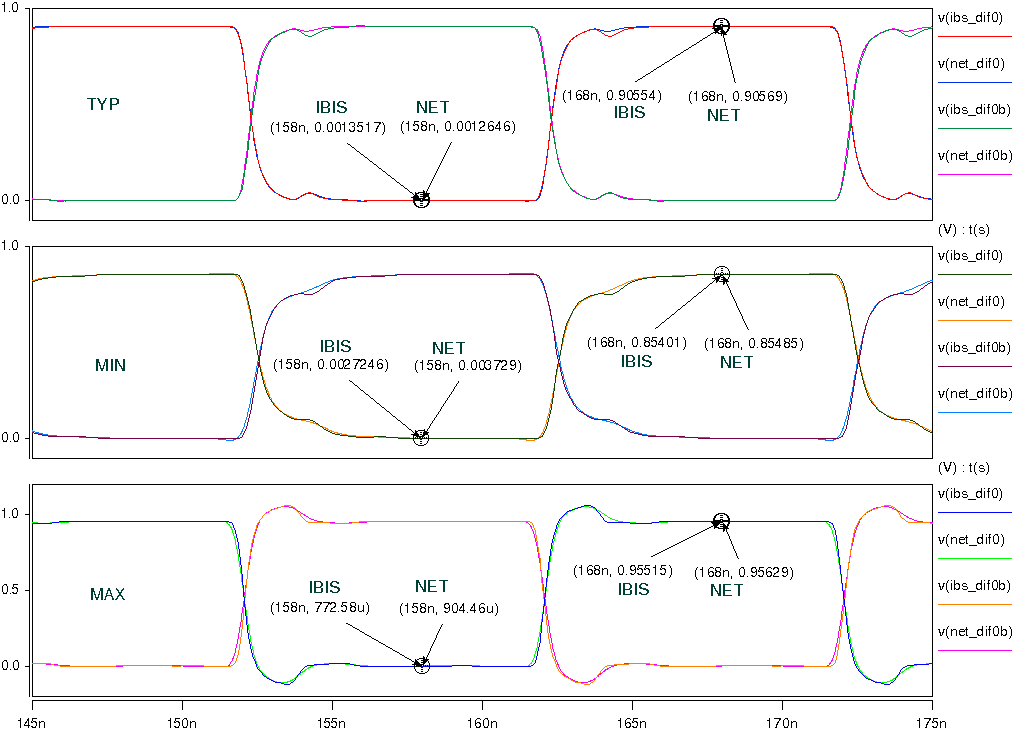
1. **HCSL\_0P9\_FAST**
2. Simulation **without** package data;



1. Simulation **with** package data.



1. **HCSL\_0P9\_SLOW**
2. Simulation **without** package data;



1. Simulation **with** package data.

