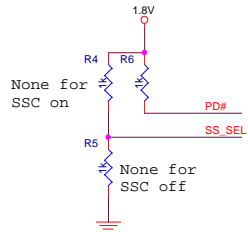
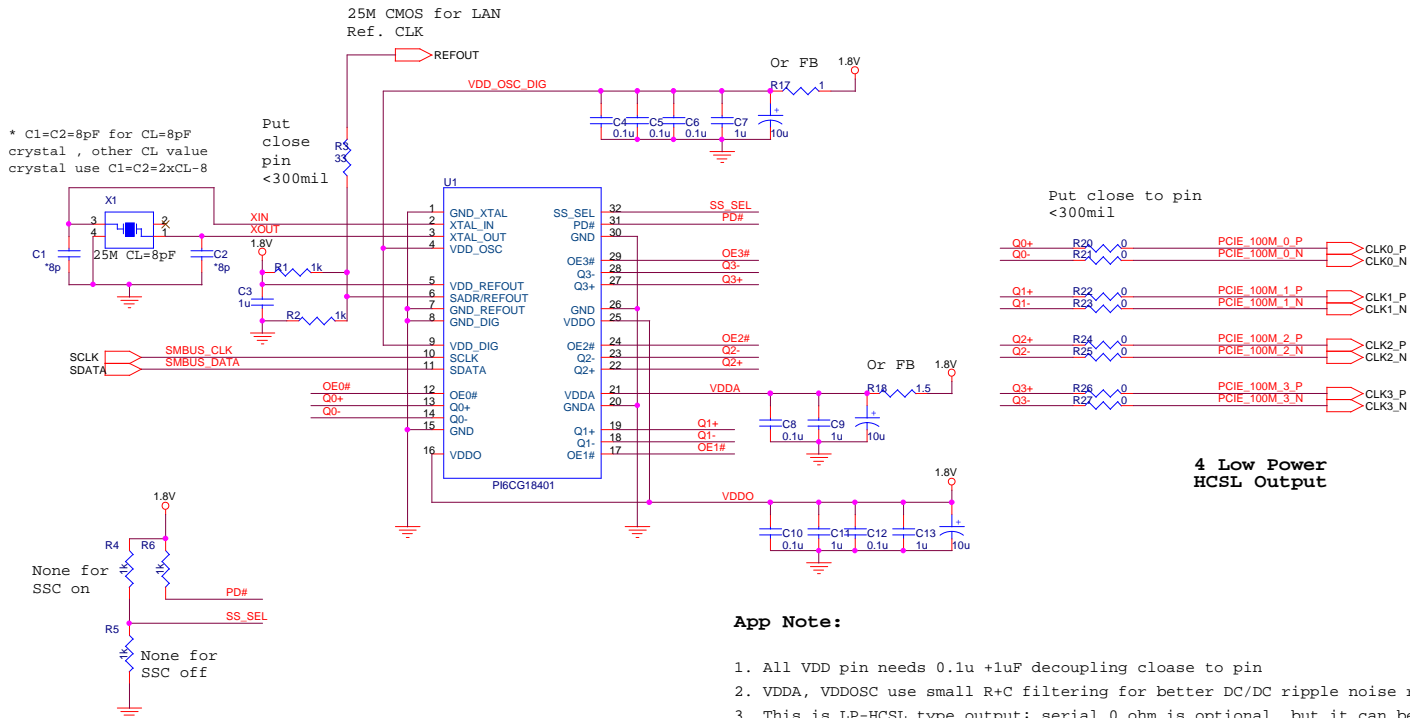


\* C1=C2=8pF for CL=8pF crystal, other CL value crystal use C1=C2=2xCL-8



**App Note:**

1. All VDD pin needs 0.1u +1uF decoupling cloase to pin
2. VDDA, VDDOSC use small R+C filtering for better DC/DC ripple noise rejection
3. This is LP-HCSL type output: serial 0 ohm is optional, but it can be replace in 2 to 5ohm for the optimal fine tune the board RX end waveform for different trace length if needed
4. Since OSC pin cap.=5pF so select CL=8pF crystal can C1=C2=8pF, other CL value crystal C1=C2=2xCL-5-3, 3 is PCB C\_stray pF
5. Note SSC\_EN and SMBUS address pins are power on latch once set;
6. Make LVDS clock, it needs AC coupling and then RX side use pull-up/down Rs to bias LVDS level, refer to datasheet;
7. OE# pins have internal pull-up, can be left open