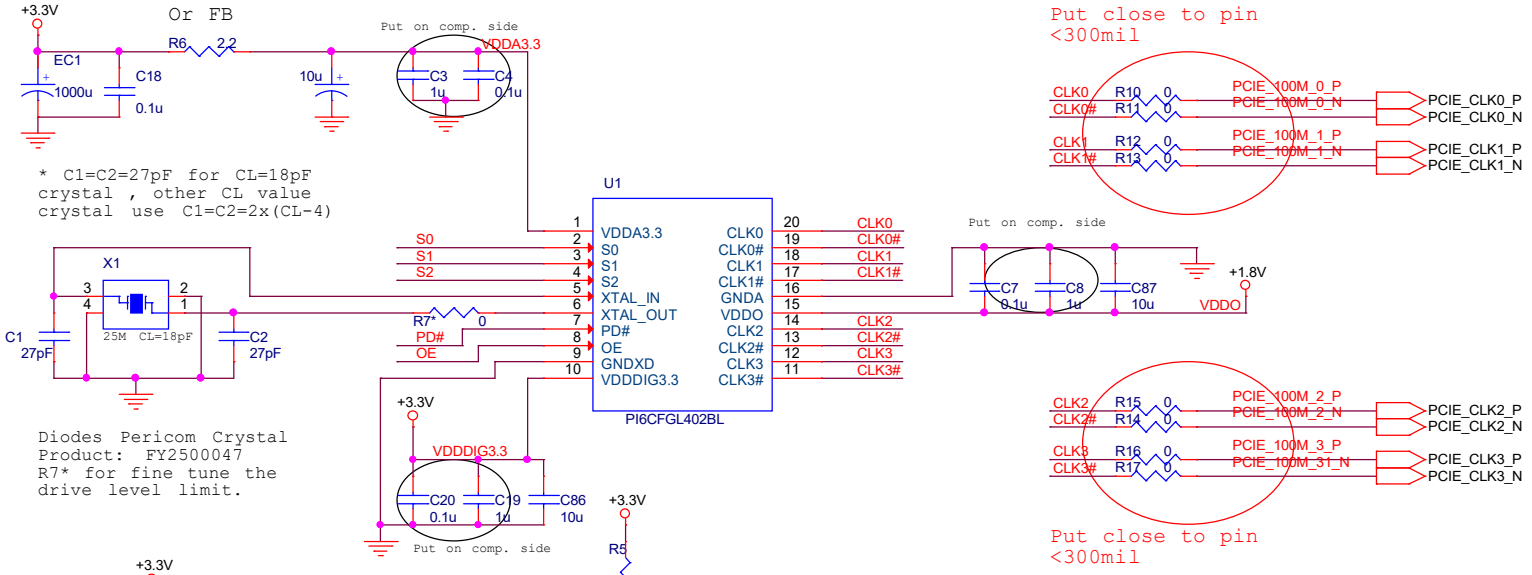

OE:
Set OE logic in R5/JP5 :
0: Disable
1: Enable

PD#
Set PD# logic in JP4.
0: Enable
1: Disable

App Note:

1. Each VDD pin needs 0.1u +1uF decoupling close to pin. (e.g.: VDDA, VDDO,...etc)
2. VDDA uses small R=1~2 ohm or FB(ferrite bead)+C=10uF filtering for better DC/DC ripple noise rejection
3. This is LP_HCSL type output: serial 0ohm R is optional, but it can be replace in 3 to 10 ohm for the optimal fine tune the board RX end waveform or different trace length if needed.

4. Leave un-used CLKx and /CLKx open

5. LVDS compatible output, refer to datasheet;

6. OE pin has internal pull-up, can be left open

S[2,1,0]
Set S0 logic in R1/JP1, S1 in R2/JP2, S2 in R3/JP3.

S2	S1	S0	SPREAD(%)	CLK(MHz)
0	0	0	-0.5	100
0	0	1	-1.0	100
0	1	0	-1.5	100
0	1	1	0.0	100
1	0	0	-0.5	200
1	0	1	-1.0	200
1	1	0	-1.5	200
1	1	1	0.0	200

Title: **PI6CFGL402B Application Schematic**

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