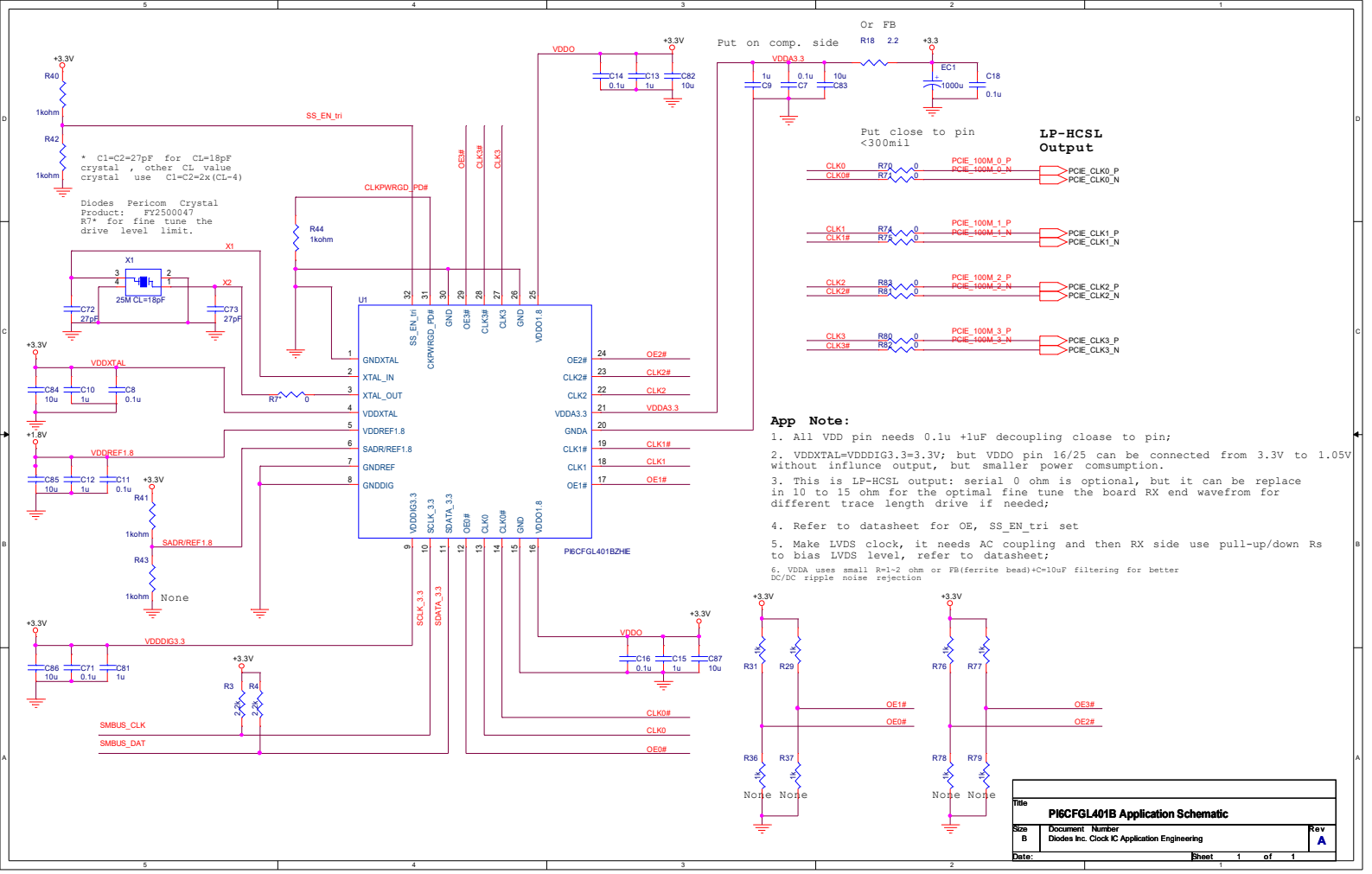

App Note:

1. All VDD pin needs 0.1u +1uF decoupling cloase to pin;
2. VDDXTAL=VDDDIG3.3=3.3V; but VDDO pin 16/25 can be connected from 3.3V to 1.05V without influnce output, but smaller power comsumption.
3. This is LP-HCSL output: serial 0 ohm is optional, but it can be replace in 10 to 15 ohm for the optimal fine tune the board RX end wavefrom for different trace length drive if needed;
4. Refer to datasheet for OE, SS_EN_tri set
5. Make LVDS clock, it needs AC coupling and then RX side use pull-up/down Rs to bias LVDS level, refer to datasheet;
6. VDDA uses small R=1~2 ohm or FB(ferrite bead)+C=10uF filtering for better DC/DC ripple noise rejection

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