**Verification of PI6CFGL201B IBIS model**

1. **Introduction:**

To verify the correlation between the ibis model and hspice model, we need to do some simulations:

The frequency of signal is **100MHz**:

Vvin vin 0 pulse( 3.3 0 4u 0.1n 0.1n 4.9n 10n )

Add a **50Ω** resistance between signals and INPUT, with Add **50Ω** pull-down resistor and **4pF** pull-down capacitance to the OUTPUT：

1. **Add 2pF pull-down capacitance to the Output:**

PI6CFGL201B

**OUT**

**SCL\_C**

**SDA\_C**

C

**Input Signals**

**SCL\_C**

**SDA\_C**

**Output**

**SCL\_C**

**SDA\_C**

**VIN**

**SCL\_C**

**SDA\_C**

1. without package;
2. with package.
3. **Add 50 Ohm pull-up resistor to the IO:**

PI6CFGL201B

**OUT**

**SCL\_C**

**SDA\_C**

**Input Signals**

**SCL\_C**

**SDA\_C**

**VIN**

**SCL\_C**

**SDA\_C**

SDA\_IO

**SCL\_C**

**SDA\_C**

SDA\_IN

**SCL\_C**

**SDA\_C**

**…..**

**SCL\_C**

**SDA\_C**

3.3V

**SCL\_C**

**SDA\_C**

R=50Ohm

**SCL\_C**

**SDA\_C**

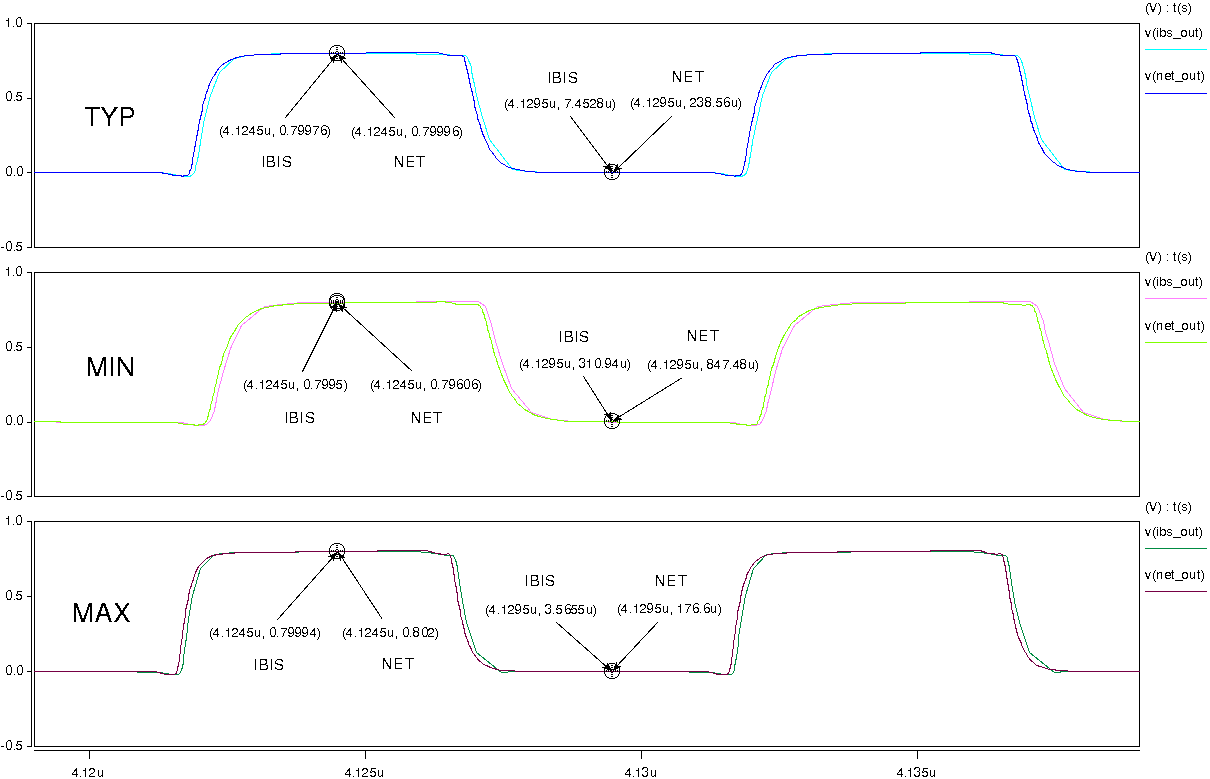
**IO**

**SCL\_C**

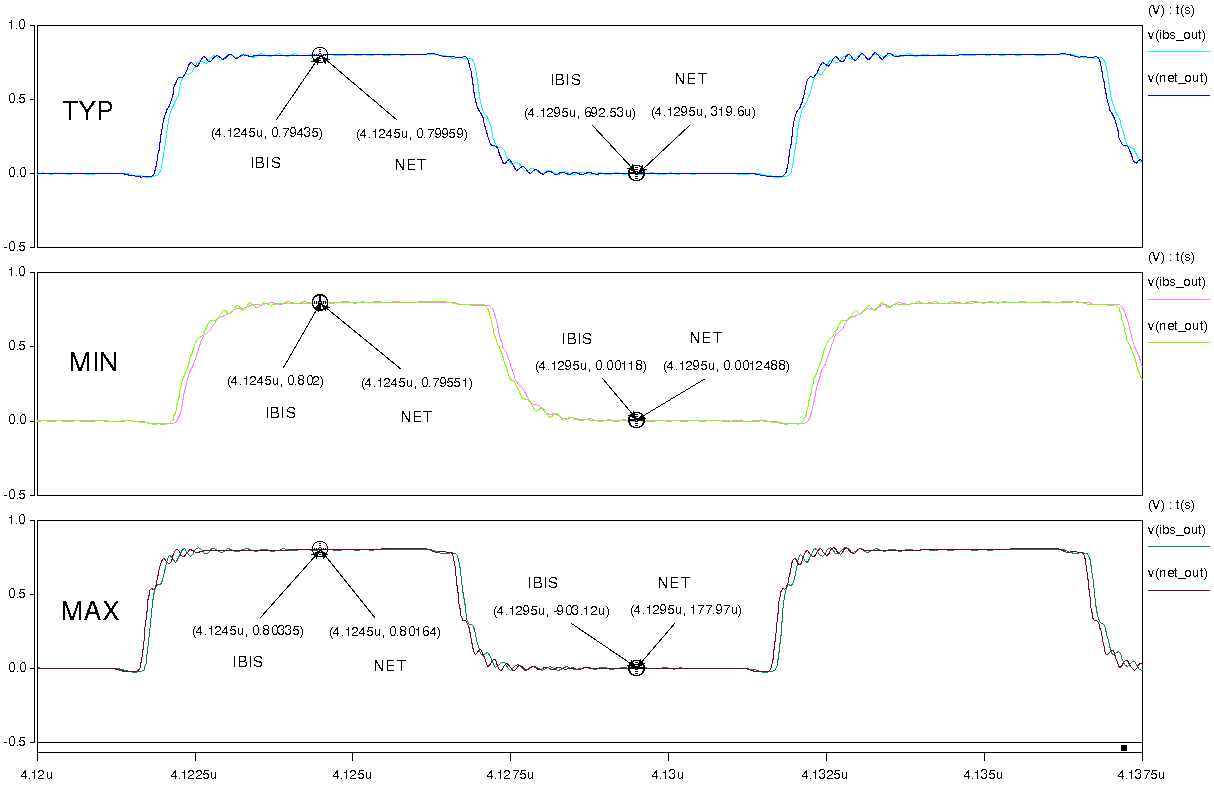
**SDA\_C**

1. **Conclusion:**
2. For OUTPUT, the simulation results of IBIS model can match very well with the HSPICE model at different load conditions;
3. For IO, the simulation results of IBIS model can match very well with the HSPICE model at different load conditions.

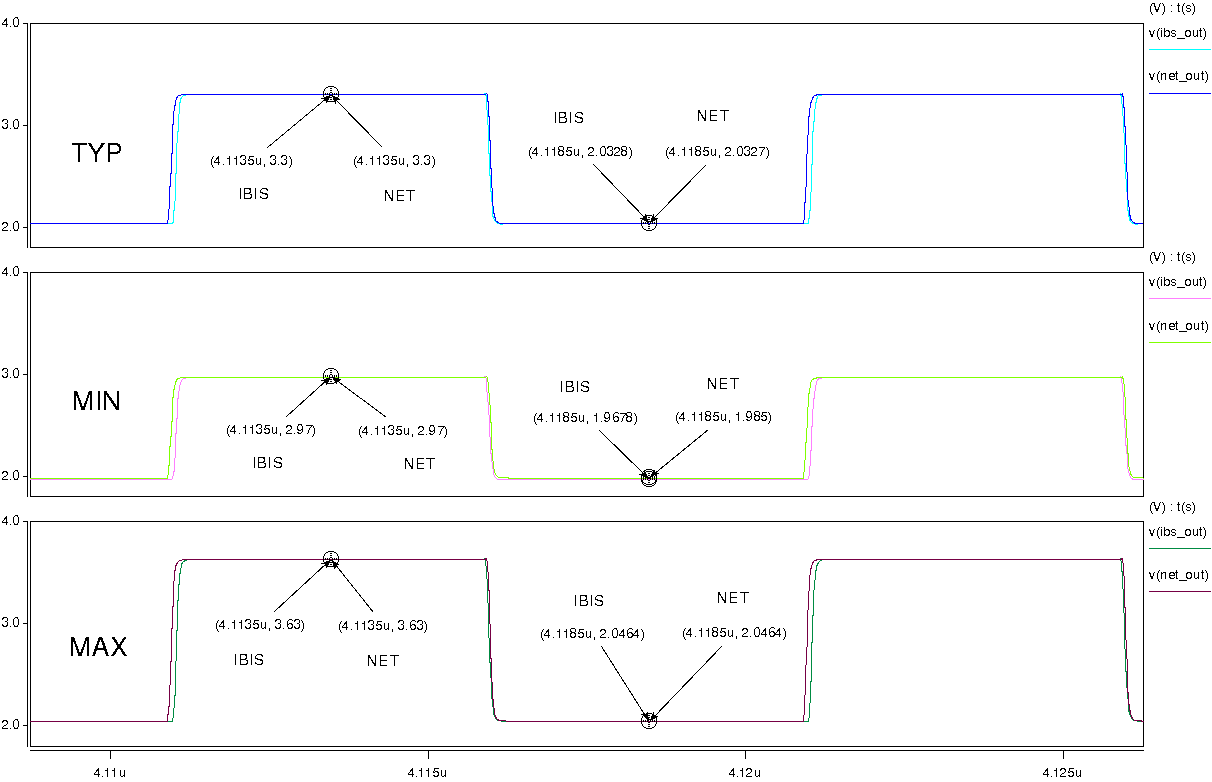
1. **Simulation Result:**
2. **OUTPUT**
3. without package;



1. with package.



1. **IO**
2. without package;



1. with package;

