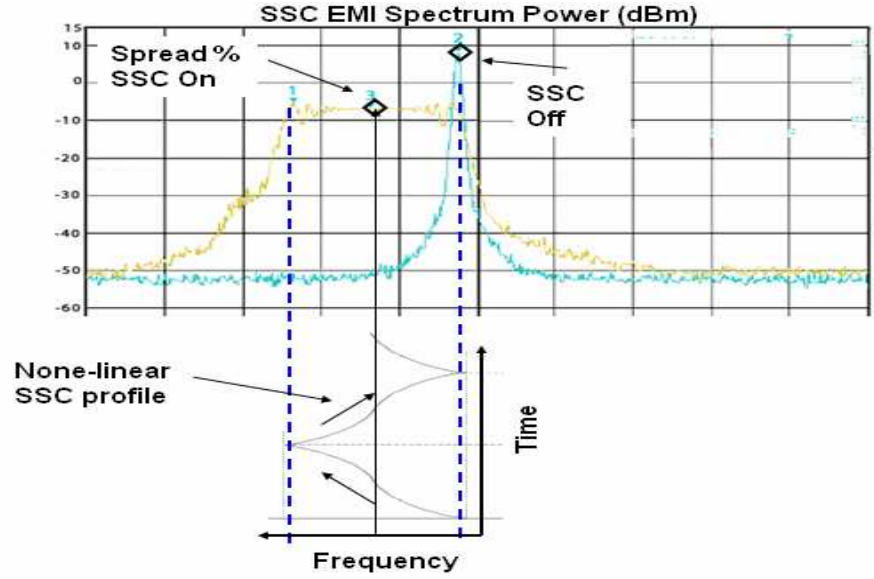
SSC Clock In PCIe ZDB Application

Pericom Application Engineering

1) Spread Spectrum Clock

To reduce system EMI, it needs SSC (Spread Spectrum Clock) to reduce EMI emission energy. The best SSC profile is "Hershey Kiss" profile which is non-linear triangle shape in about 33kHz, that has the highest efficiency of EMI energy reduction dB vs. SSC spread %. On the other hand, it takes wider frequency bandwidth to keep its non-linear shape during frequency spreading, as the following diagram.



2) SSC Need ZDB Set in H_BW

In clock buffer application, there are two kinds: i) None PLL one; ii) PLL ZDB (Zero Delay Buffer); the PLL one has advantages of zero delay and re-time in shape of output clock. For example, if the input clock is 40% dutycycle, the ZDB output will keep 50% output dutycycle. PCIe clock ZDB has PLL BW setting to adapt the SSC pass through, which depends on the applications. The wider H_BW has easy pass of SSC with less instant tracking delay and easy to keep the SSC profile shape without distortion on considering device process variation. The most SSC applications are suggested to use H_BW. The L_BW is for smaller SSC spread % and none SSC clock, this way can take L_BW advantage to filter out some input clock jitter, as the following diagram shows.

How much BW is enough? For linear triangle SSC profile, min. BW => 6x33kHz= 198kHz; For the none-linear SSC profile, mini. BW=> 8x33kHz=264kHz as an example. Of course, wider spread% SSC needs more wider BW too.