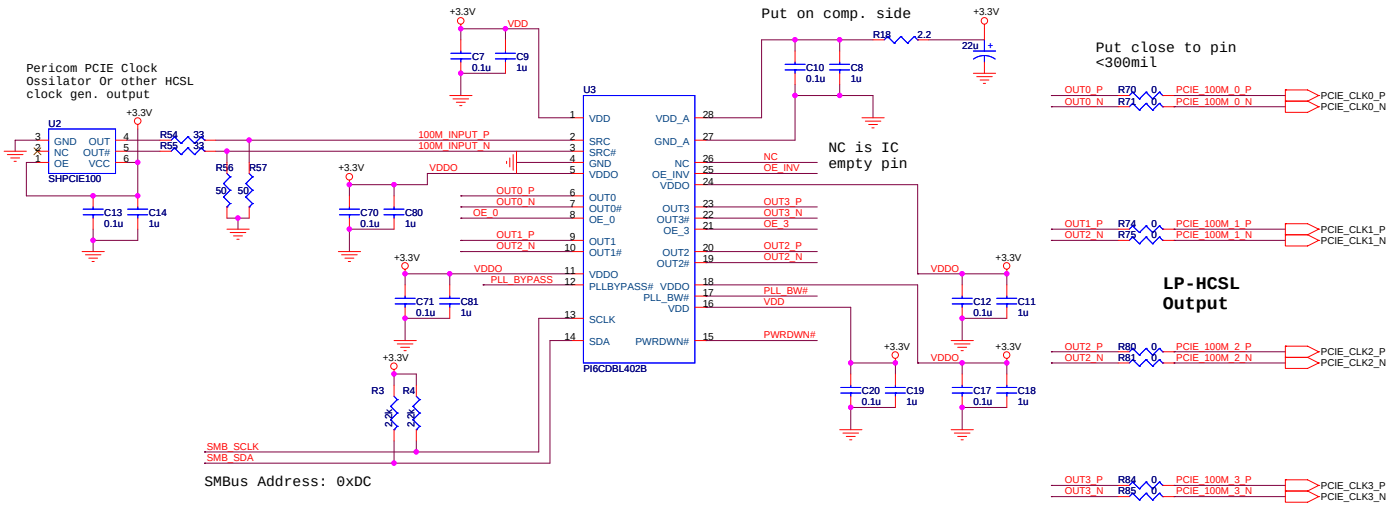

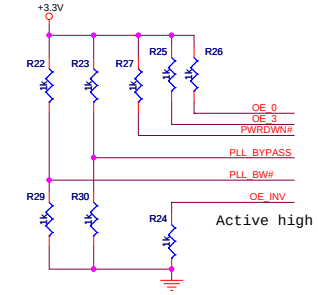

App Note:

1. All VDD pin needs 0.1u +1uF decoupling cloase to pin;
2. VDDA=VDD=3.3V; but VDDO pin 5/11/18/24 can be connected from 3.3V to 1.8V without influnce output, but smaller power comsumption.
3. This is LP-HCSL output: serial 0 ohm is optional, but it can be replace in 10 to 15 ohm for the optimal fine tune the board RX end wavefrom for different trace length drive if needed;
4. Refer to datasheet for OE, PLL_BYPASS, PLL_BW# set;
5. Make LVDS clock, it needs AC coupling and then RX side use pull-up/down Rs to bias LVDS level, refer to datasheet;

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