PI6CDBL401B(TQFN) Application Information

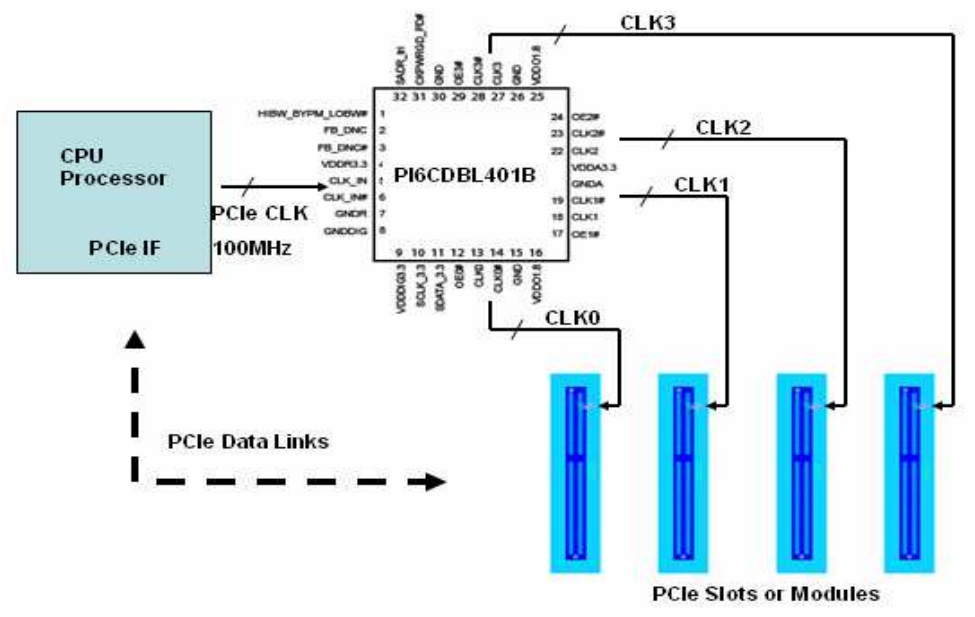
Pericom Application Engineering

1. Introduction

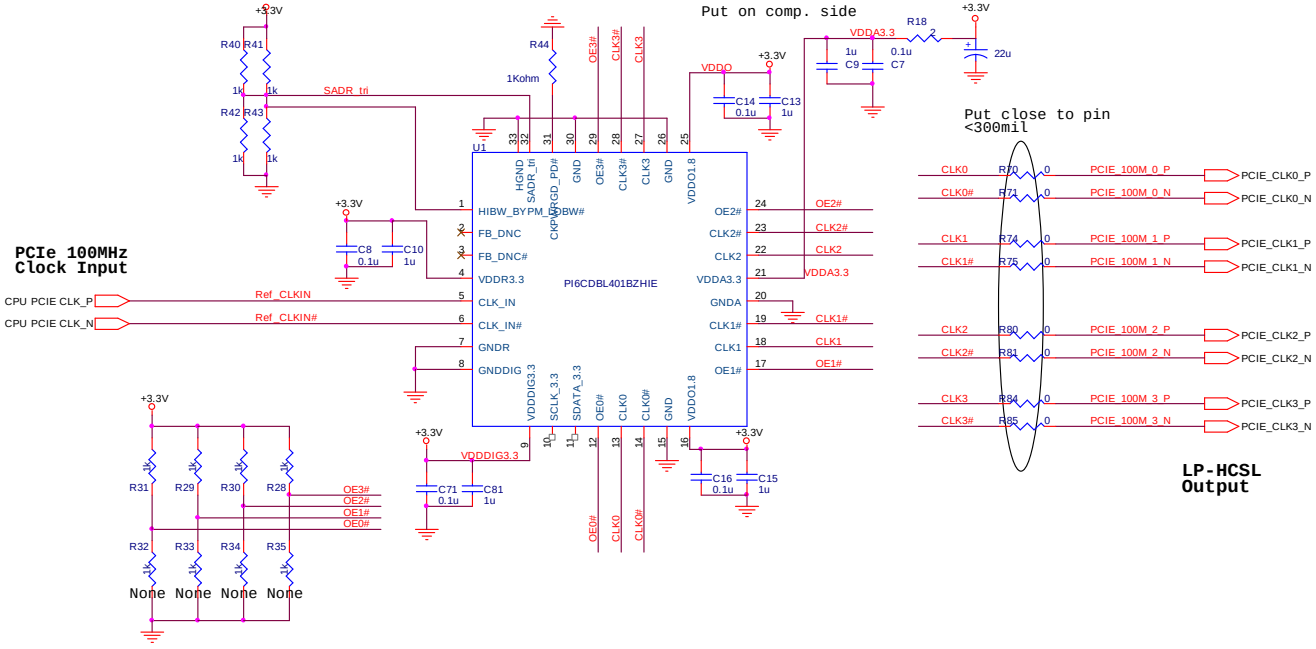
PI6CDBL401B is PCIe ZDB x4 output for PCIe gen. 1.0, 2.0, 3.0 100MHz reference clock designs. It has small package in TQFN 32 pin. Its core supply is 3.3V, but its separate VDDO can be 3.3V to 1.8V for more power saving in lower supply.

This device Low Power HCSL (LP-HCSL) output does not need 50ohm pull-down for near source termination to save power going to GND. Its other package TSSOP 28pin is LP-HCSL ZDB in x4 output as PI6C20400A/B socket compatible.

2. PCIe ZDB Application Diagram:



3. Application Schematic

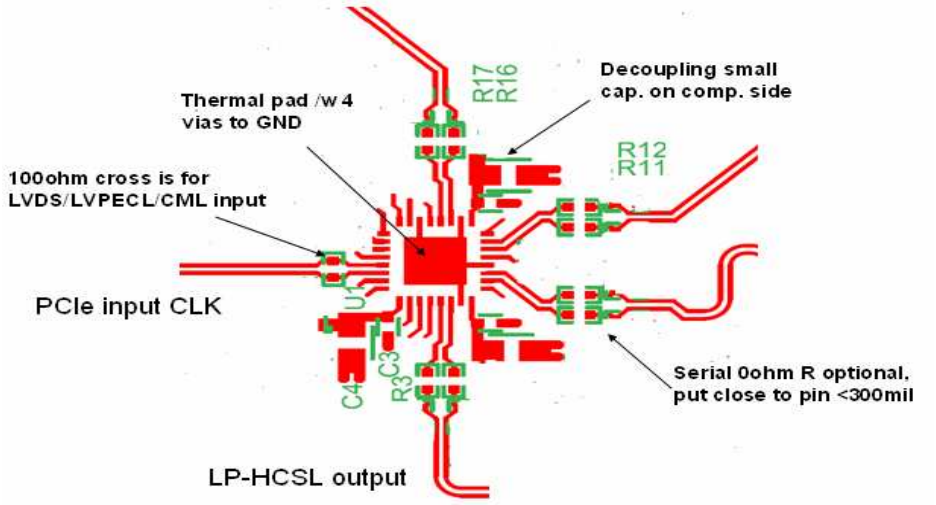


4. PCB Application Note

1 Input clock use DC coupling HCSL 100MHz; If use LVDS/LVPECL input, then add 100ohm cross at input pins;
2 LP-HCSL serial 0 ohm is optional for later on different trace fine tune RX waveform if needed;
3 Put each VDD 0.1uF+1uF close to pin, make all GNDs in one solid GND plane;
4 VDDA use serial 2 ohm to form RC filter for better low frequency (<1MHz) noise filtering;
5 Leave un-used CLKx just simplely open;
6 This part is SSC compatible and select pin 1 BW control in L_BW for better input clock jitter filtering;
7 LP-HCSL transfer to LVDS drive needs AC coupling with pull-up/down at RX side, refer to datasheet;

5. PCB Layout Example:

The following is PCB layout example with guide note. HCSL PCIe input clock does not need 100ohm cross at the inputs pins.



6. Better LVDS RX Termination

General LVDS receiver has wide RX common mode voltage range, about 1.25V +/-1V. So we can use simpler LVDS RX termination to save DC bias power by use 10k ohm with easier layout. For example, VDD=3.3V will get V_cm=1.65V; VDD=2.5V will get V_cm=1.25V.