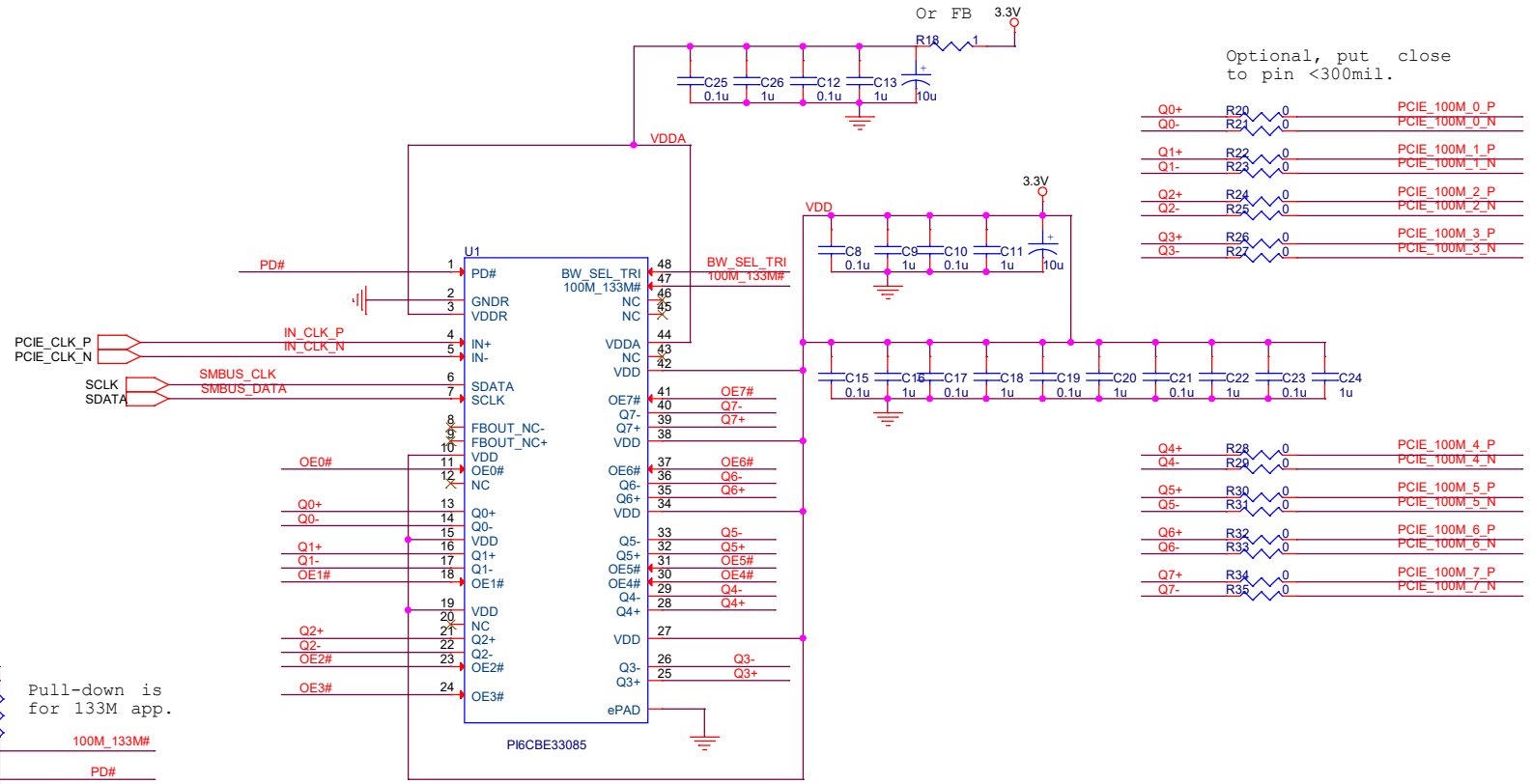

100M_133M#:

Set "0" for 133.33MHz app.
Set "1" for 100MHz app.

BW_SEL_TRI:

Set PLL BW logic in R4/R5

"0"=L_BW,"M"=Bypass,"1"=H_BW

OE0#

Make individual OEx# pull-up/down to enable/disable each output

.
.
.

OE7#

App Note:

1. Each VDD pin needs 0.1u +1uF decoupling close to pin. (e.g.: VDD, VDDA, VDDR...etc)
2. VDDA use small R=1~2 ohm or FB(ferrite bead)+C=10uF filtering for better DC/DC ripple noise rejection
3. This is LP_HCSL type output: serial 0ohm R is optional, but it can be replace in 3 to 10 ohm for the optimal fine tune the board RX end waveform or different trace length if needed
4. OEx# pins have internal pull-down
5. Connect e_Pad in 6 to 8 vias to GND plane
6. To Make LVDS output clock, it needs AC coupling and then RX side use pull-up/down Rs to bias in LVDS level, refer to datasheet;
7. Note, BW_SEL_TRI pin is power on latch once set

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