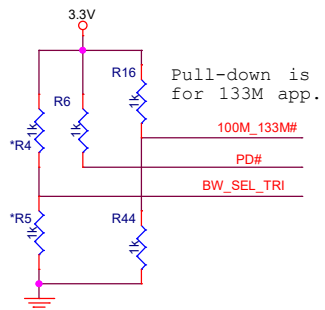


Optional, put close to pin <300mil.

Q0+	R20	0	PCIE_100M_0_P
Q0-	R21	0	PCIE_100M_0_N
Q1+	R22	0	PCIE_100M_1_P
Q1-	R23	0	PCIE_100M_1_N
Q2+	R24	0	PCIE_100M_2_P
Q2-	R25	0	PCIE_100M_2_N
Q3+	R26	0	PCIE_100M_3_P
Q3-	R27	0	PCIE_100M_3_N
Q4+	R28	0	PCIE_100M_4_P
Q4-	R29	0	PCIE_100M_4_N
Q5+	R30	0	PCIE_100M_5_P
Q5-	R31	0	PCIE_100M_5_N
Q6+	R32	0	PCIE_100M_6_P
Q6-	R33	0	PCIE_100M_6_N
Q7+	R34	0	PCIE_100M_7_P
Q7-	R35	0	PCIE_100M_7_N



**100M\_133M#:**

Set "0" for 133.33MHz app.  
Set "1" for 100MHz app.

**BW\_SEL\_TRI:**

Set PLL BW logic in R4/R5  
"0"=L\_BW, "M"=Bypass, "1"=H\_BW

**OE0#**

Make individual OEx# pull-up/down to enable/disable each output

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. .  
. . .

**OE7#**

**App Note:**

1. Each VDD pin needs 0.1u +1uF decoupling close to pin. (e.g.: VDD, VDDA, VDDR...etc)
2. VDDA use small R=1~2 ohm or FB(ferrite bead)+C=10uF filtering for better DC/DC ripple noise rejection
3. This is LP\_HCSL type output: serial 0ohm R is optional, but it can be replace in 3 to 10 ohm for the optimal fine tune the board RX end waveform or different trace length if needed
4. OEx# pins have internal pull-down
5. Connect e\_Pad in 6 to 8 vias to GND plane
6. To Make LVDS output clock, it needs AC coupling and then RX side use pull-up/down Rs to bias in LVDS level, refer to datasheet;
7. Note, BW\_SEL\_TRI pin is power on latch once set

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