



Must use 27 ohm, put close to pin <300mil.

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|-----|-----|----|---------------|
| Q0+ | R20 | 27 | PCIE_100M_0_P |
| Q0- | R21 | 27 | PCIE_100M_0_N |
| Q1+ | R22 | 27 | PCIE_100M_1_P |
| Q1- | R23 | 27 | PCIE_100M_1_N |
| Q2+ | R24 | 27 | PCIE_100M_2_P |
| Q2- | R25 | 27 | PCIE_100M_2_N |
| Q3+ | R26 | 27 | PCIE_100M_3_P |
| Q3- | R27 | 27 | PCIE_100M_3_N |
| Q4+ | R28 | 27 | PCIE_100M_4_P |
| Q4- | R29 | 27 | PCIE_100M_4_N |
| Q5+ | R30 | 27 | PCIE_100M_5_P |
| Q5- | R31 | 27 | PCIE_100M_5_N |

App Note:

1. Each VDD pin needs 0.1u +1uF decoupling close to pin.(e.g.:VDD, VDDR, VDDA...etc)
2. VDDA use small R=1~2 ohm or FB(ferrite bead)+C=10uF filtering for better DC/DC ripple noise rejection
3. This is LP HCSL type output: serial 27ohm R , but it can be replace in 27 to 33 ohm for the optimal fine tune the board RX end waveform or different trace length if needed
4. OEx# pins have internal pull-down
5. Connect e_Pad in 6 to 8 vias to GND plane
6. To Make LVDS output clock, it needs AC coupling and then RX side use pull-up/down Rs to bias in LVDS level, refer to datasheet;
7. Note, BW_SEL_TRI pin is power on latch once set

OE0#
 Make individual OEx# pull-up/down to enable/disable each output
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 .
 .
OE5#

BW_SEL_TRI:
 Set PLL BW logic in R4/R5
 "0"=L_BW,"M"=Bypass,"1"=H_BW

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| Title | | |
| P16CBE33063 Application schematic | | |
| Size | Document Number | Rev |
| B | Diodes Inc. Clock IC Application Engineering | 1.0 |
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