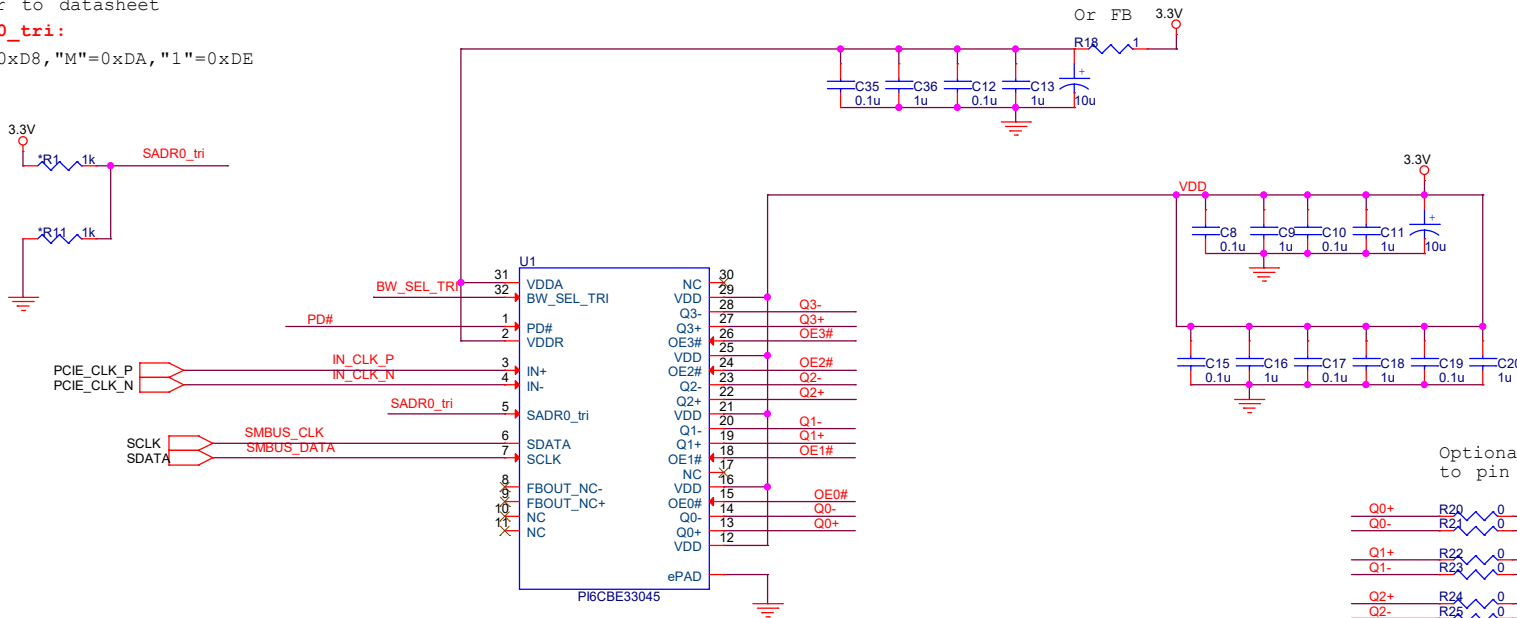


Set SADR0 logic in R1/R11,
refer to datasheet

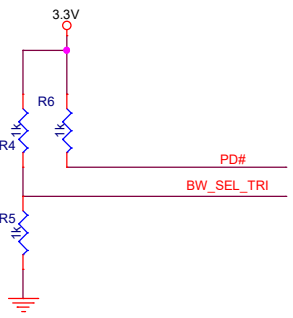
SADR0_tri:

"0"=0xD8, "M"=0xDA, "1"=0xDE



Optional, put close
to pin <300mil.

Q0+	R20	0	PCIE_100M_0_P
Q0-	R21	0	PCIE_100M_0_N
Q1+	R22	0	PCIE_100M_1_P
Q1-	R23	0	PCIE_100M_1_N
Q2+	R24	0	PCIE_100M_2_P
Q2-	R25	0	PCIE_100M_2_N
Q3+	R26	0	PCIE_100M_3_P
Q3-	R27	0	PCIE_100M_3_N



OE0#

Make individual OEx# pull-up/down to
enable/disable each output

OE3#

BW_SEL_TRI:

Set PLL BW logic in R4/R5

"0"=L_BW, "M"=Bypass, "1"=H_BW

App Note:

1. Each VDD pin needs 0.1u +1uF decoupling close to pin.(e.g.:VDD, VDDR, VDDA...etc)
2. VDDA use small R=1~2 ohm or FB(ferrite bead)+C=10uF filtering for better DC/DC ripple noise rejection
3. This is LP_HCSL type output: serial 0ohm R is optional, but it can be replace in 3 to 10 ohm for the optimal fine tune the board RX end waveform or different trace length if needed
4. OEx# pins have internal pull-down
5. Connect e_Pad in 4 to 6 vias to GND plane
6. To Make LVDS output clock, it needs AC coupling and then RX side use pull-up/down Rs to bias in LVDS level, refer to datasheet;
7. Note, BW_SEL_TRI pin is power on latch once set

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