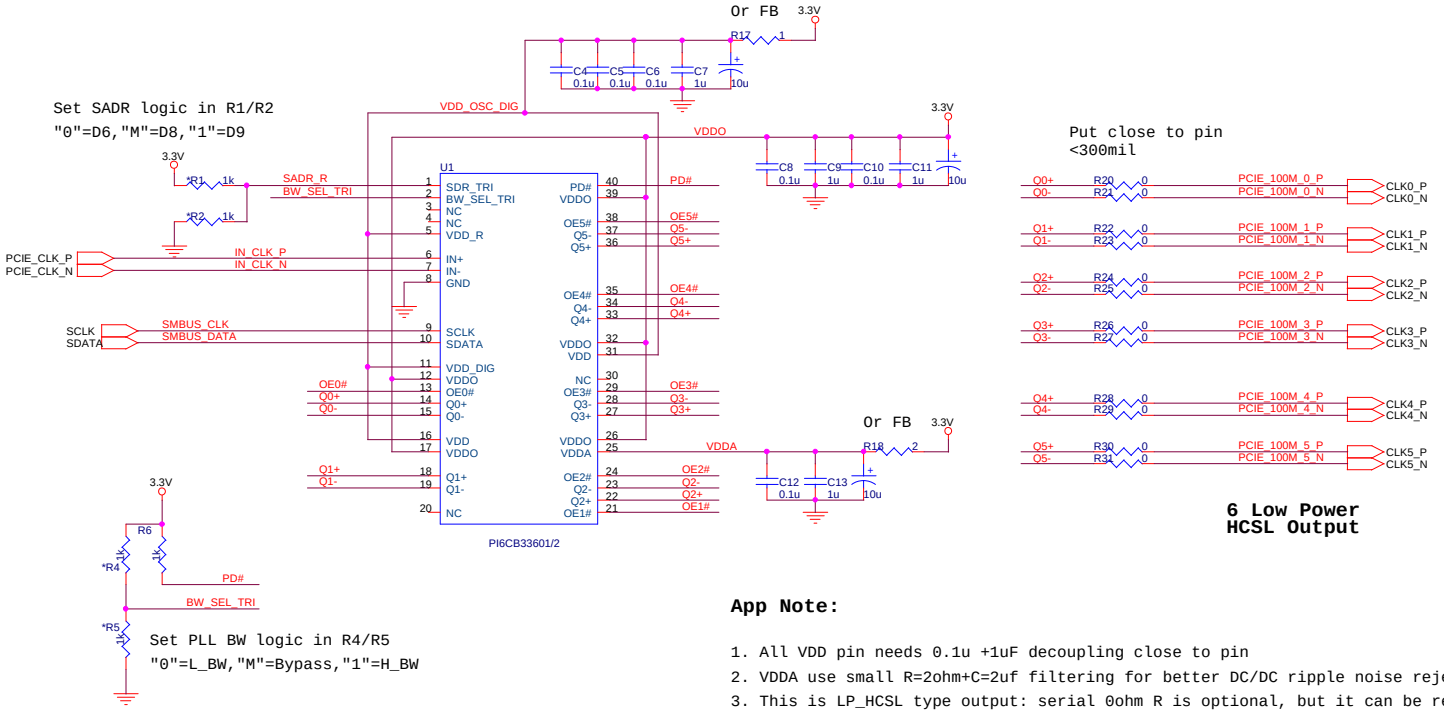

App Note:

1. All VDD pin needs 0.1u +1uF decoupling close to pin
2. VDDA use small R=2ohm+C=2uf filtering for better DC/DC ripple noise rejection
3. This is LP_HCSL type output: serial 0ohm R is optional, but it can be replace in 5 to 15 ohm for the optimal fine tune the board RX end wavefrom for different trace length if needed
4. Note, SMBUS address and PLL Bypass pins are power on latch once set;
5. OEx# pins have internal pull-down
6. Connect epad in 8 vias to GND plane
7. To Make LVDS output clock, it needs AC coupling and then RX side use pull-up/down Rs to bias in LVDS level, refer to datasheet;

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