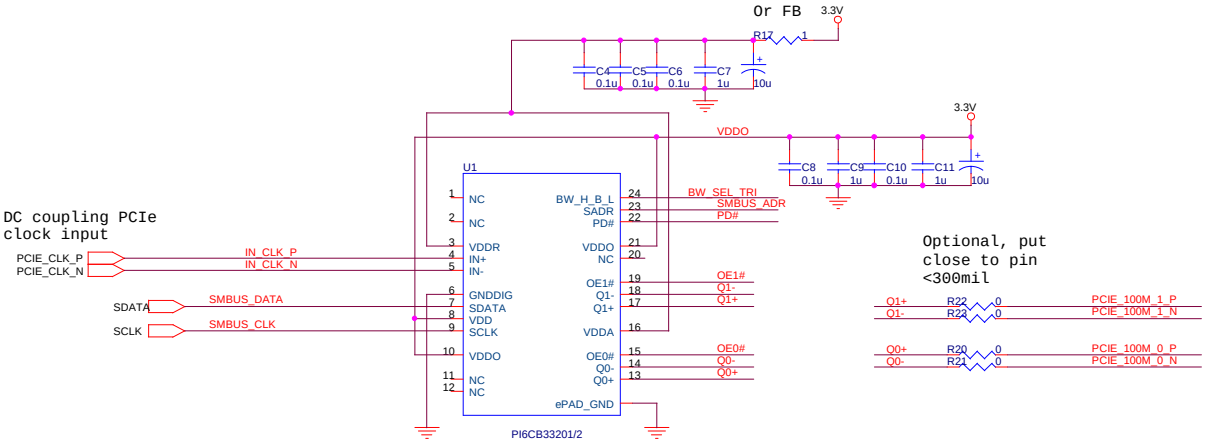

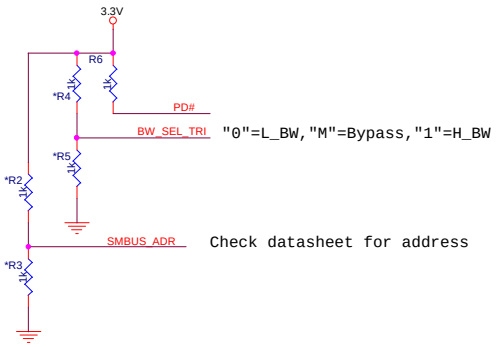

App Note:

1. All VDD pin needs 0.1u +1uF decoupling close to pin
2. VDDA use small R+C filtering for better DC/DC ripple noise rejection
3. This device is LP_HCSL output, serial R at output is optional for 5 to 10ohm fine tune waveform, if needed
4. Note SMBUS address and PLL Bypass pins are power on latch once set;
5. OEx# pins have internal pull-down for Enable, Disable needs pull-up
6. Thermal pad is IC GND, make 4 vias connected to GND plane
7. Make LVDS output clock, it needs AC coupling and then RX side use pull-up/down Rs to bias LVDS level, refer to datasheet;

Title	PI6CB33201/2 Application schematic	
Size B	Document Number Diodes Inc. Clock IC Application Engineering	Rev 1.0
Date: Monday, June 10, 2019	Sheet 1 of 1	