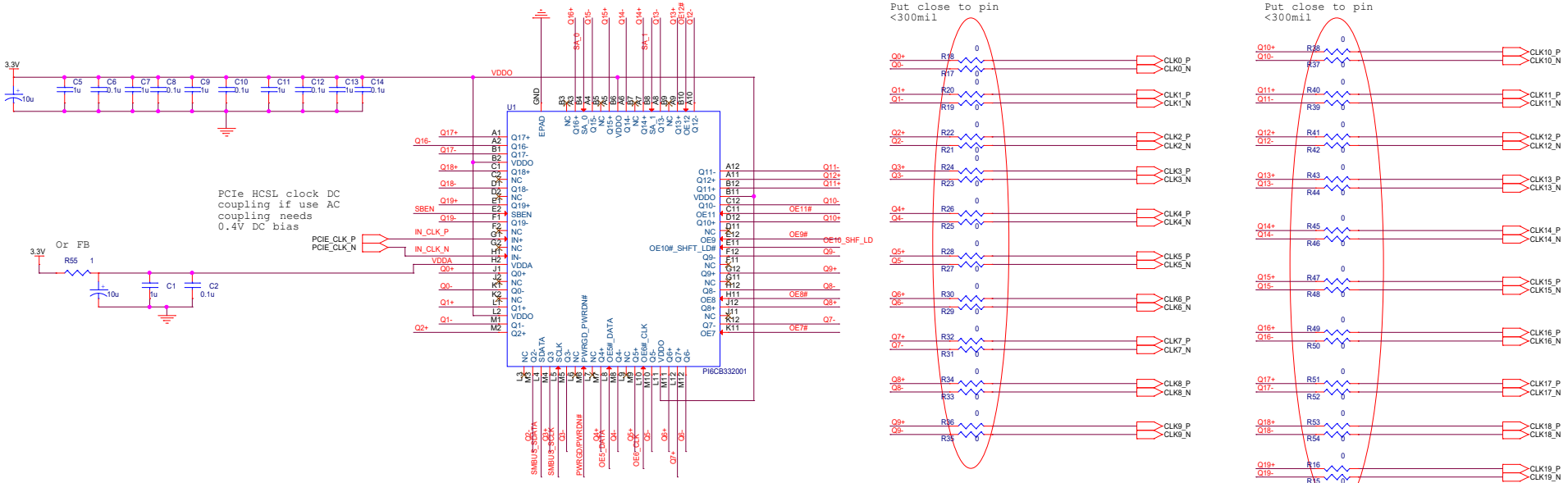
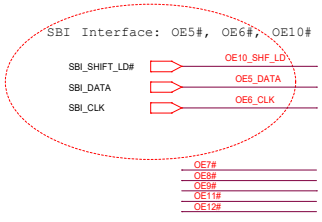
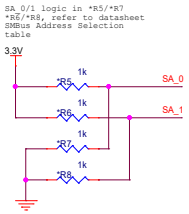
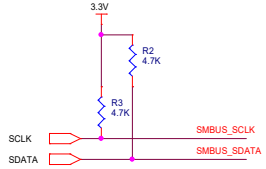




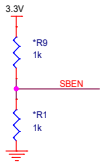




SBEN:

Set SBEN logic in R1/R9

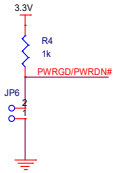
0: Side-band interace disable;
OE5#, OE6#, OE10# pins function is as output enable.
1: Side-band interface enable;
OE5#, OE6#, OE10# pins function is as SBI control.



PWRGD/PWRDN#:

Set PWRGD/PWRDN# logic in R4/JP6

0: Power Down Mode;
1: Exit Power Down Mode;



App Note:

1. Each VDD pin needs 0.1u +1uF decoupling close to pin. (e.g.: VDD, VDDA, VDDR...etc)
2. VDDA use small R=1~2 ohm or FB(ferrite bead)+C=10uF filtering for better DC/DC ripple noise rejection
3. This is LP_HCSL type output: serial 0ohm R is optional, but it can be replace in 3 to 10 ohm for the optimal fine tune the board RX end waveform or different trace length if needed
4. Note, SMBUS address pins are power on latch once set;
5. OEx# pins have internal pull-down
6. Connect epad in 8 to 12 vias to GND plane
7. To Make LVDS output clock, it needs AC coupling and then RX side use pull-up/down Rs to bias in LVDS level, refer to datasheet;

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