

PI6CB18801 EVB Use Manual

Timing Application Engineering

1.1 Introduction

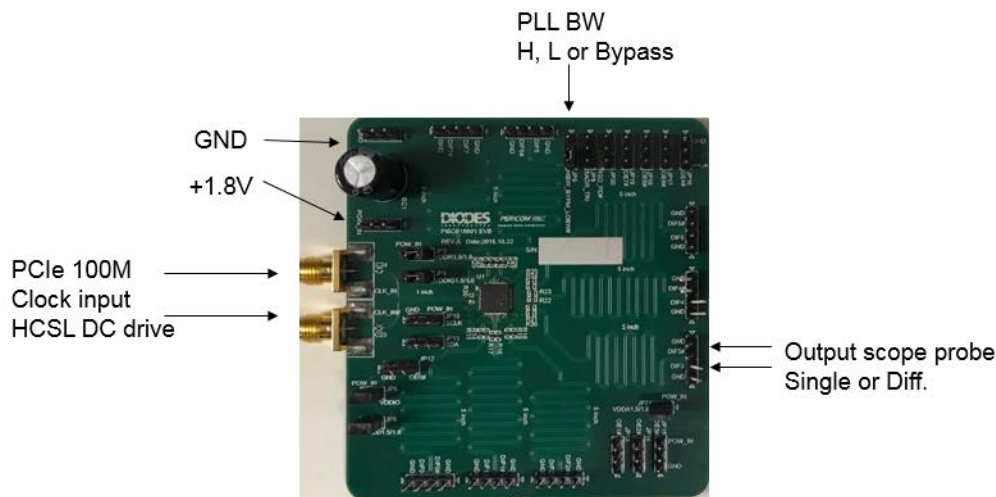
PI6CB18801 is 1.8V PCIe clock Zero-Delay-Buffer family product. Its low power HCSL output makes the IC has very low power consumption in high performance to comply with PCIe 2.0, 3.0, and 4.0 PCL_SIG.org reference clock waveform and jitter specifications. This doc. is to provide the EVB use guide and test example.

1.2 DUT Reference

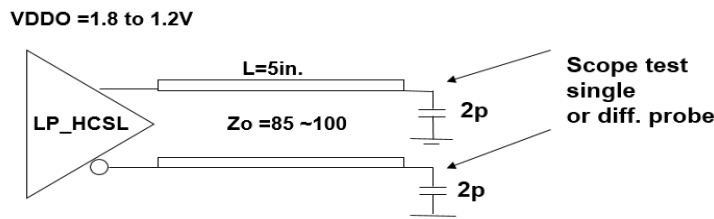
1. Datasheet
2. EVB PCB and schematic
3. Device application circuit

1.3 EVB Photo and Test Diagram

- 1) EVB photo and connection guide



- 2) LP_HCSL test diagram



1.3 Equipment

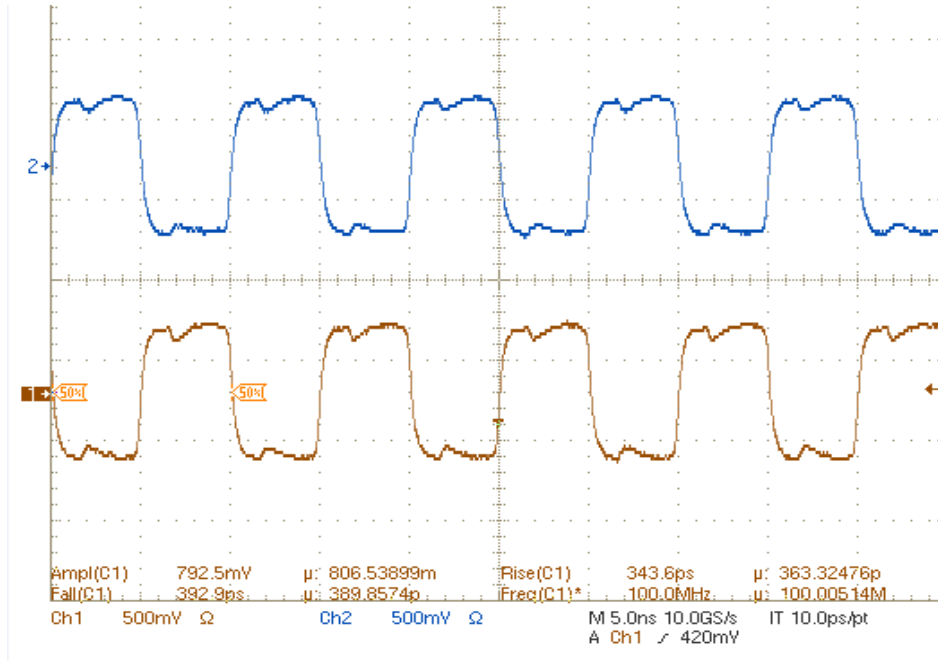
- Agilent DC supply: E3631A
- Tektronix real time scope 20G/S: TDS7404

2.1 Summary

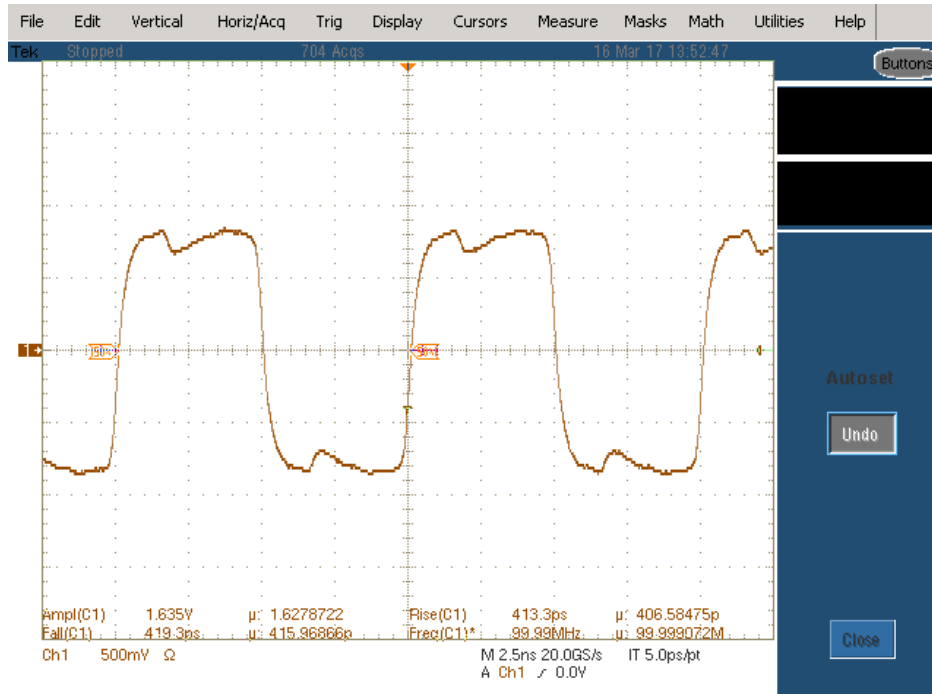
- i) The single output waveform $T_r/T_f = 363/389ps$; $V_{amp} = 806mV$
- ii) differential output waveform $T_r/T_f = 406/415ps$; $V_{amp} = 1.62V$
- iii) The EVB meets design spec.

3.1 Test Reference Waveform

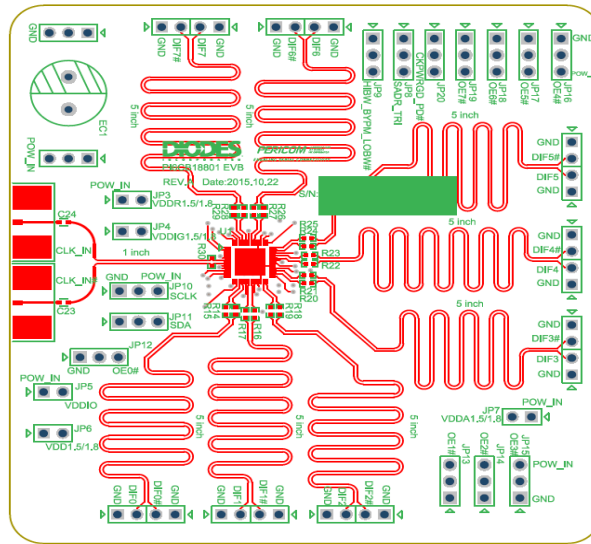
1) Tek scope single end probe waveform



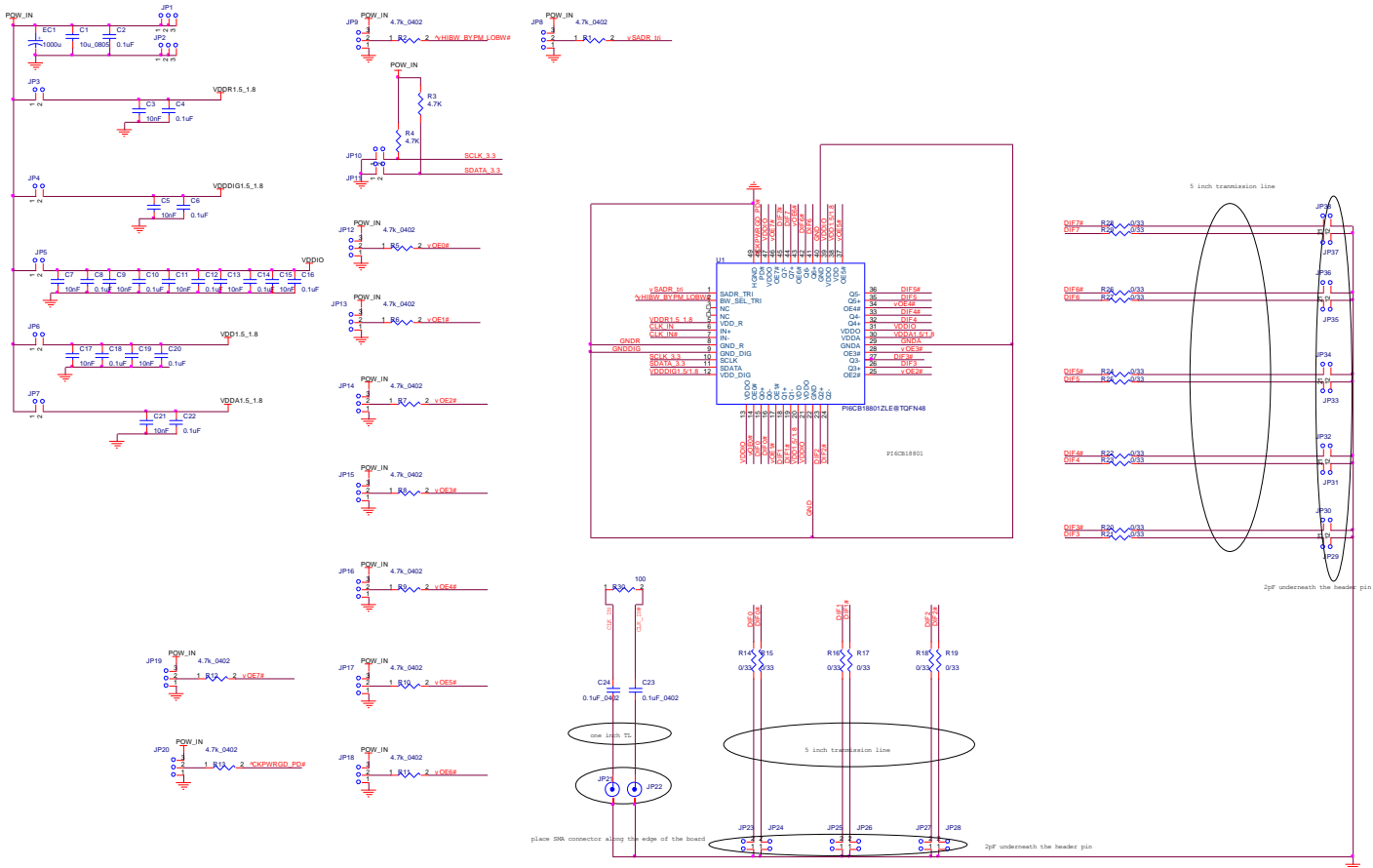
2) Tek scope differential probe waveform



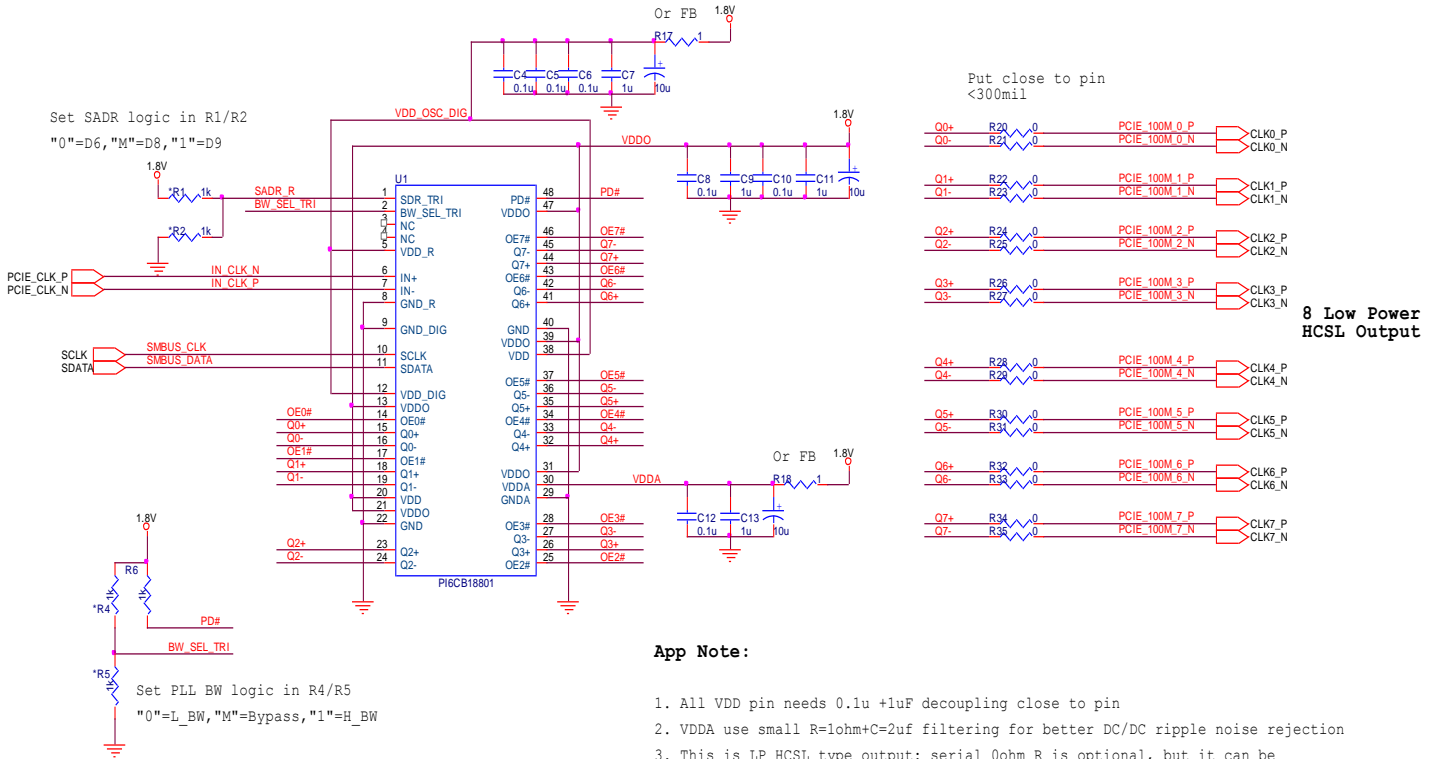
3.2 EVB PCB Layout



3.3 EVB Schematic



3.4 PI6CB18801 Application Circuit



App Note :

1. All VDD pin needs 0.1u +1uF decoupling close to pin
2. VDDA use small R=1ohm+C=2uf filtering for better DC/DC ripple noise rejection
3. This is LP_HCSL type output: serial 0ohm R is optional, but it can be replace in 5 to 15 ohm for the optimal fine tune the board RX end waveform for different trace length if needed
4. Note SMBUS address and PLL Bypass pins are power on latch once set;
5. Make LVDS clock, it needs AC coupling and then RX side use pull-up/down Rs to bias LVDS level, refer to datasheet;
6. OEx# pins have internal pull-up, can be left pin open

Document History

Revision	Date	Description	Author
1.0	Jan, 2018	1 st rev. doc	Timing AE