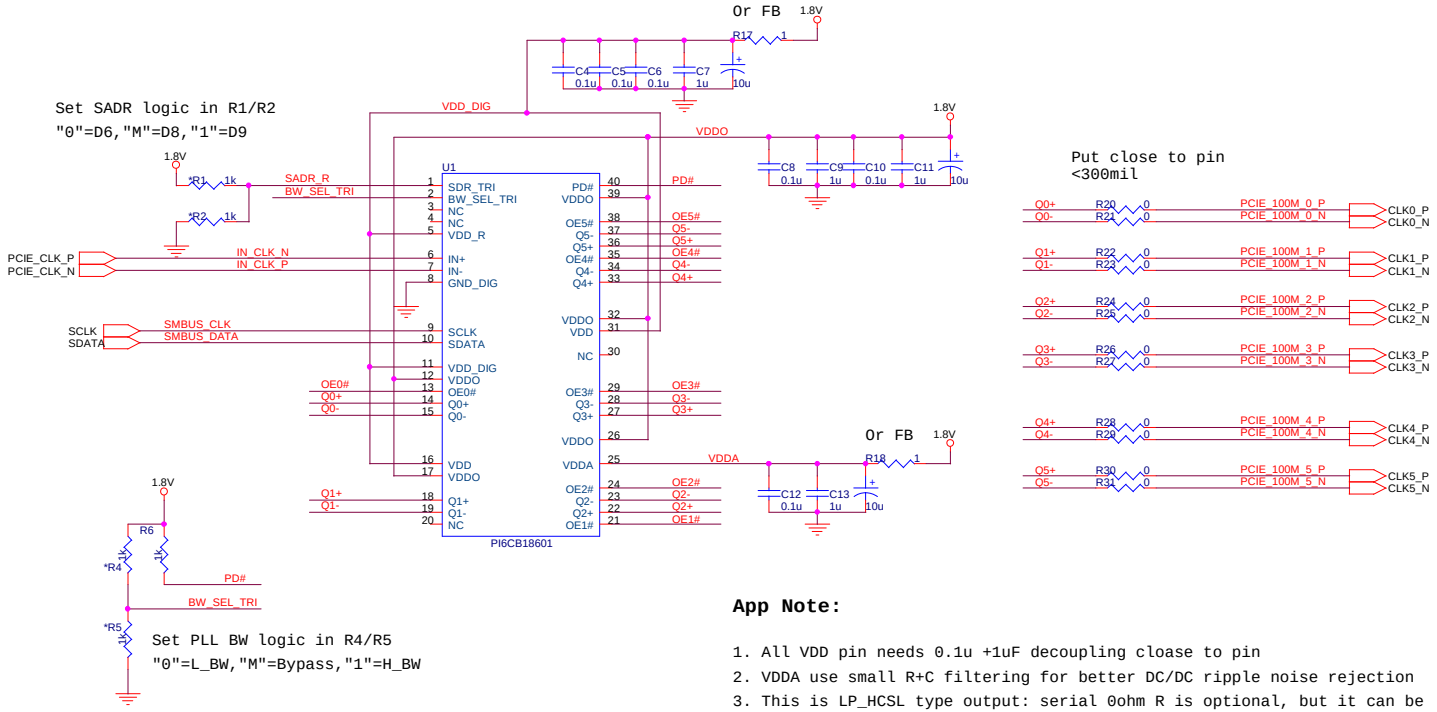

App Note:

1. All VDD pin needs 0.1u +1uF decoupling cloase to pin
2. VDDA use small R+C filtering for better DC/DC ripple noise rejection
3. This is LP_HCSL type output: serial 0ohm R is optional, but it can be replace in 5 to 15 ohm for the optimal fine tune the board RX end wavefrom for different trace length if needed
4. Note SMBUS address and PLL Bypass pins are power on latch once set;
5. Make LVDS clock, it needs AC coupling and then RX side use pull-up/down Rs to bias LVDS level, refer to datasheet;
6. OEx# pins have internal pull-up, can be left pin open
7. Thermal pad is IC GND, make > 4 vias connected to GND plane

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