



App Note:

1. All VDD pin needs 0.1u +1uF decoupling close to pin
2. VDDA use small R+C filtering for better DC/DC ripple noise rejection
3. This device LP_HCSL type output needs 33ohm serial R at output
4. Note SMBUS address and PLL Bypass pins are power on latch once set;
5. OEx# pins have internal pull-down for Enable, Disable needs pull-up
6. Thermal pad is IC GND, make > 4 vias connected to GND plane
7. Make LVDS clock, it needs AC coupling and then RX side use pull-up/down Rs to bias LVDS level, refer to datasheet;

Title		
Pi6CB18200 App. Schematic		
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