

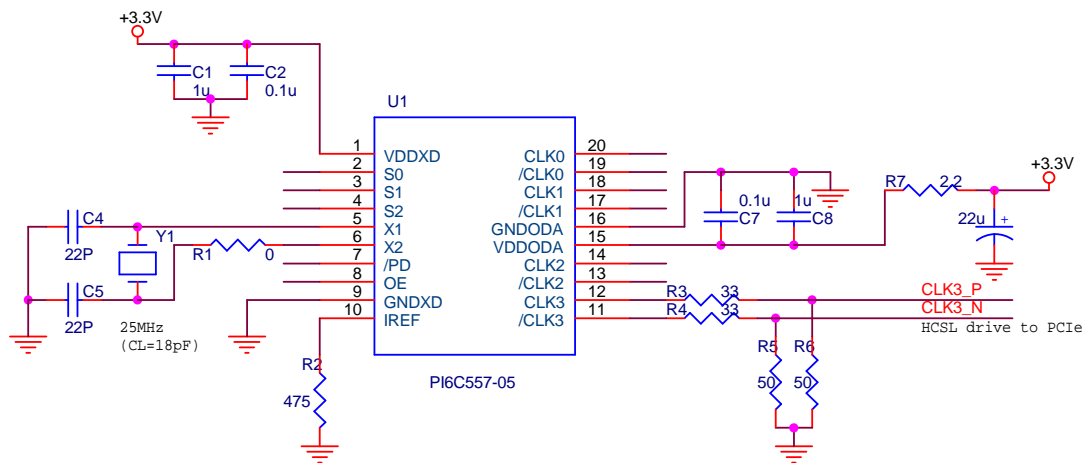
## PI6C557-05 Application and PCB Guide

Pericom Application Engineering

### 1. Introduction

PI6C557-05 is a high performance clock generator for PCIe reference clock applications. This document is to provide customer application information.

### 2. Application Schematic



Note:

- 1) Put each VDD 0.1uF decoupling cap. at least, all GNDs on one solid GND plane
- 2) On VDDA use serial 2.2 ohm in R7 to replace FB for better low frequency noise filtering
- 3) Leave un-used CLKx and /CLKx open
- 4) For small size crystal 3225 for example, choose R1=360
- 5) For output frequency and SSCG setting, please refer to the datasheet logic table

### 3. Crystal Circuit Layout

- 1) X1 and X2 pins connected to crystal trace loop should be very narrow without any board via in the loop with solid GND plane underneath.
- 2) Place crystal closer to the IC X1, X2 pins as possible and route crystal C1 and C2 load caps. on the comp layer without via between crystal pins;
- 3) Keep load cap. C1 and C2 GND pins close together to reduce board noise coupling into these caps.

### 4. HCSL Differential Output Layout

Place 33ohm serial and 50 ohm pull down <250mil close to IC output pins on comp. side. A 475 ohm resistor to GND must be connected on pin 10 (IREF) for output drive current reference.