PI6C557-03A Matches Mini. PCIe WiFi Modular Design

Pericom Timing Application Engineering

1. Introduction

PI6C557-03A is a low jitter high performance clock generator good for PCIe reference clock applications especially good for today's mini. PCIe modular designs since it only needs a 25M crystal to generate two PCIe reference clocks which meets small cell PCIe modular system design, as the following diagram Fig. 1 shows example, to match various vendor embedded processors (MCUs) PCIe adapter port applications such as WiFi/BT adapters, small cell WiFi carrier, and many other embedded controllers for home and industrial automations.

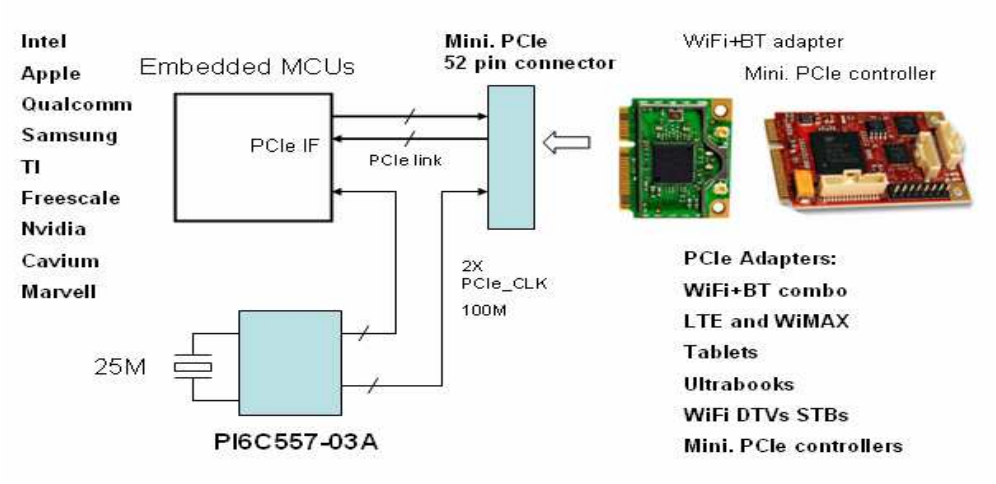

Figure 1. PC6C557-03A Good for PCIe WiFi designs

The mini. PCIe connector pin description and its use advantages are listed as in Fig. 2 and Fig. 3.

PCI Express Mini Card

Row	Pin	Symbol	Type	Legend	Status
0	1	WAKE#			
0	3	COEX1		Function is OEM specific	changed
0	5	COEX2		Function is OEM specific	changed
0	7	CLKREQ#	O	Request to ICS9DB106 for clock signal. MiniCard can tie to ground. USB-only cards leave this open.	
0	9	Gnd			
0	11	REFCLK-	I	Clock input from buffer	
0	13	REFCLK+	I	Clock input from buffer	
0	15	Gnd			
0	17	Reserved		Reserved for future SIM Card pin C8	
0	19	Reserved		Reserved for future SIM Card pin C4	
0	21	Gnd			
0	23	PERn0	I	PCI Express RX -	
0	25	PERp0	I	PCI Express RX +	
0	27	Gnd			
0	29	Gnd			
0	31	PETn0	O	PCI Express TX -	
0	33	PETp0	O	PCI Express TX +	
0	35	Gnd			

PI6C557-03A 100MHz

PCIe IF TX/TX

Figure 2. Mini. PCIe connecter pin discrétion (partial)

PCIe mini card connector is right angle, low profile, min-mount pitch which is popular for most telecommunication device designs in the following Figure 3.

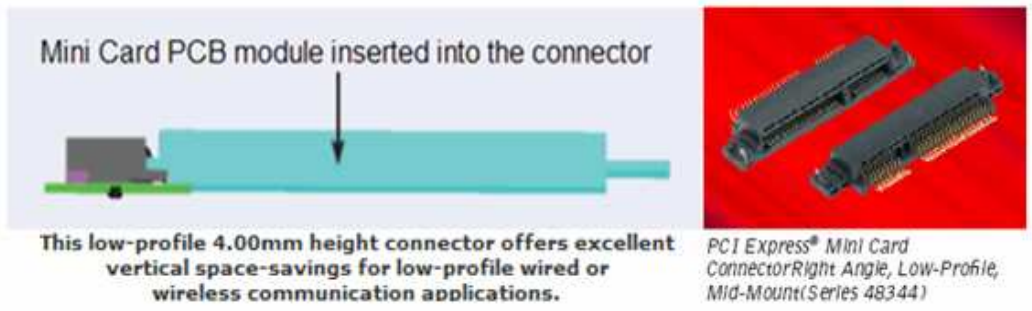

Figure 3. Mini. PCIe Connector Advantages

2. PI6C557-03A General Use Guide

Fig. 4 is PI6C557-03A circuit application guide schematic, please refer to reference circuit for more detail connection.

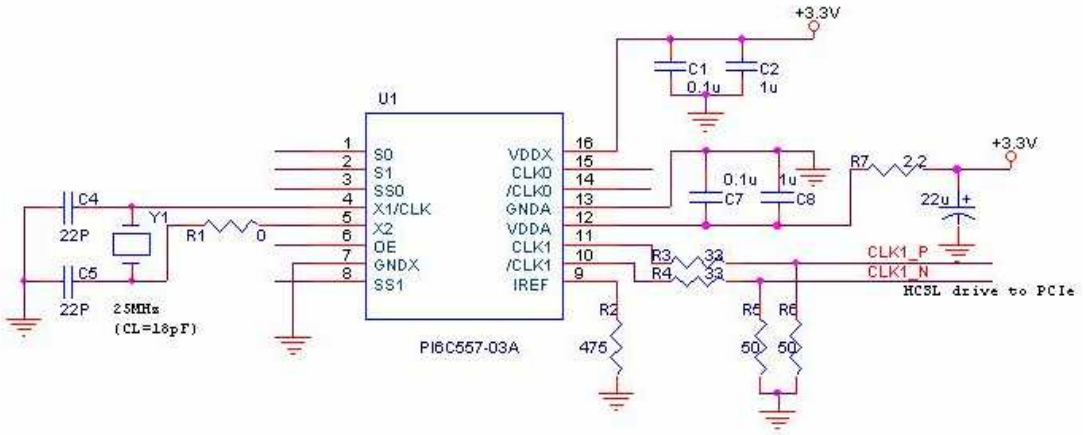

Figure 4. PI6C557-03A device application guide

Circuit connection note:

1. Put each VDD 0.1uF and 1uF decoupling cap. at least, all GNDs are on one solid GND plane
2. On VDDA use serial 2.2 ohm in R7 to replace FB for better low frequency noise filtering
3. Leave un-used CLKx and /CLKx open
4. For small size crystal 3225 for example, choose R1=360
5. For output frequency and SSCG setting, please refer to the datasheet logic table

3. Crystal Circuit Layout

1) X1 and X2 pins are connected to crystal trace loop which should be very narrow without any board via in the loop and need keep-out around the traces;
2) Place crystal closer to the IC X1, X2 pins as possible and route crystal C1 and C2 load caps. on the top layer without via during to the crystal pins;
3) Keep load cap. C1 and C2 GND pins close together to reduce board noise coupling into these caps.

4. HCSL Differential Output Layout

Place 33ohm serial and 50 ohm pull down <300mil. close to IC output pins on comp. side. A 475 ohm resistor to GND must be connected on pin 9 (IREF) for output drive current control. Without IREF 475 ohm, there will be no outputs. The Figure 5. shows the example of PCB placement and routing.

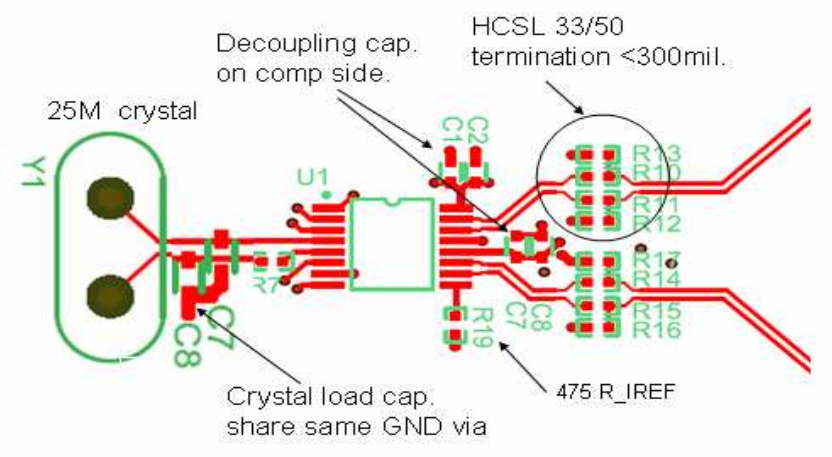

Figure 5. PI6C557-03A PCB layout example

5. HCSL Used in LVDS Output Drive

HCSL can be terminated in LVDS drive due to the IC output is in current mode, in other word, the output voltage level and V_swing range can be changed in different resistor value and connection scheme as Figure 6 shows. Please refer to product datasheet for more detail.

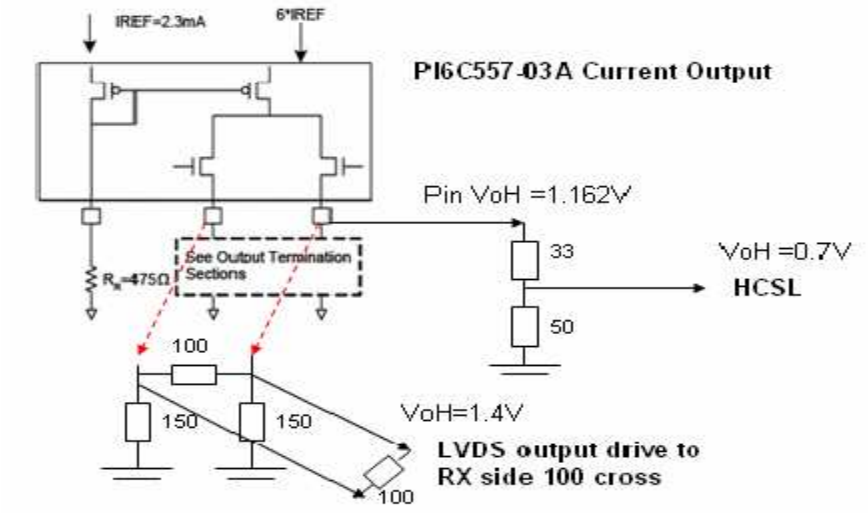

Figure 6. PI6C557-03A HCSL and LVDS Terminations

6. Other Similar PCIe Clock Product

PI6C557-05 has the same design consideration as PI6C557-03A, but it has 4 PCIe output clocks for more clock design need.
http://www.pericom.com/assets/Datasheets/PI6C557-05.pdf

PI6C557-06 is two PCIe input clock mux to 4 PCIe clock outputs. It is a PCIe differential clock buffer product.
http://www.pericom.com/assets/Datasheets/PI6C557-06.pdf

For more PCIe reference clock design consideration, please visit company web site: Clock IC category.
http://www.pericom.com/products/clocks/clock-ic/

Appendix:

Mini. PCIe connector pin description

PCI Express Mini Card

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0	25	PERp0	I	PCI Express RX +	
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0	29	Gnd			
0	31	PETn0	O	PCI Express TX -	
0	33	PETp0	O	PCI Express TX +	
0	35	Gnd			

PI6C557-03A 100MHz

PCIe IF TX/TX

0	35	Gnd			
0	37	Gnd			changed
0	39	3.3Vaux			changed
0	41	3.3Vaux			changed
0	43	Gnd			changed
0	45	Reserved			
0	47	Reserved			
0	49	Reserved			
0	51	Reserved			
1	2	3.3 Vaux			changed
1	4	Gnd			
1	6	1.5 Volt			
1	8	UIM PWR	O	SIM Card	
1	10	UIM_DATA	I/O	SIM Card	
1	12	UIM_CLK	O	SIM Card	
1	14	UIM_RESET	O	SIM Card	
1	16	UIM_VPP	O	SIM Card	
1	18	Gnd			
1	20	W_DISABLE#	I	Wireless disable (active low)	changed
1	22	PERST#	I	Power Good (Reset)	

1	24	3.3Vaux			
1	26	Gnd			
1	28	1.5Volt			
1	30	SMB CLK	I	SM Bus Clock	
1	32	SMB Data	I/O	SM Bus Data	
1	34	Gnd			
1	36	USB_D-	I/O	USB Data	
1	38	USB_D+	I/O	USB Data	
1	40	Gnd			
1	42	LED_WWAN#	O	Active low, max 9mA	
1	44	LED_WLAN#	O	Active low, max 9mA	
1	46	LED_WPAN#	O	Active low, max 9mA	
1	48	1.5Volt			
1	50	Gnd			
1	52	3.3Vaux			changed

Support SMBUS and USB

= Verified with PCI Express Mini Card Electromechanical Specification, 1.0, with ECN