**Verification of PI6C49X0206T IBIS model**

1. **Introduction:**

To verify the correlation between the ibis model and hspice model, we need to do some simulations:

**The frequency of signal is 100MHz:**

Vin0 in0 0 pulse(0 **3.3** 0 .2n .2n 9.8n 20n)

1. Add **50Ω pull-down** resistor to VDD, and 5pf pull-down capacitance to the OUTPUT

PI6C49X0206T

**VOUT**

**SCL\_C**

**SDA\_C**

**R**

**SCL\_C**

**SDA\_C**

CLK

**SCL\_C**

**SDA\_C**

**C**

**SCL\_C**

**SDA\_C**

**Input Signals**

**SCL\_C**

**SDA\_C**

Q0

**SCL\_C**

**SDA\_C**

**VIN**

**SCL\_C**

**SDA\_C**

Q1

**SCL\_C**

**SDA\_C**

1. Simulation **without** package data;
2. Simulation with package data.
3. Add **50Ω pull-up** resistor to VDD, and 5pf pull-down capacitance to the OUTPUT

PI6C49X0206T

**VOUT**

**SCL\_C**

**SDA\_C**

**R**

**SCL\_C**

**SDA\_C**

CLK

**SCL\_C**

**SDA\_C**

**C**

**SCL\_C**

**SDA\_C**

**Input Signals**

**SCL\_C**

**SDA\_C**

Q0

**SCL\_C**

**SDA\_C**

**VIN**

**SCL\_C**

**SDA\_C**

Q1

**SCL\_C**

**SDA\_C**

**VDDO**

**SCL\_C**

**SDA\_C**

1. Simulation **without** package data;
2. Simulation with package data.
3. Add **33Ω** resistor, 5 inches trace and 5pf pull-down capacitance to the OUTPUT

PI6C49X0206T

**VOUT**

**SCL\_C**

**SDA\_C**

**R**

**SCL\_C**

**SDA\_C**

CLK

**SCL\_C**

**SDA\_C**

**C**

**SCL\_C**

**SDA\_C**

**Input Signals**

**SCL\_C**

**SDA\_C**

Q0

**SCL\_C**

**SDA\_C**

**VIN**

**SCL\_C**

**SDA\_C**

Q1

**SCL\_C**

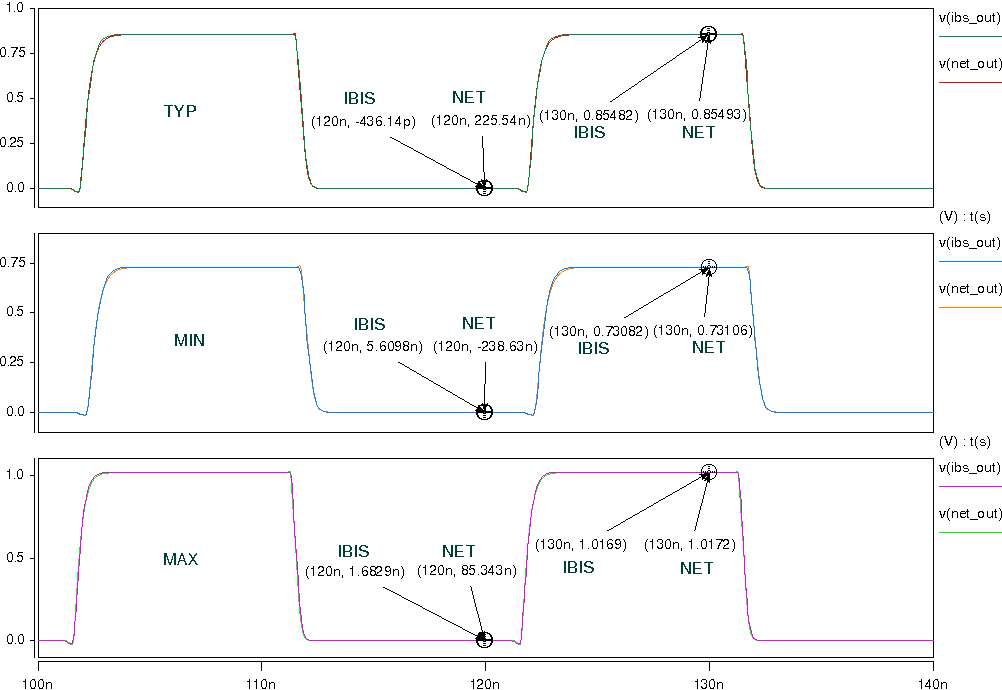
**SDA\_C**

**Trace**

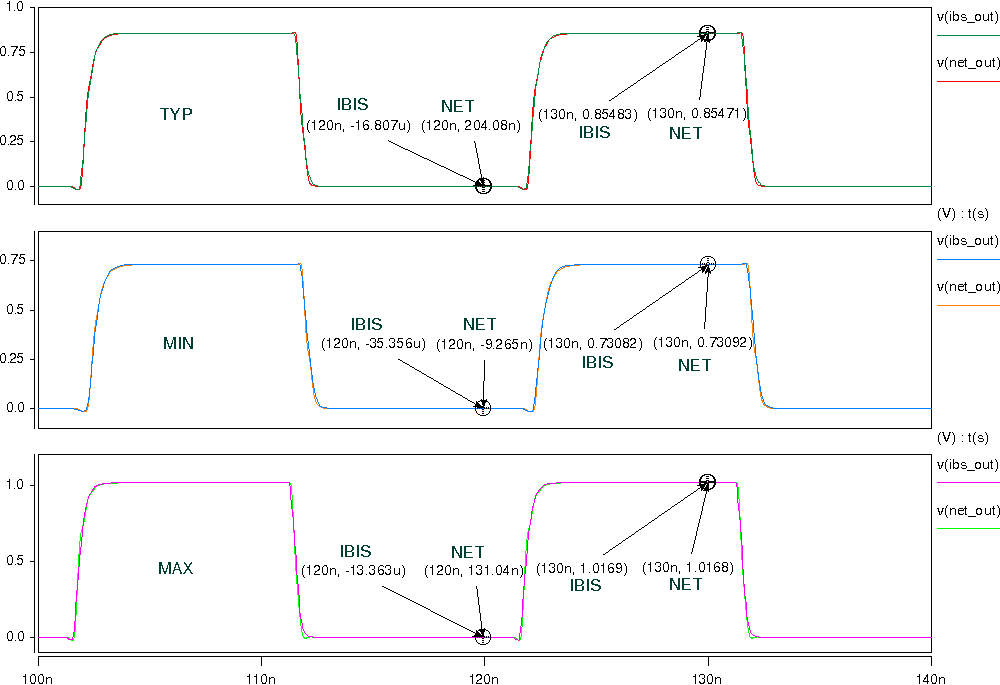
**SCL\_C**

**SDA\_C**

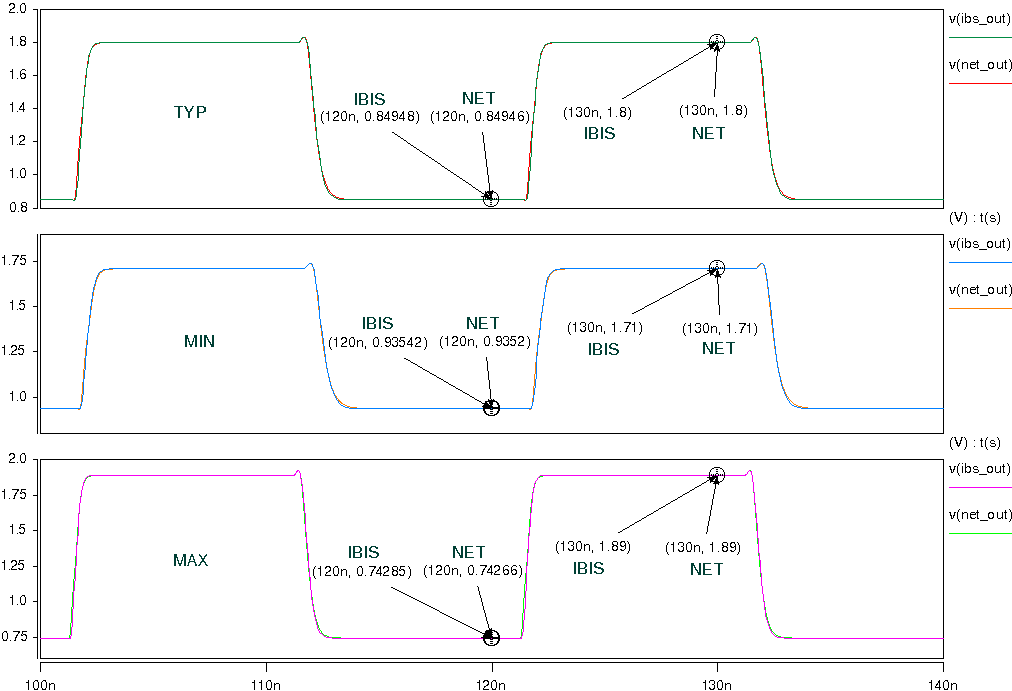
1. Simulation **without** package data;
2. Simulation with package data.
3. **Conclusion:**
4. For OUTPUT, the simulation results of IBIS model can match very well with the HSPICE model at different simulating conditions.
5. **Simulation Result:**
6. Add **50Ω pull-down** resistor to VDD, and 5pf pull-down capacitance to the OUTPUT
7. Simulation **without** package data;



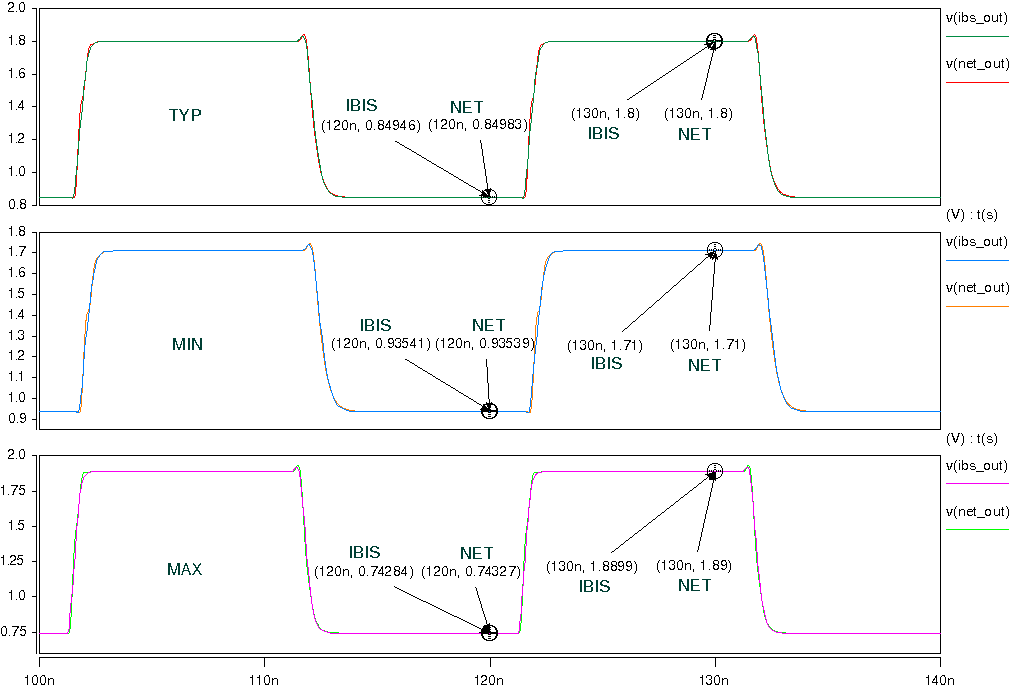
1. Simulation with package data.



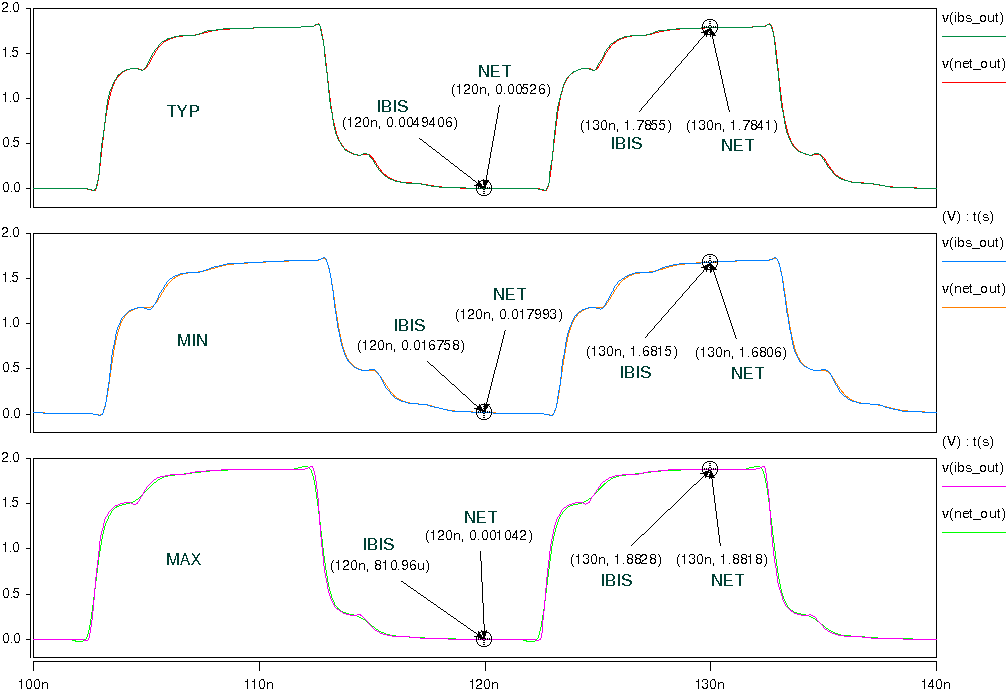
1. Add **50Ω pull-up** resistor to VDD, and 5pf pull-down capacitance to the OUTPUT
2. Simulation **without** package data;



1. Simulation with package data.



1. Add **33Ω** resistor, 5 inches trace and 5pf pull-down capacitance to the OUTPUT
2. Simulation **without** package data;



1. Simulation with package data.

