**Verification of PI6C49S1510A IBIS model**

1. **Introduction:**

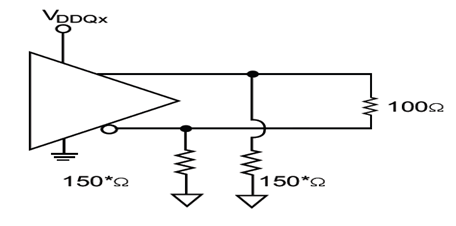
To verify the correlation between the ibis model and hspice model, we need to do some simulations:

1. For LVPECL:
2. Add each 150ohm resistor to ground and 100ohm between the differential output;
3. Add each 150ohm resistor to ground, 2inch trace and 100ohm between the differential output;
4. For LVDS:
5. Add 100ohm resistor between the differential output;
6. Add 100ohm resistor and 2inch trace between the differential output;
7. For HCSL:
8. Add each 33ohm and 50ohm at the differential output;
9. Add each 33ohm resistor, 2inch trace and 2pF capacitor at the differential output, and add each 50ohm resistor to ground after 33ohm resistor;
10. **Conclusion:**

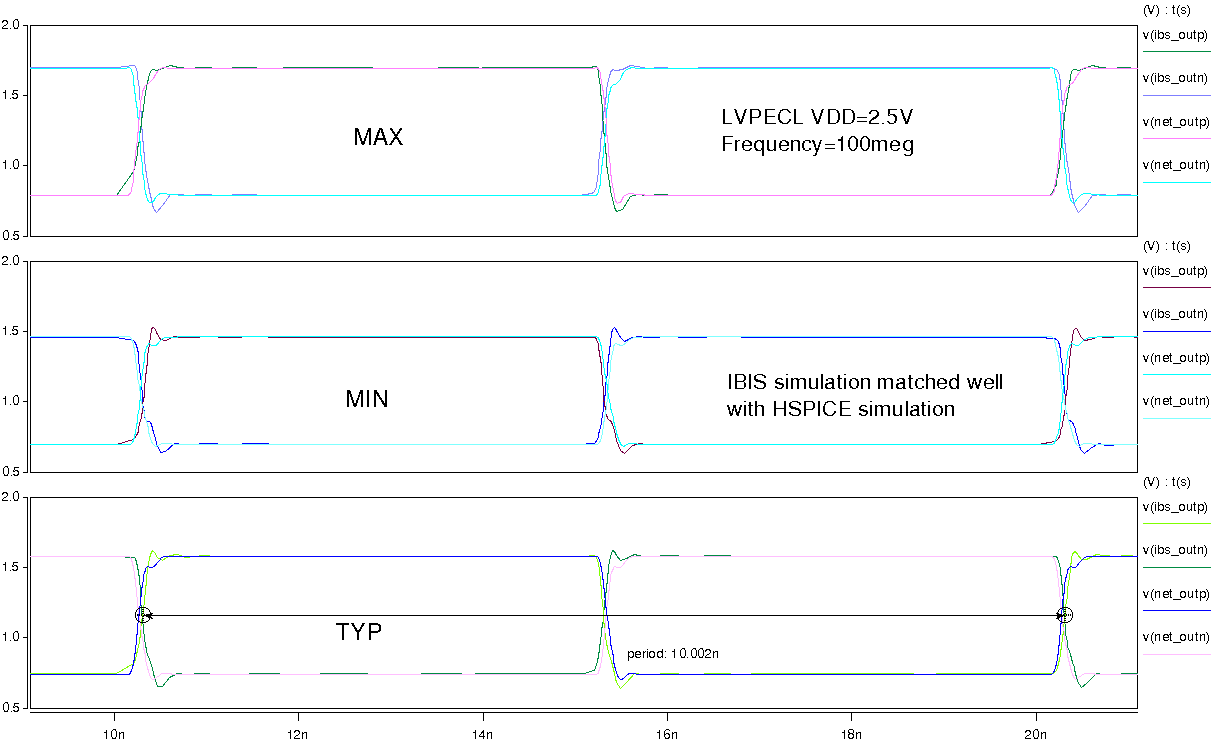
The simulated results show that the generated IBIS model can match well with the HSPICE model at different load conditions.

But there are still some **issues**:

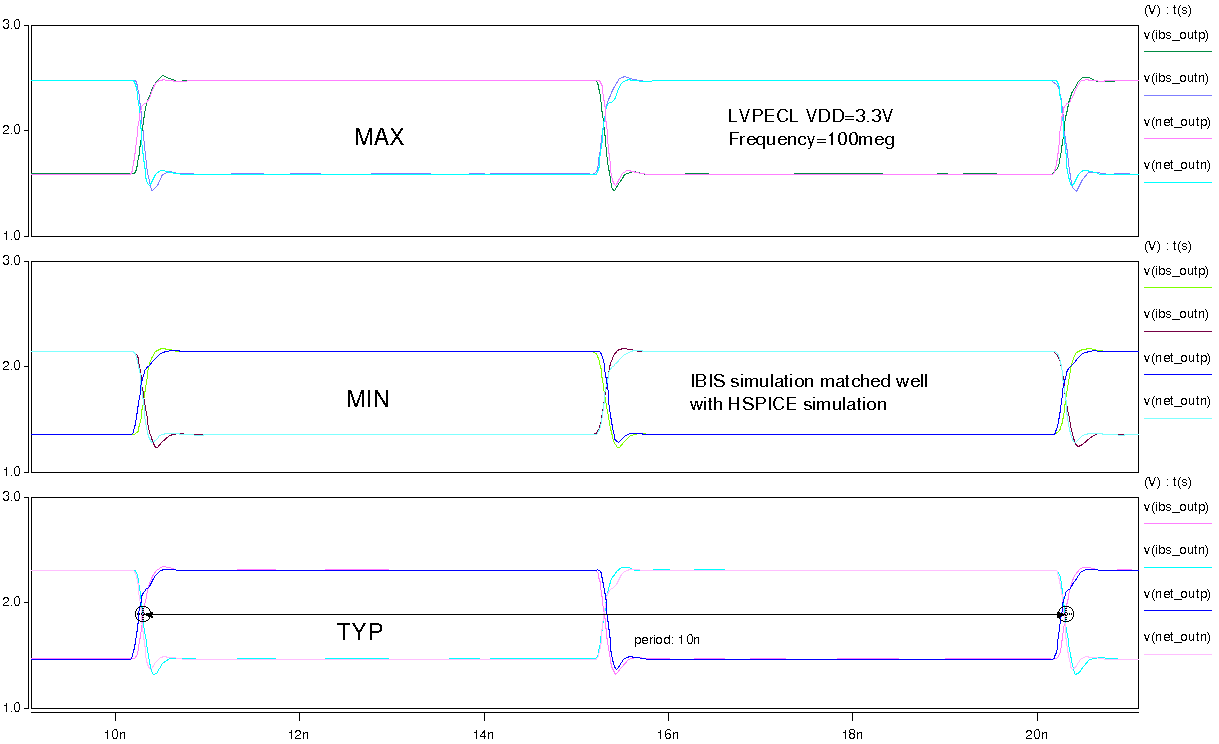
1. There is some over shoot at the rise-edge and fall-edge of “LVPECL” IBIS simulation while it is disappeared in the HSPICE simulation.
2. **LVPECL simulation:**

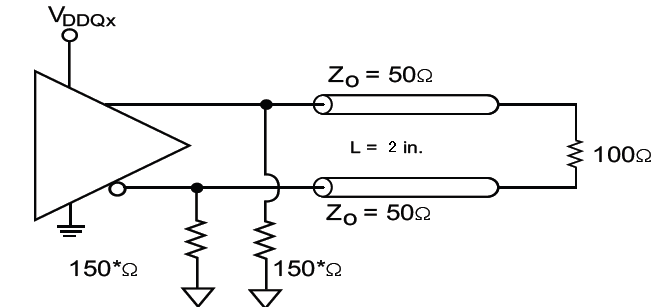


VDD=2.5V

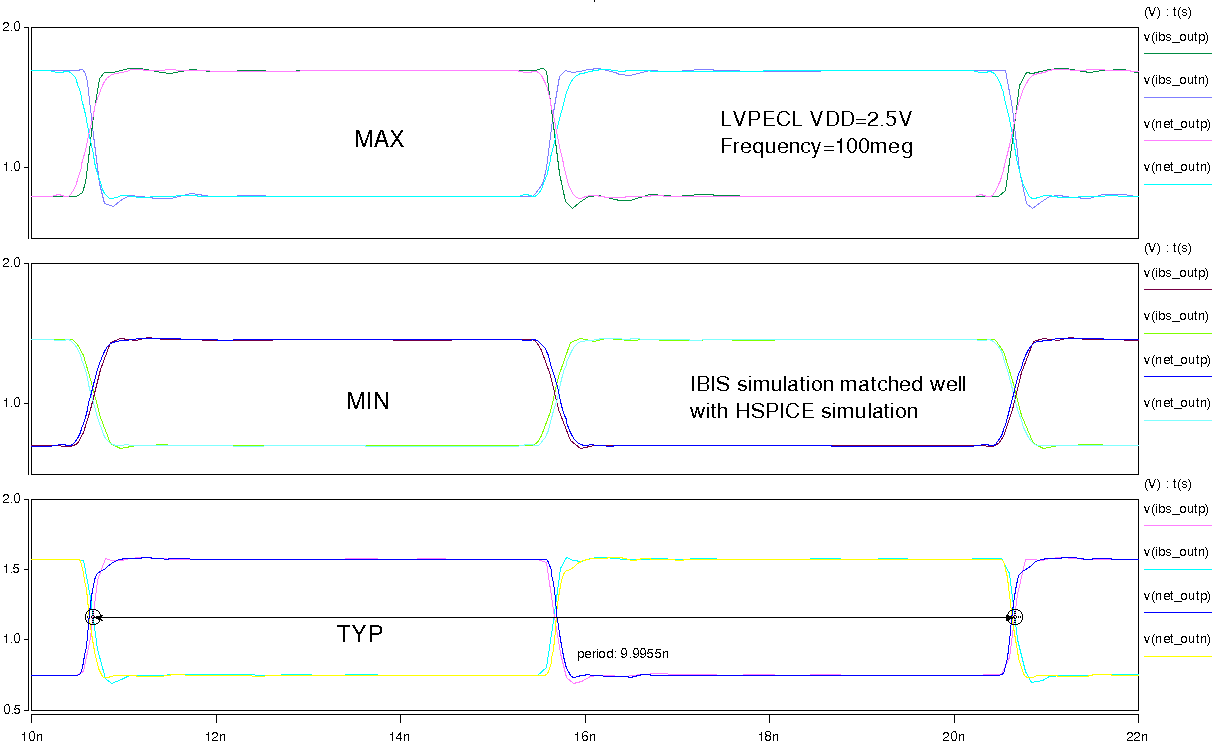


VDD=3.3V

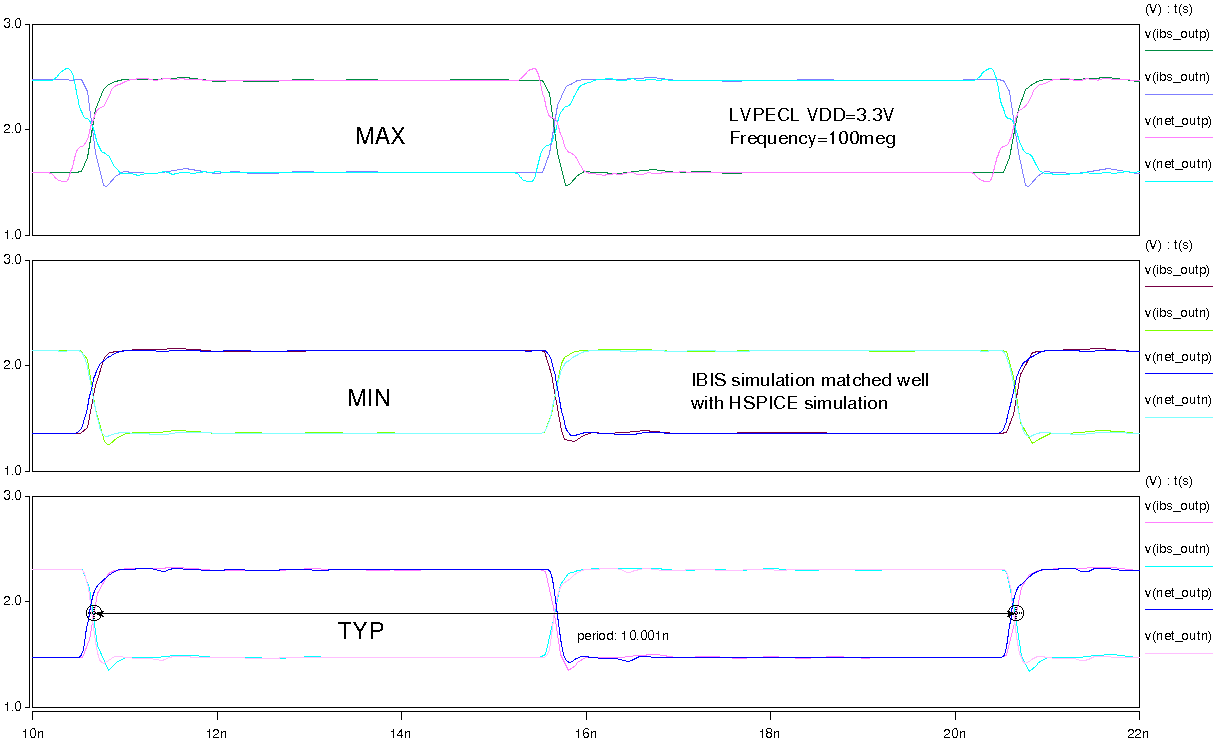




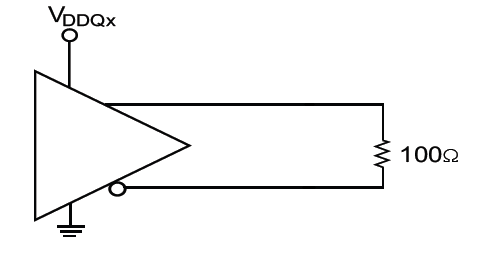
VDD=2.5V



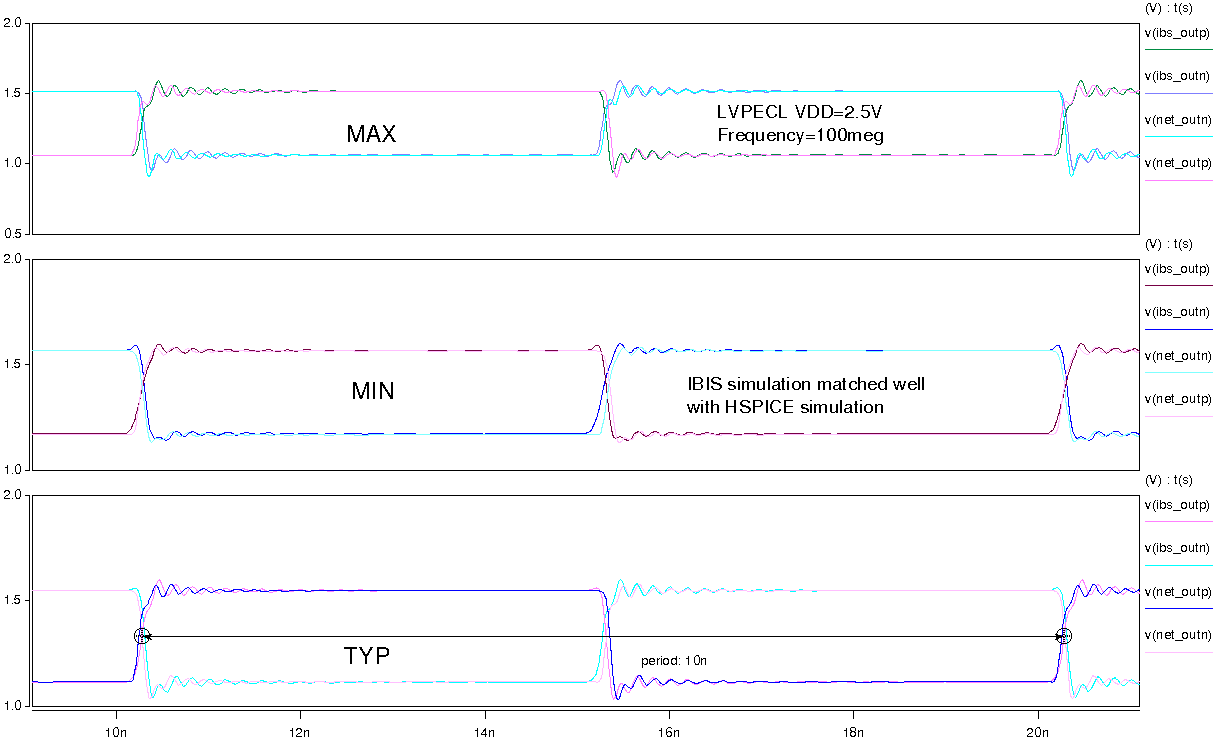
VDD=3.3V



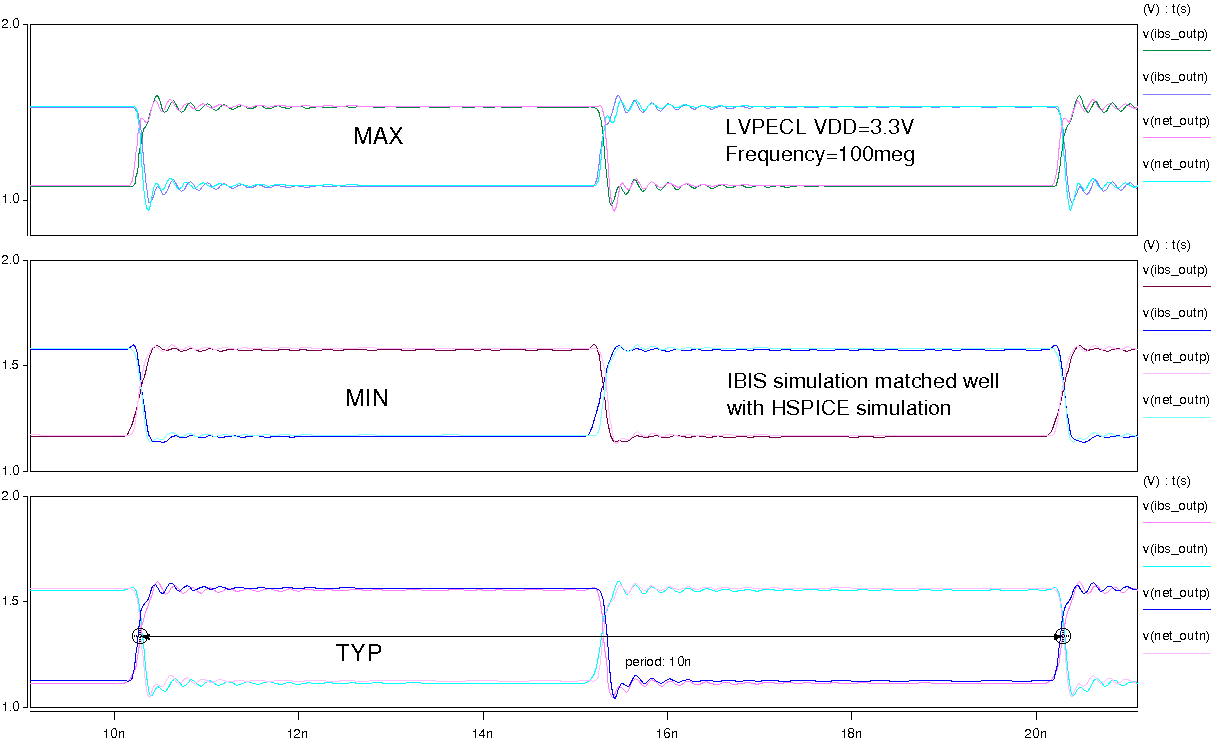
1. **LVDS simulation:**

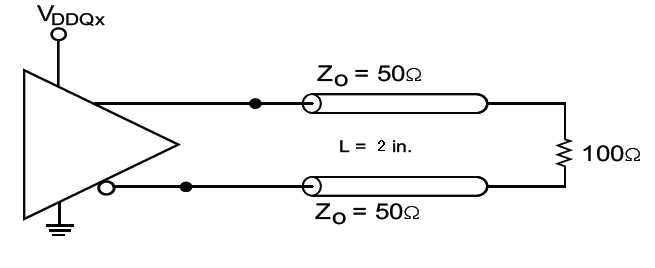


VDD=2.5V

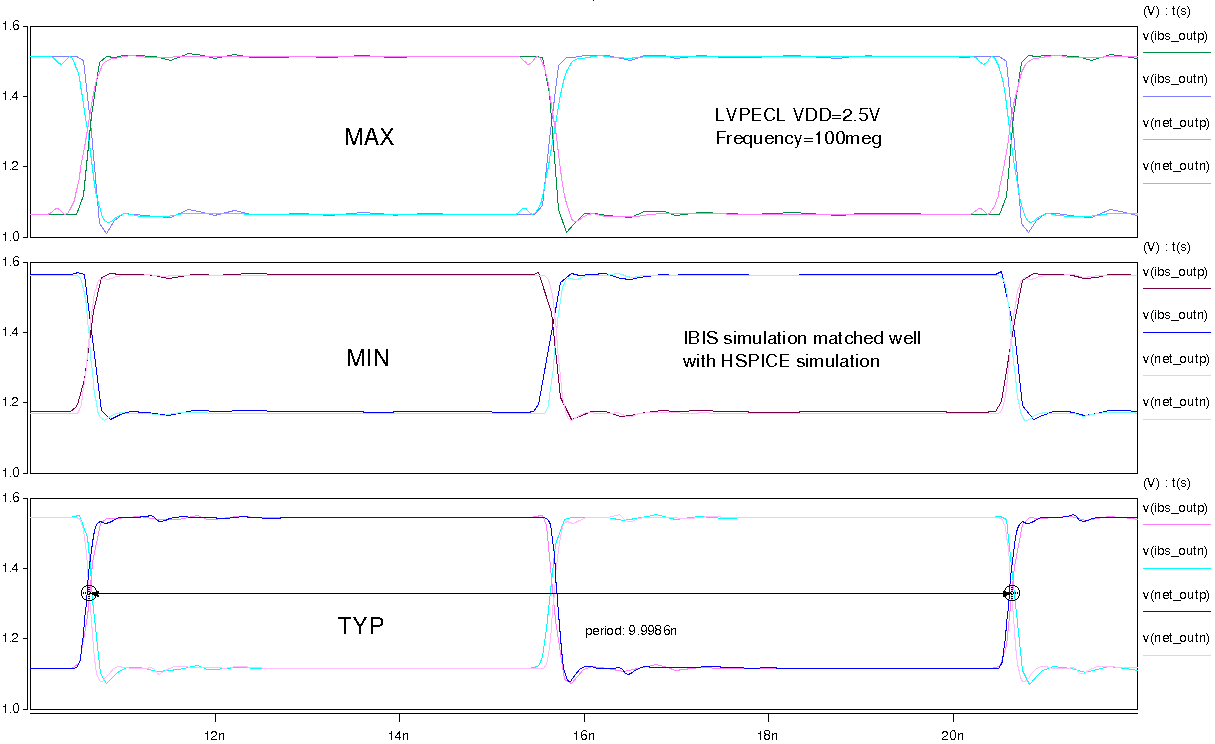


VDD=3.3V

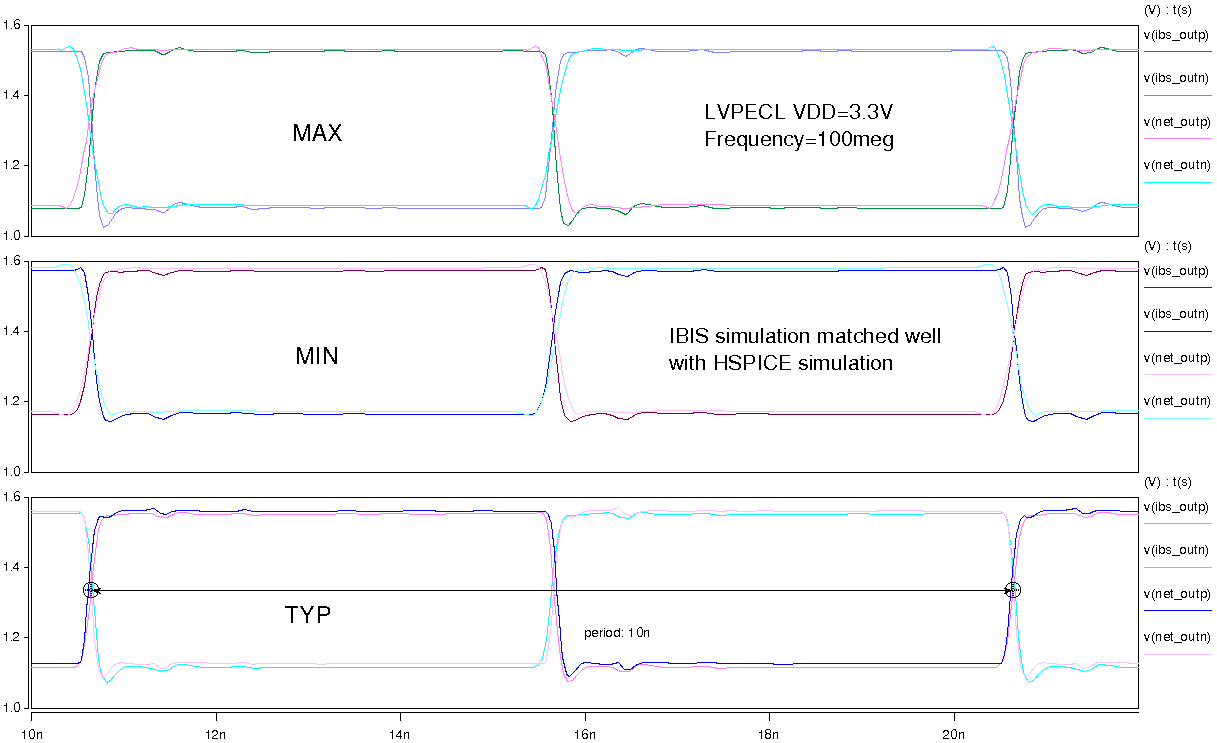




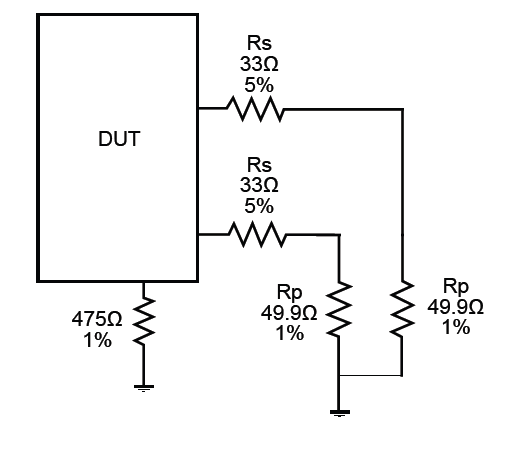
VDD=2.5V



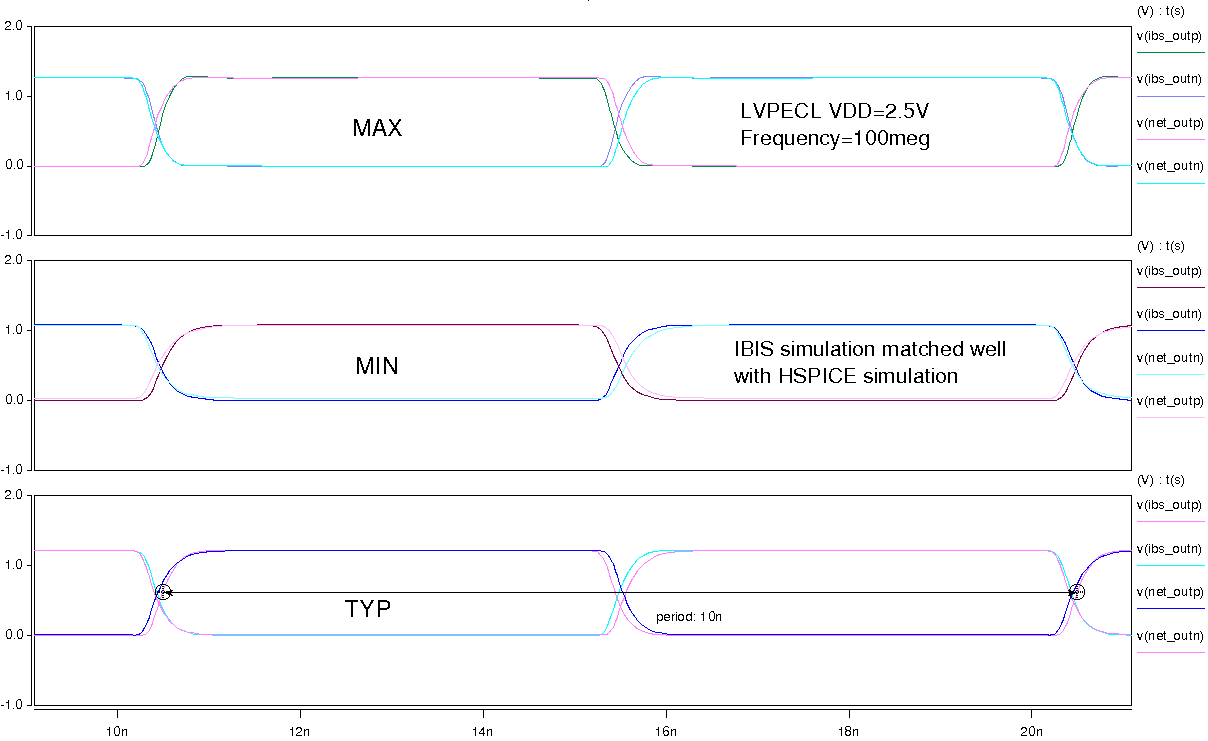
VDD=3.3V



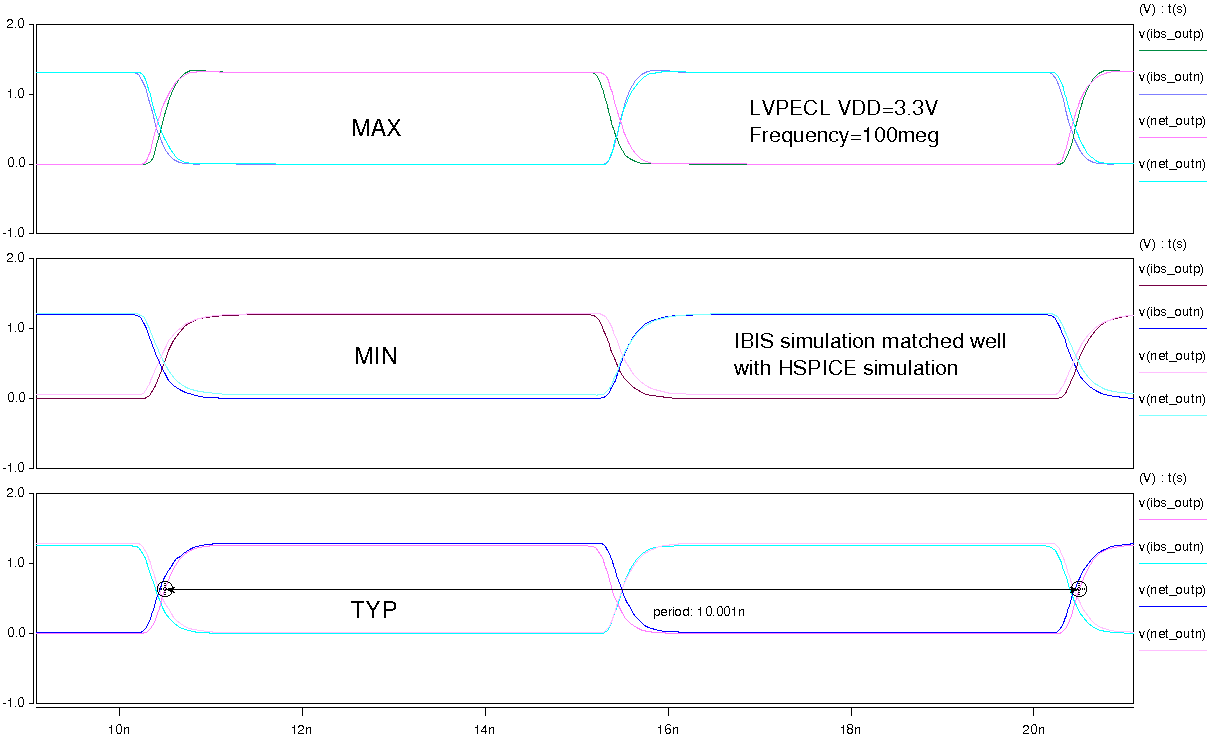
1. **HCSL simulation:**

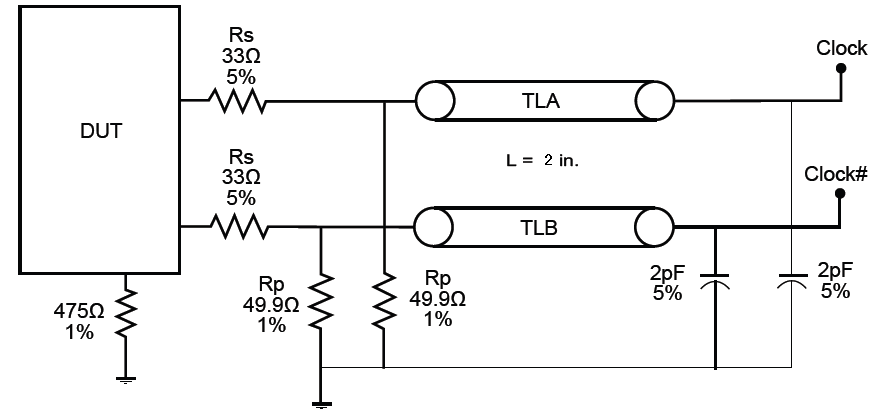


VDD=2.5V

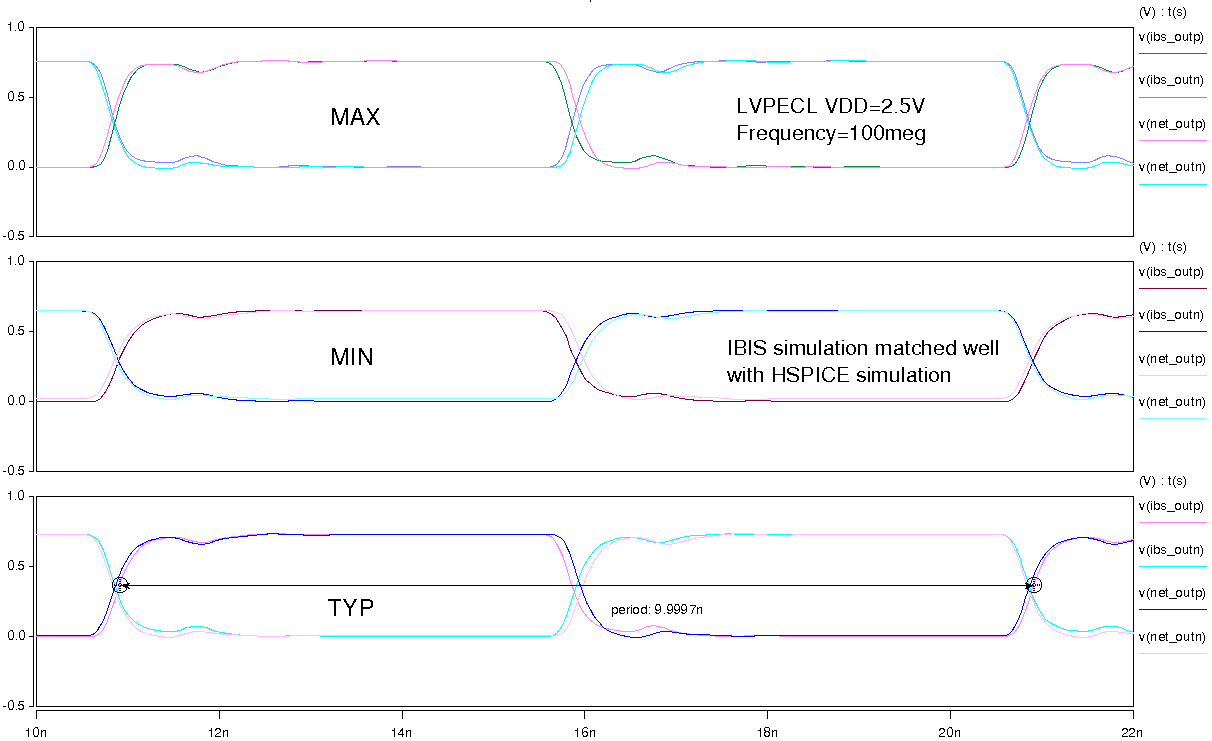


VDD=3.3V





VDD=2.5V



VDD=3.3V

