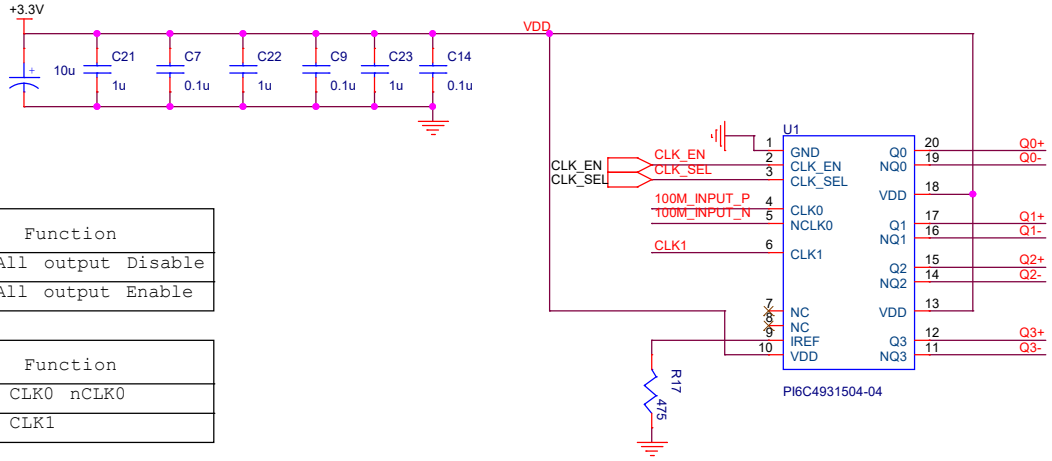
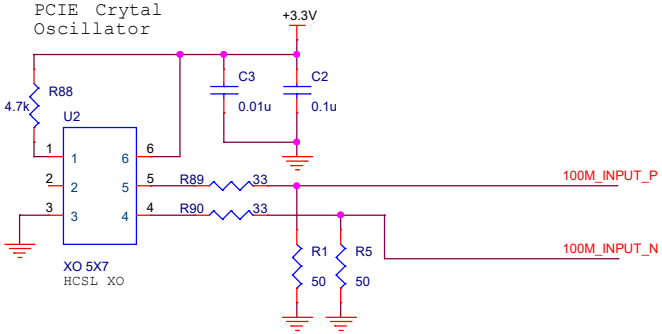
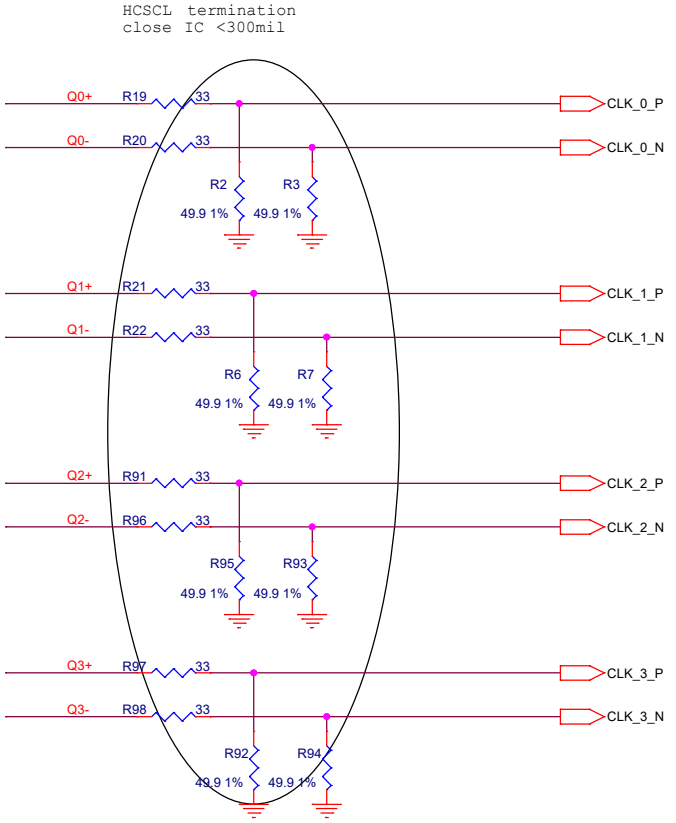


CLK_EN	Function
0	All output Disable
1	All output Enable

CLK_SEL	Function
0	CLK0 nCLK0
1	CLK1



Or, other HCSL
clock gen. output



App Note:

1. Select CLK0 or CLK1 as input ;
2. Each VDD pin needs 0.1u +1uF decoupling close to pin. (e.g.: VDD,..etc)
3. Place serial 33 ohm and 49.9 ohm pull-down in comp. side close to pin <=300mil.
4. Put 475 ohm resistor closed to IREF Pin

Title: PI6C4931504-04_App schematic		
Size: B	Document Number: Diodes Inc. Clock IC Application Engineering	Rev: 1.0
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