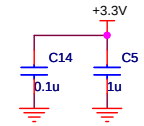
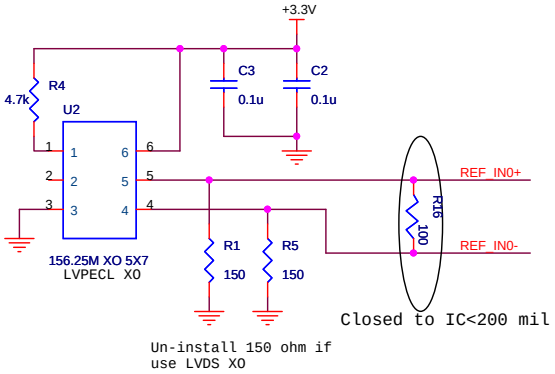
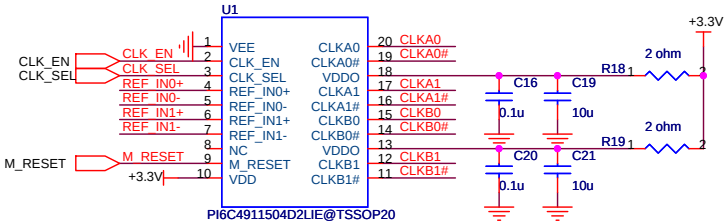
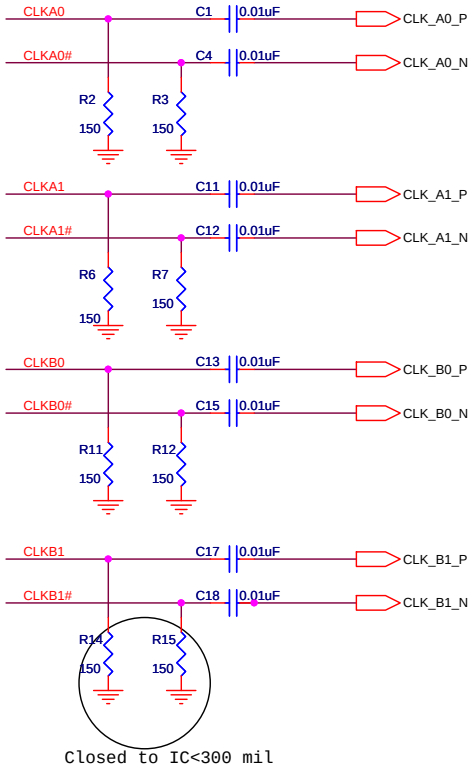
Input				Output	
M_Reset	CLK_EN	CLK_SEL	SOURCE	CLKA0 CLKA1 CLKB0 CLKB1	CLKA0# CLKA1# CLKB0# CLKB1#
1	X	X	X	LOW	HIGH
0	0	0	Ref_IN0	Disabled LOW	Disabled HIGH
0	0	1	Ref_IN1	Disabled LOW	Disabled HIGH
0	1	0	Ref_IN0	Enabled	Enabled
0	1	1	Ref_IN1	Enabled	Enabled









App Note:

1. Select Ref_IN0 or Ref_IN1 as input ;
2. Each VDD pin must have 0.1uF decoupling cap.; better has 1u more;
3. Place 150ohm pull-down in comp. side close to pin <=300mil.
4. Suggest to use DC coupling in LVPECL/LVDS drive input clock with 100ohm corss at input pins <200mil;
5. when in AC input drive either just use 100ohm cross to bias balance
6. If use CMOS XO drive, needs 1k pull-up/down at REF_IN_ pin, refer to datasheet app. page

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