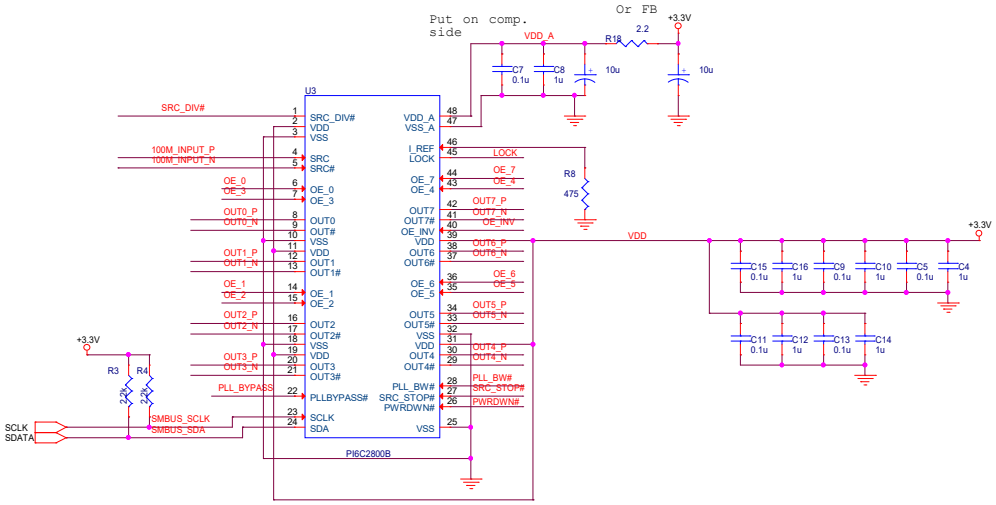
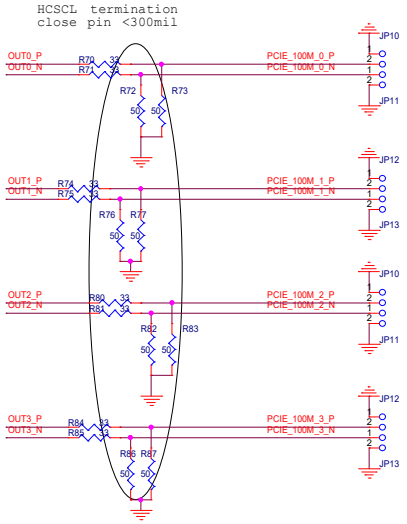
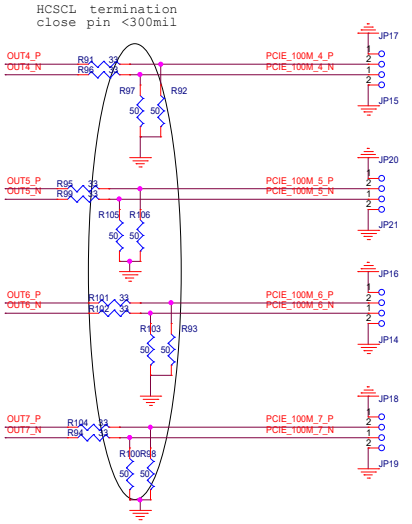
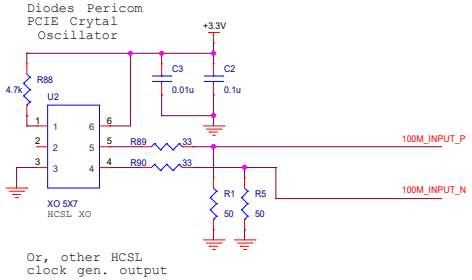








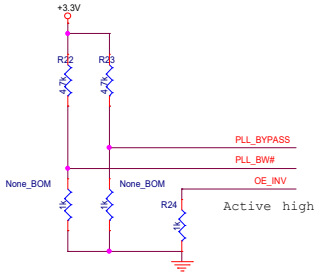
OE_0

Make individual OE_x pull-up/down to enable/disable

. . .

Active high

OE_7



PLL/BYPASS#:

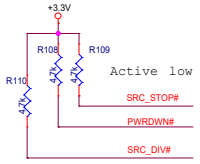
0: BYPASS; 1: PLL

PLL_BW#:

0: High BW; 1: Low BW

OE_INV:

0: Same stage;
1: OE_[0:7], SRC_STOP#, PWRDWN# inverted.



SRC_STOP#/PWRDWN#/SRC_DIV#:

Active low.

LOCK#:

Transition high when PLL lock is achieved (Latched output)

App Note:

1. Each VDD pin needs 0.1u +1uF decoupling close to pin. (e.g.: VDD,VDD_A...etc)

2. VDDA use small R=1~2 ohm or FB(ferrite bead)+C=10uF filtering for better DC/DC ripple noise rejection

3. Place serial 33 ohm and 50 ohm pull-down in comp. side close to pin <=300mil.

4. Put 475 ohm resistor closed to IREF Pin

Title	PI6C20800B App. Schematic	
Size C	Document Number Diodes Inc. Clock IC Application Engineering	Rev 1.0
Date: Thursday, October 26, 2023	Sheet 1 of 1	