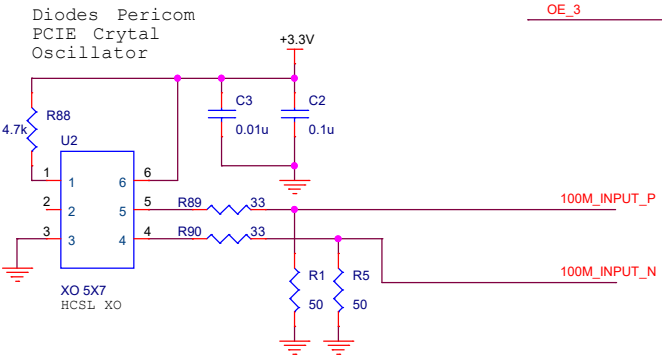


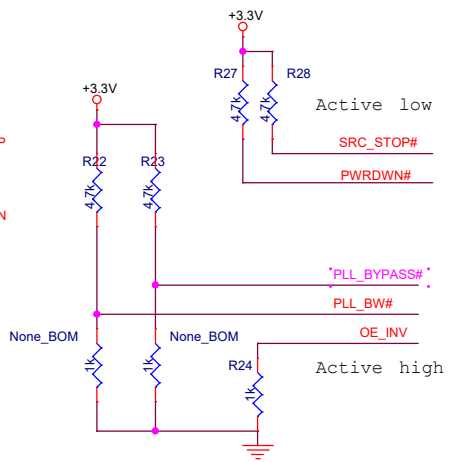
OE_0

Make individual OE x pull-up/down to enable/disable dedicated output:
 OE_0 for OUT0 / OUT0#
 .
 .
 OE_3 for OUT3 / OUT3#

OE_3



Or, other HCSL clock gen. output

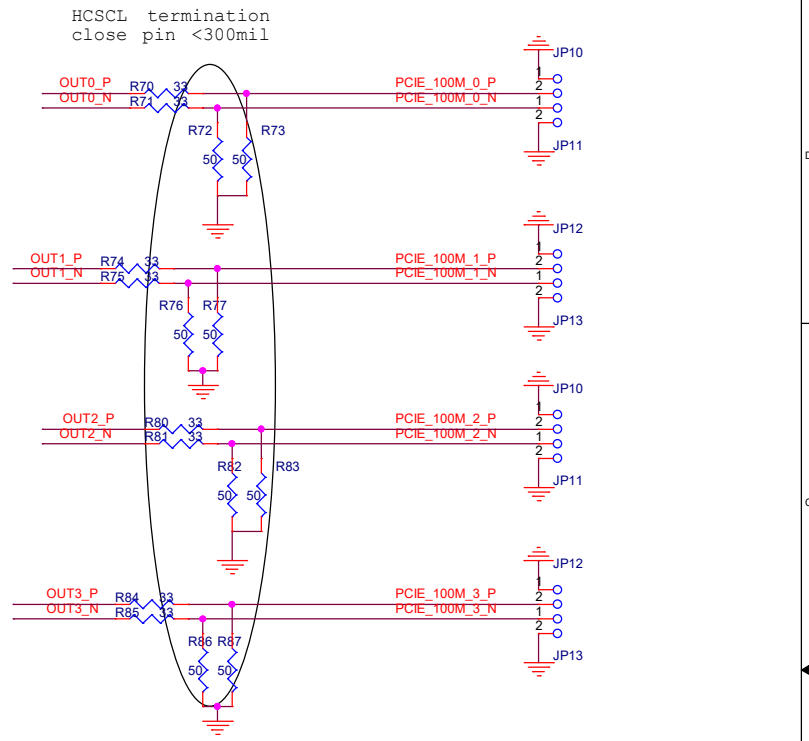


SRC_STOP#/PWRDWN#:
Active low.

PLL/BYPASS#:
0: BYPASS; 1: PLL

PLL_BW#:
0: High BW; 1: Low BW

OE_INV:
0: Same stage; 1: OE_0, OE_3, SRC_STOP#, PWRDWN# inverted.



App Note:

1. Each VDD pin needs 0.1u +1uF decoupling close to pin. (e.g.: VDD, VDD_A...etc)
2. VDDA use small R=1~2 ohm or FB(ferrite bead)+C=10uF filtering for better DC/DC ripple noise rejection
3. Place serial 33 ohm and 50 ohm pull-down in comp. side close to pin <=300mil.
4. Put 475 ohm resistor closed to IREF Pin

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