**Verification of PI6C10806B IBIS model**

1. **Introduction: to verify the correlation between the ibis model and hspice model, we need to do some simulations:**

**The frequency of signal is 20MHz:** Vin in 0 pulse (0 pwr 0 0.1n 0.1n 24.9n 50n)

1. Without any load to the OUTPUT
2. Add **50Ω** resistor to 1/2 VDD, and 5pf pull-down capacitance to the OUTPUT

PI6C10806B

**VOUT**

**SCL\_C**

**SDA\_C**

**R**

**SCL\_C**

**SDA\_C**

**Input Signals**

**SCL\_C**

**SDA\_C**

**VIN**

**SCL\_C**

**SDA\_C**

CLK0

**SCL\_C**

**SDA\_C**

IN

**SCL\_C**

**SDA\_C**

**1/2 VDD**

**SCL\_C**

**SDA\_C**

**C**

**SCL\_C**

**SDA\_C**

1. Add 50Ω resistor to 1/2 VDD directly:
2. Add 50Ω resistor between OUTPUT and **out1**, and then add 100Ω Pull-Up and 100Ω pull-down resistors to **out1**:
3. Add **33Ω** resistor, 5 inches trace and 5pf pull-down capacitance to the OUTPUT

**VOUT**

**SCL\_C**

**SDA\_C**

IN

**SCL\_C**

**SDA\_C**

**Input Signals**

**SCL\_C**

**SDA\_C**

**VIN**

**SCL\_C**

**SDA\_C**

CLK0

**SCL\_C**

**SDA\_C**

5-inch

PI6C10806B

-06

**C**

**SCL\_C**

**SDA\_C**

**R**

**SCL\_C**

**SDA\_C**

1. **Conclusion:**

Without any load to the output, the simulation result of IBIS model is ideal, while Add **50Ω pull-down** resistor to the output, the result is a little bad with **obvious undershoot**.

1. **Simulation Result:**
2. Without any load to the output



1. Add 50Ω resistor to 1/2 VDD, and 5pf pull-down capacitance to the OUTPUT
2. Add 50Ω resistor to 1/2 VDD directly:



1. Add 50Ω resistor between OUTPUT and **out1**, and then add 100Ω Pull-Up and 100Ω pull-down resistors to **out1**:



1. Add 33Ω resistor, 5 inches trace and 5pf pull-down capacitance to the OUTPUT

