**Verification of PI4IOE5V9554 IBIS model**

**Introduction:**

To verify the correlation between the ibis model and hspice model, we need to do some simulations:

1. IO**(I/O)**

PI4IOE5V9554

**VOUT**

**SCL\_C**

**SDA\_C**

**R**

**SCL\_C**

**SDA\_C**

input

**SCL\_C**

**SDA\_C**

**Input Signals**

**SCL\_C**

**SDA\_C**

**VIN**

**SCL\_C**

**SDA\_C**

**VDD**

**SCL\_C**

**SDA\_C**

IO0

**SCL\_C**

**SDA\_C**

…..

**SCL\_C**

**SDA\_C**

**The frequency of signal is 5MHz:**

Vin input 0 pulse (0 power 0 1n 1n 99n 200n)

1. Add **1kΩ** pull-up resistor and **without** package data to the output;
2. With **ZH** package data to the output;
3. With **L** package data to the output.
4. OUTPUT**(\_INT)**

PI4IOE5V9554

**VOUT**

**SCL\_C**

**SDA\_C**

**R**

**SCL\_C**

**SDA\_C**

input

**SCL\_C**

**SDA\_C**

**Input Signals**

**SCL\_C**

**SDA\_C**

**VIN**

**SCL\_C**

**SDA\_C**

**VDD**

**SCL\_C**

**SDA\_C**

\_INT

**SCL\_C**

**SDA\_C**

…..

**SCL\_C**

**SDA\_C**

**The frequency of signal is 20MHz:**

Vin input 0 pulse (0 power 0 1n 1n 24n 50n)

1. Add **1kΩ** pull-up resistor and **without** package data to the output;
2. With **ZH** package data to the output;
3. With **L** package data to the output.
4. IO\_OD**(SDA)**

PI4IOE5V9554

**VOUT**

**SCL\_C**

**SDA\_C**

**R**

**SCL\_C**

**SDA\_C**

input

**SCL\_C**

**SDA\_C**

**Input Signals**

**SCL\_C**

**SDA\_C**

**VIN**

**SCL\_C**

**SDA\_C**

**VDD**

**SCL\_C**

**SDA\_C**

SDA

**SCL\_C**

**SDA\_C**

…..

**SCL\_C**

**SDA\_C**

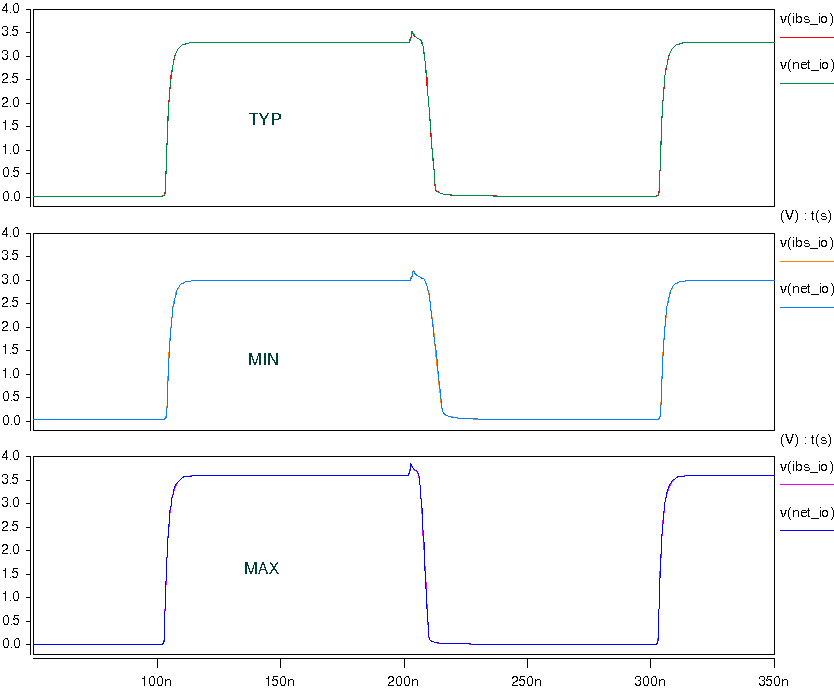
**The frequency of signal is 20MHz:**

Vin input 0 pulse (0 power 0 1n 1n 24n 50n)

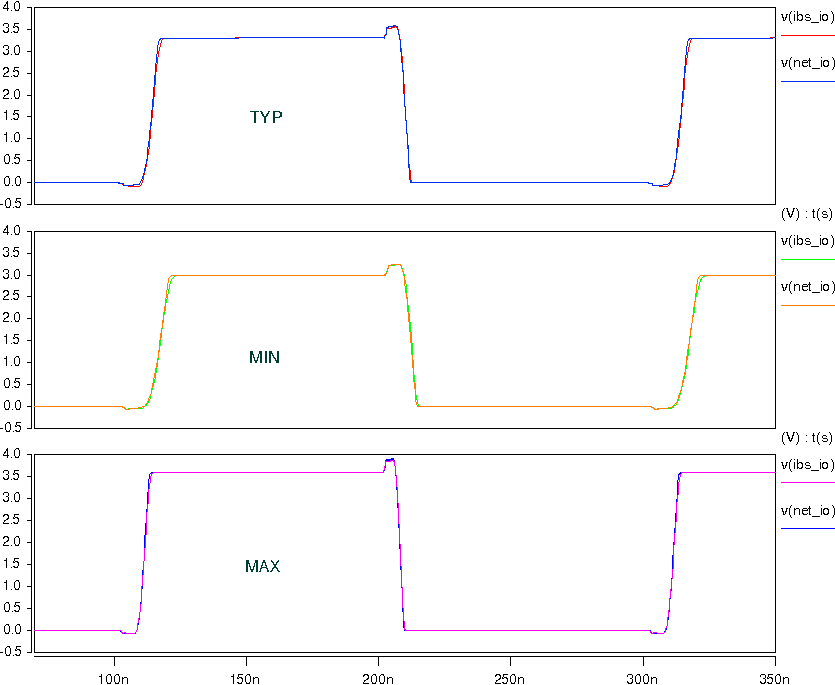
1. Add **1kΩ** pull-up resistor and **without** package data to the output;
2. With **ZH** package data to the output;
3. With **L** package data to the output.

**Simulation Result:**

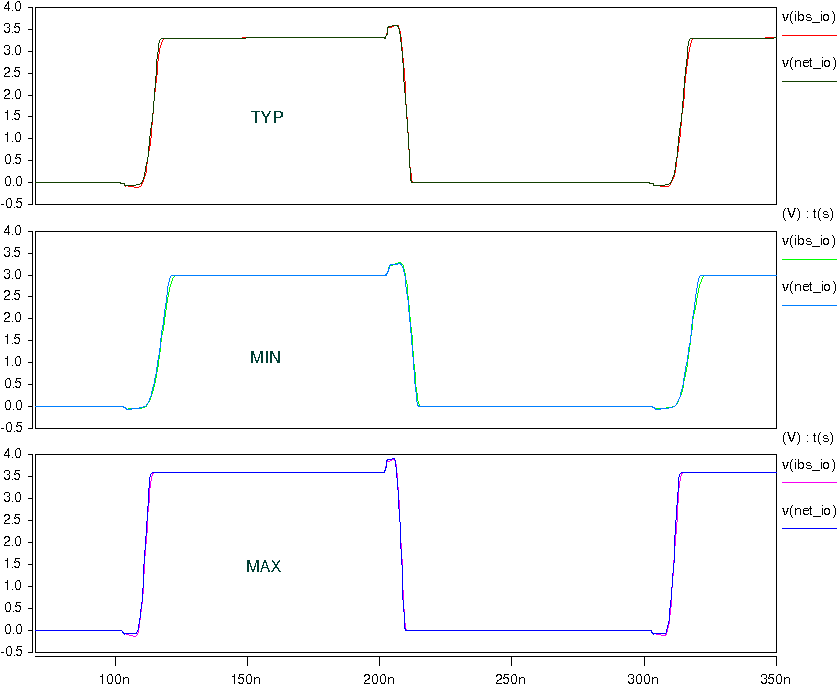
1. IO
2. Add **1kΩ** pull-up resistor and **without** package data to the output;



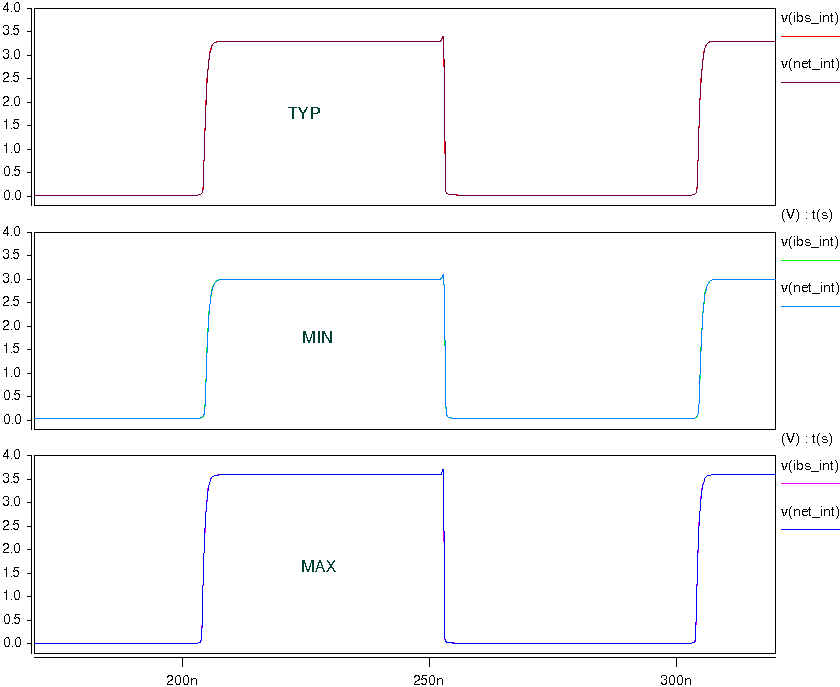
1. With **ZH** package data to the output;



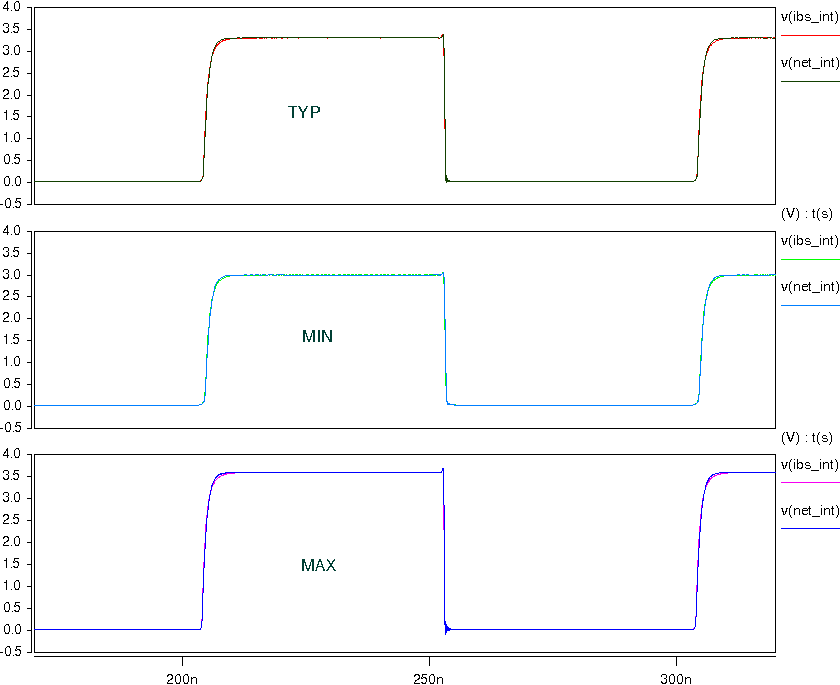
1. With **L** package data to the output.



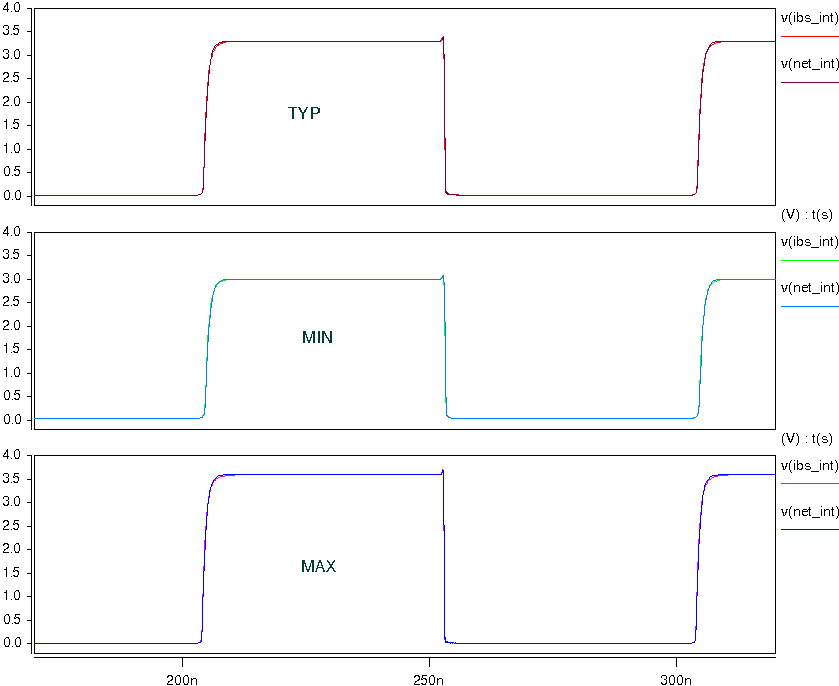
1. OUTPUT
2. Add **1kΩ** pull-up resistor and **without** package data to the output;



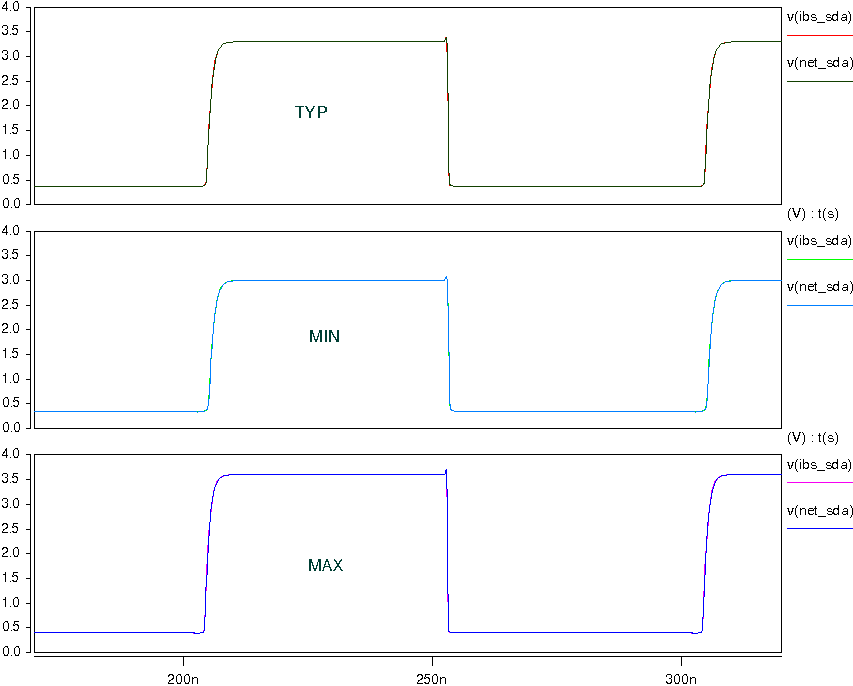
1. Add **1kΩ** pull-up resistor and with **ZH** package data to the output;



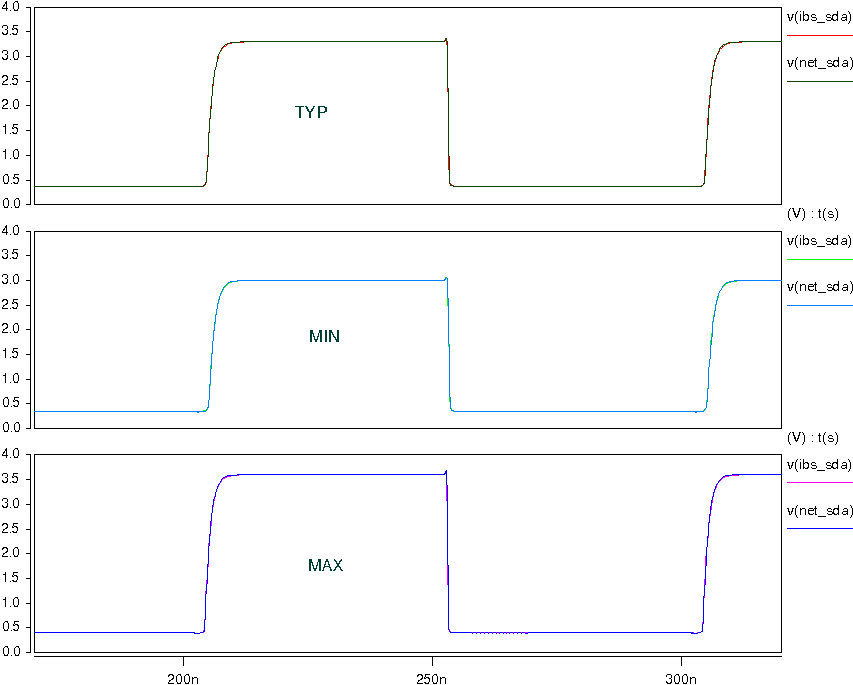
1. Add **1kΩ** pull-up resistor and with **L** package data to the output.



1. IO\_OD
2. Add **1kΩ** pull-up resistor and **without** package data to the output;



1. Add **1kΩ** pull-up resistor and with **ZH** package data to the output;



1. Add **1kΩ** pull-up resistor and with **L** package data to the output.

